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SEMICONDUCTOR

FIN1047 3.3V LVDS 4-Bit Flow-Through High Speed Differential Driver

General Description

This quad driver is designed for high speed interconnects utilizing Low Voltage Differential Signaling (LVDS) technology. The driver translates LVTTL signal levels to LVDS levels with a typical differential output swing of 350mV which provides low EMI at ultra low power dissipation even at high frequencies. This device is ideal for high speed transfer of clock and data.

The FIN1047 can be paired with its companion receiver, the FIN1048, or any other LVDS receiver.

Features

- Greater than 400Mbs data rate
- Flow-through pinout simplifies PCB layout
- 3.3V power supply operation
- 0.4 ns maximum differential pulse skew
- 1.7 ns maximum propagation delay
- Low power dissipation
- Power-Off protection
- Meets or exceeds the TIA/EIA-644 LVDS standard
 Pin compatible with equivalent RS-422 and LVPECL devices

June 2001

Revised August 2003

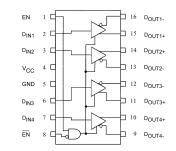
■ 16-Lead SOIC and TSSOP packages save space

Ordering Code:

FIN1047M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
FIN1047MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Pin Descriptions

Pin Name	Description
D _{IN1} , D _{IN2} , D _{IN3} , D _{IN4}	LVTTL Data Inputs
D _{OUT1+} , D _{OUT2+} , D _{OUT3+} , D _{OUT4+}	Non-Inverting Driver Outputs
D _{OUT1-} , D _{OUT2-} , D _{OUT3-} , D _{OUT4-}	Inverting Driver Outputs
EN	Driver Enable Pin
EN	Inverting Driver Enable Pin
V _{CC}	Power Supply
GND	Ground

Truth Table

	Inputs		Out	puts
EN	EN	D _{IN}	D _{OUT+}	D _{OUT-}
Н	L or OPEN	Н	Н	L
Н	L or OPEN	L	L	Н
Н	L or OPEN	OPEN	L	Н
Х	Н	Х	Z	Z
L or OPEN	Х	Х	Z	Z
H = HIGH Logic X = Don't Care		/ Logic Level h Impedance		

Absolute Maximum Ratings(Note 1)

Supply Voltage (V _{CC})	-0.5V to +4.6V
	0.01 10 1 1.01
DC Input Voltage (V _{IN})	-0.5V to +6V
DC Input Voltage (V _{OUT})	-0.5V to 4.6V
Driver Short Circuit Current (I _{OSD})	Continuous
Storage Temperature Range (T _{STG})	$-65^{\circ}C$ to $+150^{\circ}C$
Max Junction Temperature (T _J)	150°C
Lead Temperature (T _L)	260°C
(Soldering, 10 seconds)	
ESD (Human Body Model)	≥ 9000V
ESD (Machine Model)	≥ 1200V

Recommended Operating Conditions

Supply Voltage (V _{CC})	3.0V to 3.6V
Input Voltage (V _{IN})	0 to V_{CC}
Operating Temperature (T _A)	$-40^{\circ}C$ to $+85^{\circ}C$

Note 1: The "Absolute Maximum Ratings": are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. Fairchild does not recommend operation of circuits outside databook specification.

DC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ (Note 2)	Мах	Units
V _{OD}	Output Differential Voltage		250	340	450	mV
ΔV_{OD}	V _{OD} Magnitude Change from Differential LOW-to-HIGH	$R_L = 100\Omega$, Driver Enabled,		1.4	25	mV
V _{OS}	Offset Voltage	See Figure 1	1.125	1.25	1.375	V
ΔV_{OS}	Offset Magnitude Change from Differential LOW-to-HIGH			1.2	25	mV
V _{OH}	HIGH Output Voltage	$V_{IN} = V_{CC}$		1.4	1.6	V
V _{OL}	LOW Output Voltage	$V_{IN} = 0V$	0.9	1.05		V
I _{OFF}	Power Off Output Current	V _{CC} = 0V, V _{OUT} = 0V or 3.6V	-20		20	μA
I _{OS}	Short Circuit Output Current	V _{OUT} = 0V, Driver Enabled		-3	-6	mA
		V _{OD} = 0V, Driver Enabled		-3.5	-6	IIIA
V _{IH}	Input HIGH Voltage		2.0		V _{CC} + 1.0	V
VIL	Input LOW Voltage (Note 3)		GND		0.8	V
I _{IN}	Input Current	$V_{IN} = 0V \text{ or } V_{CC}$	-20		20	μA
I _{oz}	Disabled Output Leakage Current	$V_{OUT} = 0V \text{ or } 4.6V$	-20		20	μA
I _{I(OFF)}	Power-Off Input Current	V _{CC} = 0V, V _{IN} = 0V or 3.6V	-20		20	μA
V _{IK}	Input Clamp Voltage	I _{IK} = -18 mA	-1.5	-0.7		V
I _{CC}	Power Supply Current	No Load, $V_{IN} = 0V$ or V_{CC} , Driver Enabled		5	8	
		$R_L = 100 \Omega$, Driver Disabled		1.7	4	mA
		R_L = 100 Ω,V_{IN} = 0V or $V_{CC},Driver$ Enabled		16	22	
I _{PU/PD}	Output Power Up/Power Down High Z Leakage Current	V _{CC} = 0V or 1.5V	-20		20	μA

Note 2: All typical values are at $T_A=25^\circ C$ and with $V_{CC}=3.3 V.$

Note 3: For transient conditions when $t \leq 5ns$ and $I_{IN} \leq -100$ mA, $V_{ILmin} = -1.0V.$

Symbol	Parameter	Test Conditions	Min	Typ (Note 4)	Max	Units
t _{PLHD}	Differential Propagation Delay LOW-to-HIGH		0.6	1.1	1.7	ns
t _{PHLD}	Differential Propagation Delay HIGH-to-LOW		0.6	1.2	1.7	ns
t _{TLHD}	Differential Output Rise Time (20% to 80%)	$R_L = 100 \Omega$, $C_L = 10 pF$,	0.4		1.2	ns
t _{THLD}	Differential Output Fall Time (80% to 20%)	See Figure 2 (Note 8), and Figure 3	0.4		1.2	ns
t _{SK(P)}	Pulse Skew t _{PLH} - t _{PHL}	-			0.4	ns
t _{SK(LH)}	Channel-to-Channel Skew	-		0.05	0.3	ns
t _{SK(HL)}	(Note 5)			0.05	0.5	115
t _{SK(PP)}	Part-to-Part Skew (Note 6)				1.0	ns
f _{MAX}	Maximum Frequency (Note 7)	$R_L = 100\Omega$, See Figure 6 (Note 8)	200	250		MHz
t _{ZHD}	Differential Output Enable Time from Z to HIGH			1.7	5.0	ns
t _{ZLD}	Differential Output Enable Time from Z to LOW	$R_L = 100\Omega$, $C_L = 10$ pF,		1.7	5.0	ns
t _{HZD}	Differential Output Disable Time from HIGH to Z	See Figure 4 (Note 8), and Figure 5		2.7	5.0	ns
t _{LZD}	Differential Output Disable Time from LOW to Z			2.7	5.0	ns
CIN	Input Capacitance			4.2		pF
COUT	Output Capacitance			5.2		pF

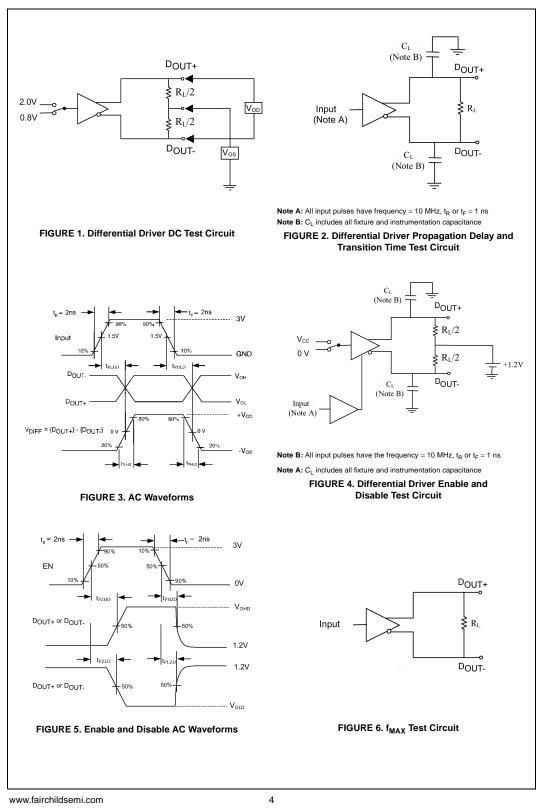
Note 4: All typical values are at $T_A = 25^{\circ}C$ and with $V_{CC} = 3.3V$.

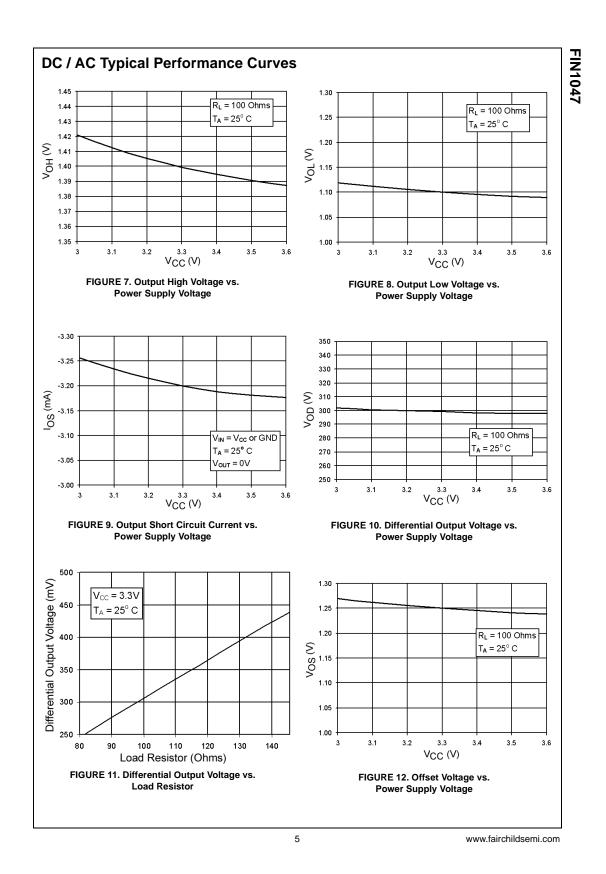
Note 5: $t_{SK(LH)}$, $t_{SK(HL)}$ is the skew between specified outputs of a single device when the outputs have identical loads and are switching in the same direction.

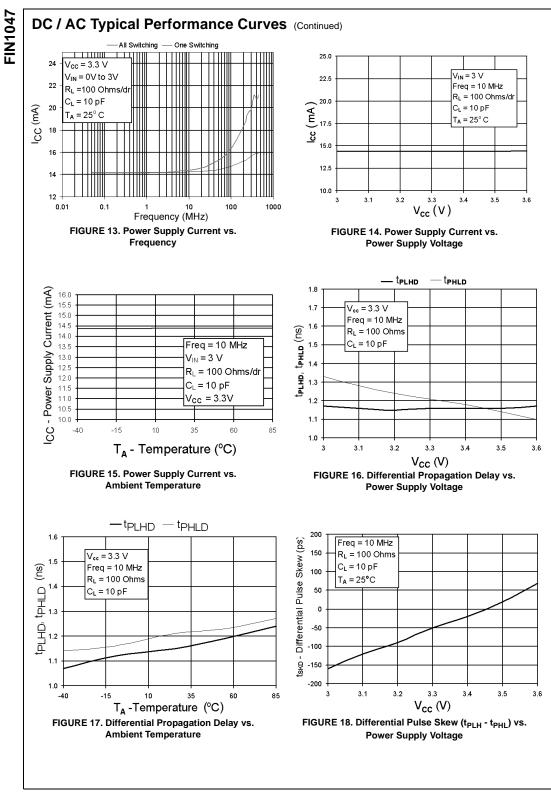
Note 6: $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices switching in the same direction (either LOW-to-HIGH or HIGH-to-LOW) when both devices operate with the same supply voltage, same temperature, and have identical test circuits. Note 7: f_{MAX} criteria: Input $t_R = t_F < 1ns$, 0V to 3V, 50% Duty Cycle; Output $V_{OD} > 250$ mv, 45% to 55% Duty Cycle; all switching in phase channels. Note 8: Test Circuits in Figures 2, 4, 6 are simplified representations of test fixture and DUT loading.

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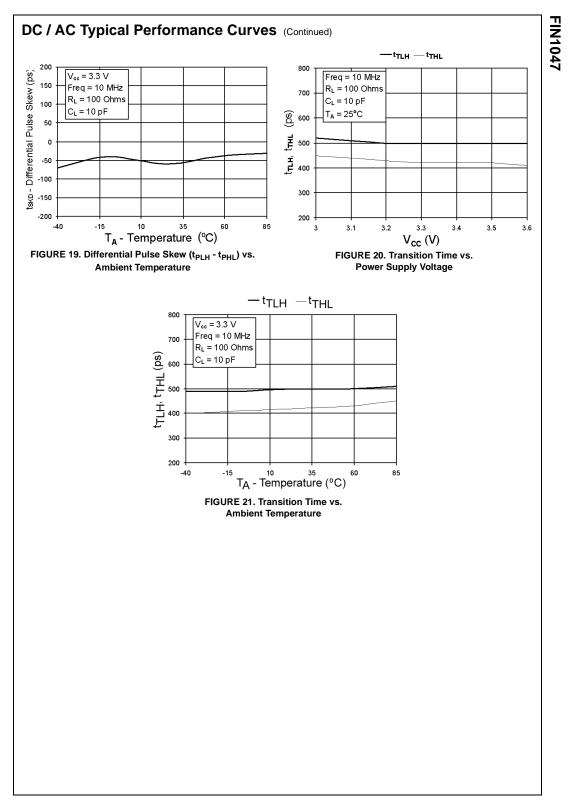
FIN1047

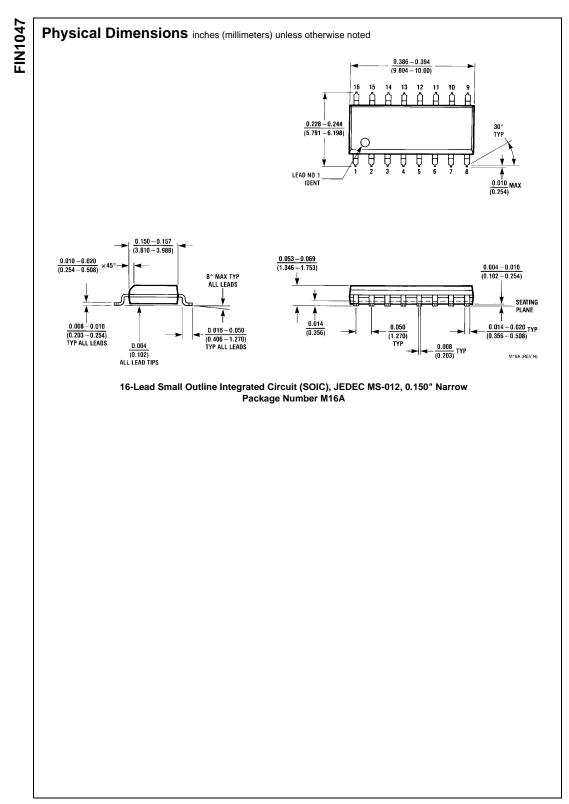


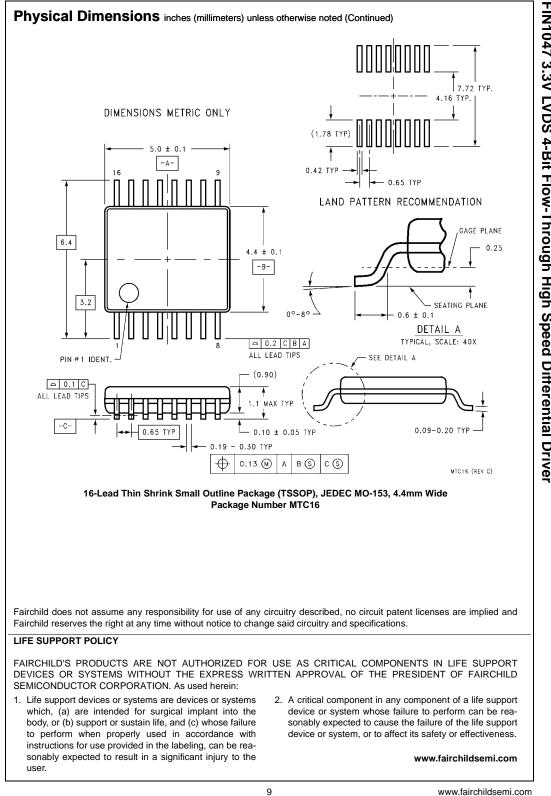




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