FAIRCHILD SEMICONDUCTOR™

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# GTLP1B151
# 1-Bit LVTTL/GTLP Transceiver with Separate LVTTL Port and Feedback Path

## General Description

The GTLP1B151 is a 1-bit transceiver that provides LVTTL-to-GTLP signal level translation. Individual LVTTL and GTLP driver enables are also available. The GTLP1B151 offers separate LVTTL inputs and outputs, and can provide a feedback path for control and diagnostics monitoring.

High-speed backplane operation is a direct result of GTLP's reduced output swing (<1V), reduced input threshold levels and output edge rate control. The edge rate control minimizes bus-settling time. GTLP is a Fairchild Semiconductor derivative of the Gunning Transistor Logic (GTL) JEDEC standard JESD8-3.

Fairchild's GTLP has internal edge-rate control and is process, voltage and temperature compensated. GTLP's I/O structure is similar to GTL and BTL but offers different output levels and receiver threshold. Typical GTLP output voltage levels are: $V_{OL}$ = 0.5V, $V_{OH}$ = 1.5V, and $V_{REF}$ = 1V.

## Features

- Separate LVTTL inputs and outputs
- A feedback path for control and diagnostics monitoring
- Bidirectional interface between GTLP and LVTTL logic levels
- Designed with edge rate control circuitry to reduce output noise on the GTLP port
- $V_{REF}$ pin provides external supply reference voltage for receiver threshold adjustibility
- Special PVT compensation circuitry to provide consistent performance over variations of process, supply voltage and temperature
- TTL compatible driver and control inputs
- Designed using Fairchild advanced BiCMOS technology
- Bushold data inputs on A port to eliminate the need for external pull-up resistors for unused inputs
- Power up/down and power off high impedance for live insertion
- Open drain on GTLP to support wired-or connection
- Flow through pinout optimizes PCB layout
- A Port source/sink –24mA / +24mA
- B Port sink +50mA

## Ordering Code:

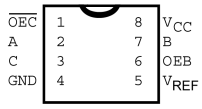
| Order Number | Package Number | Package Description |
|---|---|---|
| GTLP1B151M | M08A | 8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow [TUBE] |
| GTLP1B151MX | M08A | 8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow [TAPE and REEL] |
| GTLP1B151K8X | MAB08A (Preliminary) | 8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide [TAPE and REEL] |

## Pin Descriptions

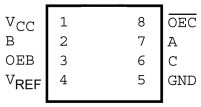
| Pin Names | Description |
|---|---|
| OEB, $\overline{OEC}$ | LVTTL Individual Output Enable Controls ($\overline{OEC}$ is Active LOW) |
| $V_{CC}$, GND, $V_{REF}$ | Device Supplies |
| A | A Port LVTTL Input |
| B | B Port GTLP Input/Output |
| C | C Port LVTTL Output |

## Connection Diagrams

**US8**




**SOIC**



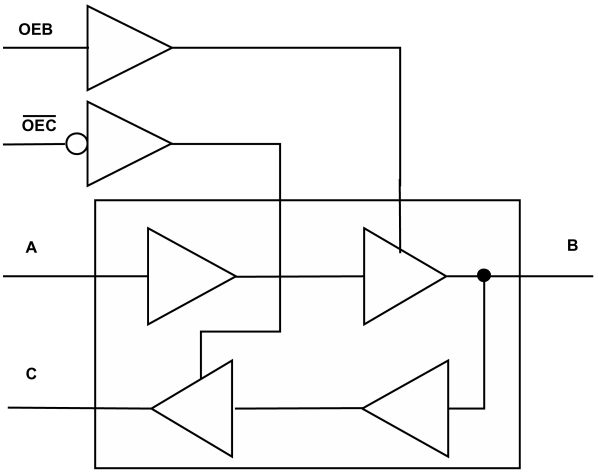

## Functional Description

The GTLP1B151 is a 1-bit transceiver that supports GTLP and LVTTL signal levels. Data polarity is non-inverting with separate LVTTL inputs and outputs and there are individual GTLP and LVTTL output enable controls.

## Functional Tables

| Inputs | | | | Outputs | | Description |
|---|---|---|---|---|---|---|
| OEB | $\overline{OEC}$ | $A_n$ | $B_n$ | $B_n$ | $C_n$ | |
| H | L | L | Output | L | L | B Bus Enabled, C Bus Enabled |
| H | L | H | Output | H | H | B Bus Enabled, C Bus Enabled |
| H | H | L | Output | L | Z | B Bus Enabled, C Bus Disabled |
| H | H | H | Output | H | Z | B Bus Enabled, C Bus Disabled |
| L | H | L | L | Z | Z | B Bus Disabled, C Bus Disabled |
| L | H | H | H | Z | Z | B Bus Disabled, C Bus Disabled |
| L | L | N/A | L | Z | L | B Bus Disabled, C Bus Enabled |
| L | L | N/A | H | Z | H | B Bus Disabled, C Bus Enabled |

## Logic Diagram



## Absolute Maximum Ratings(Note 1)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5V to +4.6V |
| DC Input Voltage ($V_I$) | −0.5V to +4.6V |
| DC Output Voltage ($V_O$) | |
| Outputs 3-STATE | −0.5V to +4.6V |
| Outputs Active (Note 2) | −0.5V to +4.6V |
| DC Output Sink Current into | |
| C Port $I_{OL}$ | 48 mA |
| DC Output Source Current from | |
| C Port $I_{OH}$ | −48 mA |
| DC Output Sink Current into | |
| B Port in the LOW State, $I_{OL}$ | 100 mA |
| DC Input Diode Current ($I_{IK}$) | |
| $V_I < 0V$ | −50 mA |
| DC Output Diode Current ($I_{OK}$) | |
| $V_O < 0V$ | −50 mA |
| ESD Rating | >2000V |
| Storage Temperature ($T_{STG}$) | −65°C to +150°C |

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage $V_{CC}$ | 3.15V to 3.45V |
| Bus Termination Voltage ($V_{TT}$) | |
| GTLP | 1.47V to 1.53V |
| $V_{REF}$ | 0.98V to 1.02V |
| Input Voltage ($V_I$) | |
| on A Port and Control Pins | 0.0V to $V_{CC}$ |
| HIGH Level Output Current ($I_{OH}$) | |
| C Port | −24 mA |
| LOW Level Output Current ($I_{OL}$) | |
| C Port | +24 mA |
| B Port | +50 mA |
| Operating Temperature ($T_A$) | −40°C to +85°C |

**Note 1:** Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 2:** $I_O$ Absolute Maximum Rating must be observed.

## DC Electrical Characteristics

Over Recommended Operating Free-Air Temperature Range, $V_{REF}$ = 1.0V (unless otherwise noted).

| Symbol | | Test Conditions | | Min | Typ (Note 3) | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | B Port | | | $V_{REF}$ + 0.05 | | $V_{TT}$ | V |
| | Others | | | 2.0 | | | |
| $V_{IL}$ | B Port | | | 0.0 | | $V_{REF}$ − 0.05 | V |
| | Others | | | | | 0.8 | |
| $V_{REF}$ | B Port | | | 0.7V | 1.0 | 1.3V | V |
| $V_{TT}$ | B Port | | | $V_{REF}$ + 50 mV | 1.5 | $V_{CC}$ | V |
| $V_{IK}$ | | $V_{CC}$ = 3.15V | $I_I$ = −18 mA | | | −1.2 | V |
| $V_{OH}$ | C Port | $V_{CC}$ = Min to Max (Note 4) | $I_{OH}$ = −100 µA | $V_{CC}$ −0.2 | | | V |
| | | $V_{CC}$ = 3.15V | $I_{OH}$ = −8 mA | 2.4 | | | |
| | | | $I_{OH}$ = -24mA | 2.2 | | | |
| $V_{OL}$ | C Port | $V_{CC}$ = Min to Max (Note 4) | $I_{OL}$ = 100 µA | | | 0.2 | V |
| | | $V_{CC}$ = 3.15V | $I_{OL}$ = 8 mA | | | 0.4 | |
| | | $V_{CC}$ = 3.15V | $I_{OL}$ = 24mA | | | 0.5 | |
| | B Port | $V_{CC}$ = 3.15V | $I_{OL}$ = 40 mA | | | 0.4 | V |
| | | | $I_{OL}$ = 50 mA | | | 0.55 | |
| $I_I$ | Control Pins | $V_{CC}$ = 3.45V | $V_I$ = 3.45V | | | 5 | µA |
| | | | $V_I$ = 0V | | | −5 | |
| | A Port | $V_{CC}$ = 3.45V | $V_I$ = 3.45V | | | 10 | µA |
| | | | $V_I$ = 0V | | | −10 | |
| | B Port | $V_{CC}$ = 3.45V | $V_I$ = 3.45 | | | 5 | µA |
| | | | $V_I$ = 0 | | | −5 | |
| $I_{OFF}$ | A or C Ports, Control Pins | $V_{CC}$ = 0 | $V_I$ or $V_O$ = 0 to 3.45V | | | 30 | µA |
| | B Port | $V_{CC}$ = 0 | $V_I$ or $V_O$ = 0 to 3.45V | | | 30 | µA |
| $I_{I\ (HOLD)}$ | A Port | $V_{CC}$ = 3.15V | $V_I$ = 0.8V | 75 | | | µA |
| | | | $V_I$ = 2.0V | | | −75 | |
| $I_{OZH}$ | C Port | $V_{CC}$ = 3.45V | $V_O$ = 3.45V | | | 10 | µA |
| | B Port | | $V_O$ = 3.45V | | | 5 | |
| $I_{OZL}$ | C Port | $V_{CC}$ = 3.45V | $V_O$ = 0V | | | −10 | µA |
| | B Port | | $V_O$ = 0.0V | | | −5 | |

## DC Electrical Characteristics (Continued)

| Symbol | | Test Conditions | | Min | Typ (Note 3) | Max | Units |
|---|---|---|---|---|---|---|---|
| $I_{PU/PD}$ | All Ports | $V_{CC}$ = 0 to 1.5V | $V_I$ = 0 to 3.45V | | | 30 | µA |
| $I_{CC}$ | A or B Ports or C Port | $V_{CC}$ = 3.45V | Outputs HIGH | | | 11 | mA |
| | | $I_O$ = 0 | Outputs LOW | | | 11 | |
| | | $V_I = V_{CC}/V_{TT}$ or GND | Outputs Disabled | | | 11 | |
| $\Delta I_{CC}$ (Note 5) | A Port and Control Pins | $V_{CC}$ = 3.45V, A or Control Inputs at $V_{CC}$ or GND | One Input at $V_{CC}$ –0.6V | | | 2 | mA |
| $C_i$ | Control Pins and A Port | | $V_I = V_{CC}$ or 0 | | | 3 | pF |
| $C_O$ | C Port | | $V_I = V_{CC}$ or 0 | | | 5 | pF |
| $C_{I/O}$ | B Port | | $V_I = V_{TT}$ or 0 | | | 5.5 | pF |

**Note 3:** All typical values are at $V_{CC}$ = 3.3V and $T_A$ = 25°C.

**Note 4:** For conditions shown as Min, use the appropriate value specified under recommended operating conditions.

**Note 5:** This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

**Note:** GTLP $V_{REF}$ and $V_{TT}$ are specified to 2% tolerance since signal integrity and noise margin can be significantly degraded if these supplies are noisy. In addition, $V_{TT}$ and $R_{TERM}$ can be adjusted beyond the recommended operating to accommodate backplane impedances other than 50Ω, but must remain within the boundaries of the DC Absolute Maximum Ratings. Similarly, $V_{REF}$ can be adjusted to optimize noise margin.

## AC Electrical Characteristics

Over recommended range of supply voltage and operating free-air temperature, $V_{REF}$ = 1.0V (unless otherwise noted).

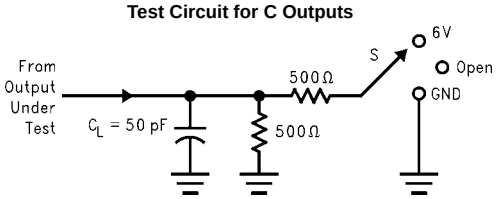
$C_L$ = 30 pF for B Port and $C_L$ = 50 pF for C Port.

| Symbol | From (Input) | To (Output) | Min | Typ (Note 6) | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | A | B | 1.2 | 3.2 | 7.3 | ns |
| $t_{PHL}$ | | | 0.8 | 2.3 | 4.5 | |
| $t_{PLH}$ | B | C | 1.4 | 2.8 | 4.4 | ns |
| $t_{PHL}$ | | | 1.6 | 2.9 | 5.0 | |
| $t_{PLH}$ | A | C | 1.6 | 6.0 | 8.1 | ns |
| $t_{PHL}$ | | | 2.0 | 5.1 | 7.5 | |
| $t_{RISE}$ | Transition Time, B Outputs (20% to 80%) | | | 1.4 | | ns |
| $t_{FALL}$ | Transition Time, B Outputs (80% to 20%) | | | 2.0 | | ns |
| $t_{RISE}$ | Transition Time, C Outputs (10% to 90%) | | | 2.8 | | ns |
| $t_{FALL}$ | Transition Time, C Outputs (90% to 10%) | | | 2.5 | | ns |
| $t_{PZH}$, $t_{PZL}$ | $\overline{OEC}$ | C | 1.2 | 2.7 | 5.3 | ns |
| $t_{PHZ}$, $t_{PLZ}$ | | | 1.4 | 2.8 | 4.9 | |
| $t_{PLH}$ | OEB | B | 1.7 | 3.5 | 5.9 | ns |
| $t_{PHL}$ | | | 0.5 | 2.2 | 4.7 | |

**Note 6:** All typical values are at $V_{CC}$ = 3.3V, and $T_A$ = 25°C.

## Test Circuits and Timing Waveforms

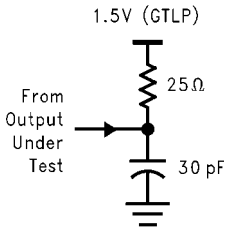
**Test Circuit for C Outputs**




| Test | S |
|---|---|
| $t_{PLH}/t_{PHL}$ | OPEN |
| $t_{PLZ}/t_{PZL}$ | 6V |
| $t_{PHZ}/t_{PZH}$ | GND |

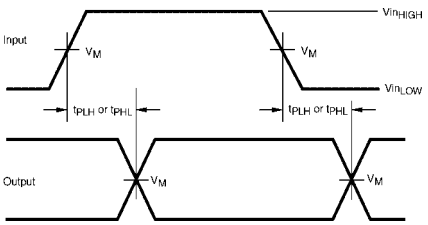
**Note:** $C_L$ includes probes and Jig capacitance.

**Test Circuit for B Outputs**

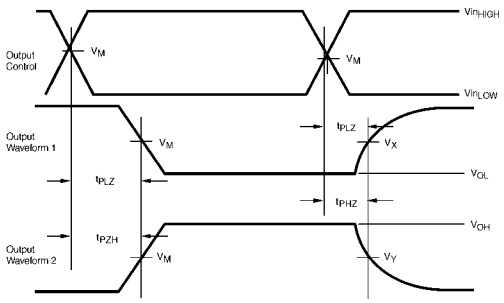



**Note:** $C_L$ includes probes and Jig capacitance.
**Note:** For B Port, $C_L$ = 30 pF is used for worst case.

**Voltage Waveforms Propagation Delay**



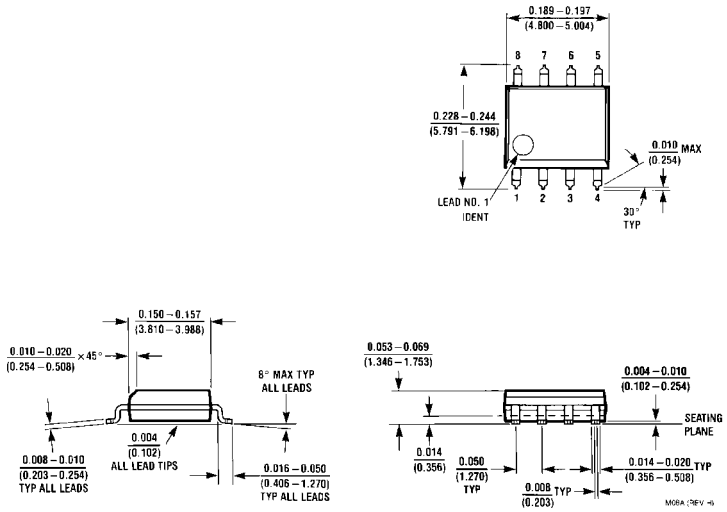

**Voltage Waveform Enable and Disable Times**




| | A or LVTTL Pins | B or GTLP Pins |
|---|---|---|
| $V_{INHIGH}$ | $V_{CC}$ | 1.5 |
| $V_{INLOW}$ | 0.0 | 0.0 |
| $V_M$ | $V_{CC}/2$ | 1.0 |
| $V_X$ | $V_{OL}$ + 0.3V | N/A |
| $V_Y$ | $V_{OH}$ − 0.3V | N/A |

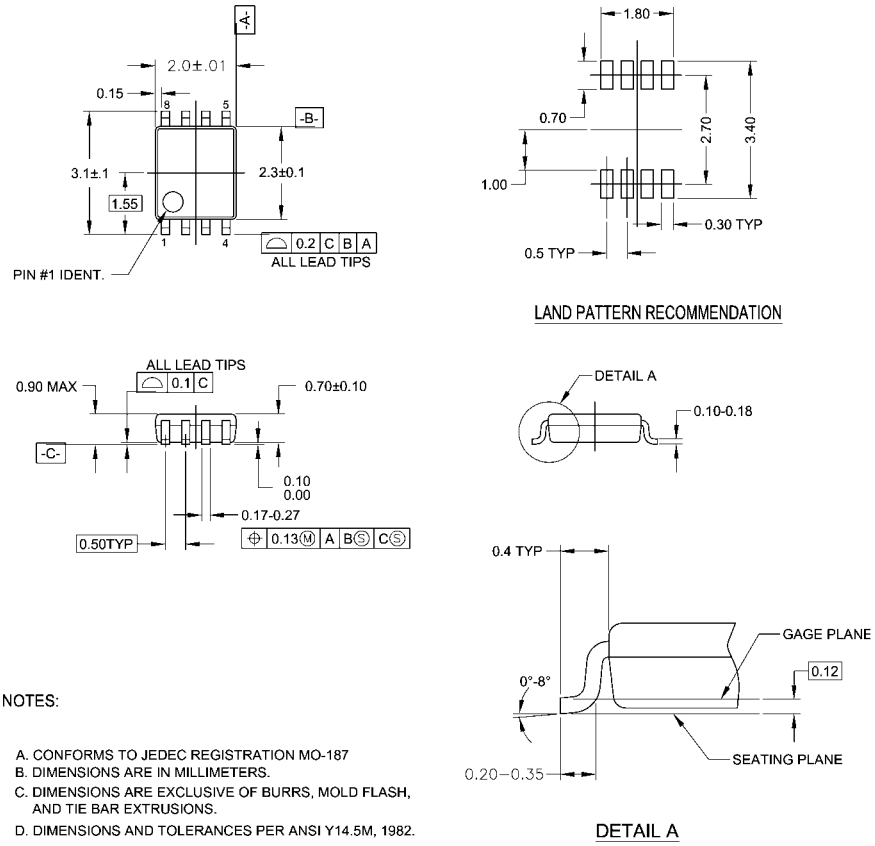
**Note:** Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.
**Note:** All input pulses have the following characteristics:
Frequency = 10MHz, $t_{RISE} = t_{FALL}$ = 2 ns (10% to 90%), $Z_O$ = 50Ω. The outputs are measured one at a time with one transition per measurement.

## Physical Dimensions inches (millimeters) unless otherwise noted




**8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow**
**Package Number M08A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-187
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MAB08AREVC

**8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide**
**Package Number MAB08A**
**Preliminary**



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