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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD
SEMICONDUCTOR™

November 1983
Revised April 2002

CD4051BC • CD4052BC • CD4053BC
Single 8-Channel Analog Multiplexer/Demultiplexer • Dual 4-Channel Analog Multiplexer/Demultiplexer • Triple 2-Channel Analog Multiplexer/Demultiplexer

General Description

The CD4051BC, CD4052BC, and CD4053BC analog multiplexers/demultiplexers are digitally controlled analog switches having low "ON" impedance and very low "OFF" leakage currents. Control of analog signals up to $15V_{p-p}$ can be achieved by digital signal amplitudes of 3–15V. For example, if $V_{DD} = 5V$, $V_{SS} = 0V$ and $V_{EE} = -5V$, analog signals from −5V to +5V can be controlled by digital inputs of 0–5V. The multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD}–V_{SS}$ and $V_{DD}–V_{EE}$ supply voltage ranges, independent of the logic state of the control signals. When a logical "1" is present at the inhibit input terminal all channels are "OFF".

CD4051BC is a single 8-channel multiplexer having three binary control inputs. A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned "ON" and connect the input to the output.

CD4052BC is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 or 4 pairs of channels to be turned on and connect the differential analog inputs to the differential outputs.

CD4053BC is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

Features

- Wide range of digital and analog signal levels: digital 3 – 15V, analog to $15V_{p-p}$
- Low "ON" resistance: 80Ω (typ.) over entire $15V_{p-p}$ signal-input range for $V_{DD} - V_{EE} = 15V$
- High "OFF" resistance: channel leakage of ±10 pA (typ.) at $V_{DD} - V_{EE} = 10V$
- Logic level conversion for digital addressing signals of 3 – 15V ($V_{DD} - V_{SS} = 3 - 15V$) to switch analog signals to 15 V_{p-p} ($V_{DD} - V_{EE} = 15V$)
- Matched switch characteristics: $\Delta R_{ON} = 5\Omega$ (typ.) for $V_{DD} - V_{EE} = 15V$
- Very low quiescent power dissipation under all digital-control input and supply conditions: 1 µ W (typ.) at $V_{DD} - V_{SS} = V_{DD} - V_{EE} = 10V$
- Binary address decoding on chip

Ordering Code:

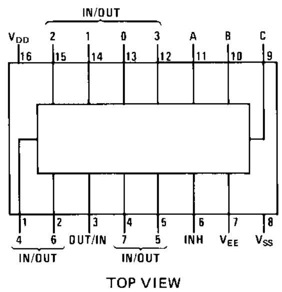
Order Number	Package Number	Package Description
CD4051BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4051BCSJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
CD4051BCMTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
CD4051BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
CD4052BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4052BCSJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
CD4052BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
CD4053BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4053BCSJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
CD4053BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

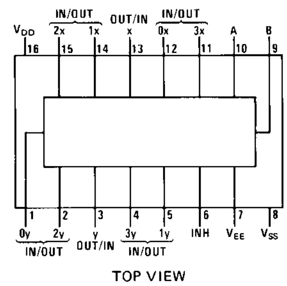
Connection Diagrams

Pin Assignments for DIP and SOIC

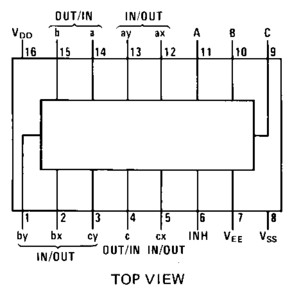
CD4051BC



CD4052BC



CD4053BC



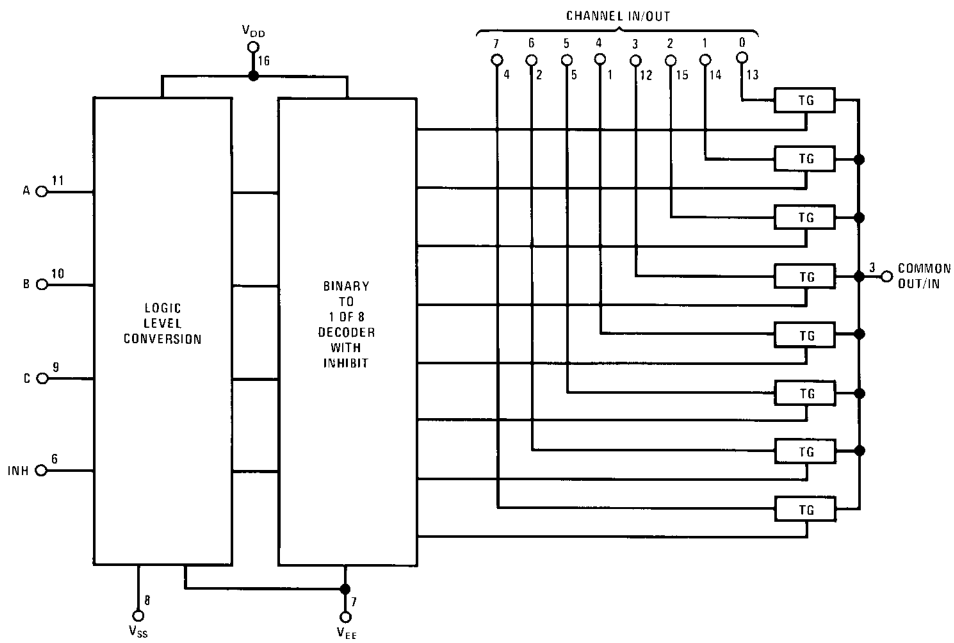
Truth Table

INPUT STATES				"ON" CHANNELS		
INHIBIT	C	B	A	CD4051B	CD4052B	CD4053B
0	0	0	0	0	0X, 0Y	cx, bx, ax
0	0	0	1	1	1X, 1Y	cx, bx, ay
0	0	1	0	2	2X, 2Y	cx, by, ax
0	0	1	1	3	3X, 3Y	cx, by, ay
0	1	0	0	4		cy, bx, ax
0	1	0	1	5		cy, bx, ay
0	1	1	0	6		cy, by, ax
0	1	1	1	7		cy, by, ay
1	*	*	*	NONE	NONE	NONE

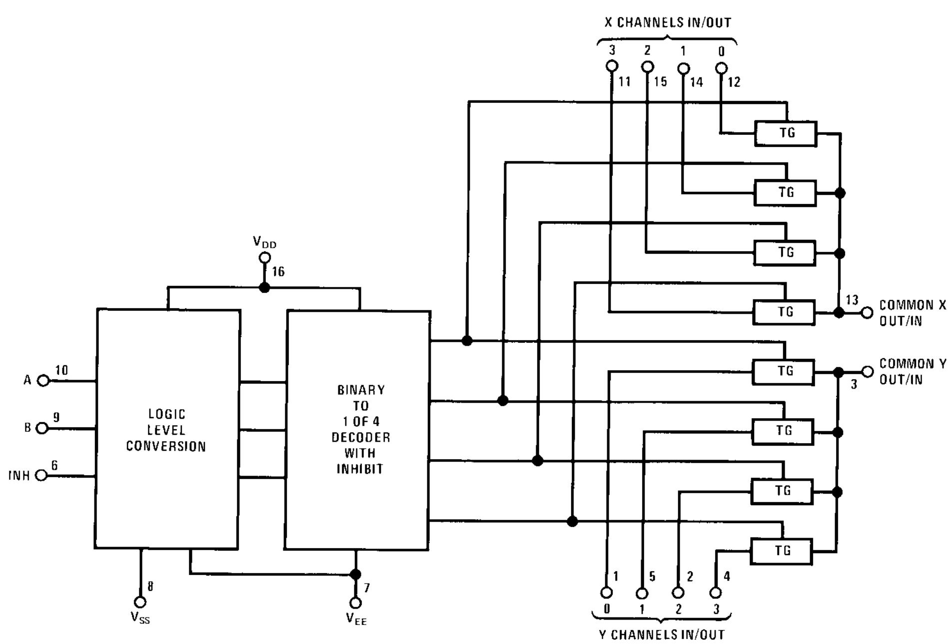
*Don't Care condition.

Logic Diagrams

CD4051BC

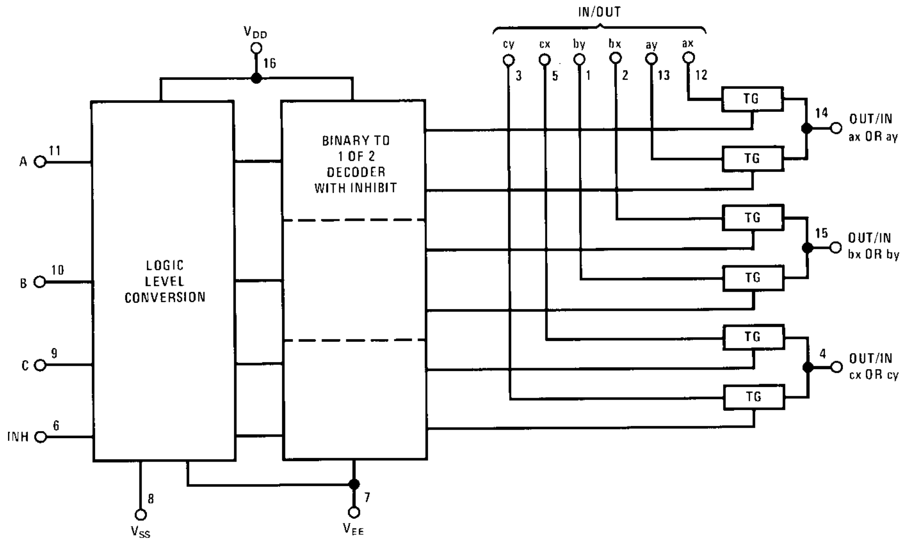


CD4052BC



Logic Diagrams (Continued)

CD4053BC



Absolute Maximum Ratings (Note 1)

DC Supply Voltage (V_{DD})	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
Input Voltage (V_{IN})	$-0.5\ V_{DC}$ to V_{DD} $+0.5\ V_{DC}$
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (soldering, 10 seconds)	260°C

Recommended Operating Conditions

DC Supply Voltage (V_{DD})	$+5\ V_{DC}$ to $+15\ V_{DC}$
Input Voltage (V_{IN})	0V to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
CD4051BC/CD4052BC/CD4053BC	−55°C to +125°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics tables provide conditions for actual device operation.

DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions		−55°C		+25°			125°C		Units
				Min	Max	Min	Typ	Max	Min	Max	
Control A, B, C and Inhibit											
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$	$V_{EE} = 0V$		−0.1		-10^{-5}	−0.1		−1.0	µA
		$V_{DD} = 15V$, $V_{IN} = 15V$	$V_{EE} = 0V$		0.1		10^{-5}	0.1		1.0	µA
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$			5			5		150	µA
		$V_{DD} = 10V$			10			10		300	µA
		$V_{DD} = 15V$			20			20		600	µA
Signal Inputs (V_{IS}) and Outputs (V_{OS})											
R_{ON}	"ON" Resistance (Peak for $V_{EE} \le V_{IS} \le V_{DD}$)	$R_L = 10\ k\Omega$ (any channel selected)	$V_{DD} = 2.5V$, $V_{EE} = -2.5V$ or $V_{DD} = 5V$, $V_{EE} = 0V$		800		270	1050		1300	Ω
			$V_{DD} = 5V$, $V_{EE} = -5V$ or $V_{DD} = 10V$, $V_{EE} = 0V$		310		120	400		550	Ω
			$V_{DD} = 7.5V$, $V_{EE} = -7.5V$ or $V_{DD} = 15V$, $V_{EE} = 0V$		200		80	240		320	Ω
ΔR_{ON}	Δ "ON" Resistance Between Any Two Channels	$R_L = 10\ k\Omega$ (any channel selected)	$V_{DD} = 2.5V$, $V_{EE} = -2.5V$ or $V_{DD} = 5V$, $V_{EE} = 0V$				10				Ω
			$V_{DD} = 5V$ $V_{EE} = -5V$ or $V_{DD} = 10V$, $V_{EE} = 0V$				10				Ω
			$V_{DD} = 7.5V$, $V_{EE} = -7.5V$ or $V_{DD} = 15V$, $V_{EE} = 0V$				5				Ω
	"OFF" Channel Leakage Current, any channel "OFF"	V_{DD}=7.5V, O/I=±7.5V, I/O=0V	V_{EE}=−7.5V		±50		±0.01	±50		±500	nA
	"OFF" Channel Leakage Current, all channels "OFF" (Common OUT/IN)	Inhibit = 7.5V	CD4051		±200		±0.08	±200		±2000	nA
		$V_{DD} = 7.5V$, $V_{EE} = -7.5V$, O/I = 0V	D4052		±200		±0.04	±200		±2000	nA
		I/O = ±7.5V	CD4053		±200		±0.02	±200		±2000	nA

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	−55°C		+25°			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
Control Inputs A, B, C and Inhibit										
V_{IL}	LOW Level Input Voltage	$V_{EE} = V_{SS}$ $R_L = 1\ k\Omega$ to V_{SS}								
		I_{IS}<2 µA on all OFF Channels								
		$V_{IS} = V_{DD}$ thru 1 kΩ								
		$V_{DD} = 5V$		1.5			1.5		1.5	
		$V_{DD} = 10V$		3.0			3.0		3.0	V
		$V_{DD} = 15V$		4.0			4.0		4.0	
V_{IH}	HIGH Level Input Voltage	$V_{DD} = 5$	3.5		3.5			3.5		
		$V_{DD} = 10$	7		7			7		V
		$V_{DD} = 15$	11		11			11		

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

AC Electrical Characteristics (Note 3)

$T_A = 25°C$, $t_r = t_f = 20$ ns, unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	Min	Typ	Max	Units
t_{PZH},	Propagation Delay Time from	$V_{EE} = V_{SS} = 0V$	5V		600	1200	
t_{PZL}	Inhibit to Signal Output	$R_L = 1$ kΩ	10V		225	450	ns
	(channel turning on)	$C_L = 50$ pF	15V		160	320	
t_{PHZ},	Propagation Delay Time from	$V_{EE} = V_{SS} = 0V$	5V		210	420	
t_{PLZ}	Inhibit to Signal Output	$R_L = 1$ kΩ	10V		100	200	ns
	(channel turning off)	$C_L = 50$ pF	15V		75	150	
C_{IN}	Input Capacitance						
	Control input				5	7.5	pF
	Signal Input (IN/OUT)				10	15	
C_{OUT}	Output Capacitance						
	(common OUT/IN)						
	CD4051		10V		30		
	CD4052	$V_{EE} = V_{SS} = 0V$	10V		15		pF
	CD4053		10V		8		
C_{IOS}	Feedthrough Capacitance				0.2		pF
C_{PD}	Power Dissipation Capacitance						
	CD4051				110		
	CD4052				140		pF
	CD4053				70		
Signal Inputs (V_{IS}) and Outputs (V_{OS})							
	Sine Wave Response	$R_L = 10$ kΩ					
	(Distortion)	$f_{IS} = 1$ kHz	10V		0.04		%
		$V_{IS} = 5\ V_{p\text{-}p}$					
		$V_{EE} = V_{SI} = 0V$					
	Frequency Response, Channel	$R_L = 1$ kΩ, $V_{EE} = 0V$, $V_{IS} = 5V_{p\text{-}p}$,	10V		40		MHz
	“ON” (Sine Wave Input)	$20 \log_{10} V_{OS}/V_{IS} = -3$ dB					
	Feedthrough, Channel “OFF”	$R_L = 1$ kΩ, $V_{EE} = V_{SS} = 0V$, $V_{IS} = 5V_{p\text{-}p}$,	10V		10		MHz
		$20 \log_{10} V_{OS}/V_{IS} = -40$ dB					
	Crosstalk Between Any Two	$R_L = 1$ kΩ, $V_{EE} = V_{SS} = 0V$, $V_{IS}(A) = 5V_{p\text{-}p}$	10V		3		MHz
	Channels (frequency at 40 dB)	$20 \log_{10} V_{OS}(B)/V_{IS}(A) = -40$ dB (Note 4)					
t_{PHL}	Propagation Delay Signal	$V_{EE} = V_{SS} = 0V$	5V		25	55	
t_{PLH}	Input to Signal Output	$C_L = 50$ pF	10V		15	35	ns
			15V		10	25	
Control Inputs, A, B, C and Inhibit							
	Control Input to Signal	$V_{EE} = V_{SS} = 0V$, $R_L = 10$ kΩ at both ends					
	Crosstalk	of channel.	10V		65		mV (peak)
		Input Square Wave Amplitude = 10V					
t_{PHL},	Propagation Delay Time from	$V_{EE} = V_{SS} = 0V$	5V		500	1000	
t_{PLH}	Address to Signal Output	$C_L = 50$ pF	10V		180	360	ns
	(channels “ON” or “OFF”)		15V		120	240	

Note 3: AC Parameters are guaranteed by DC correlated testing.

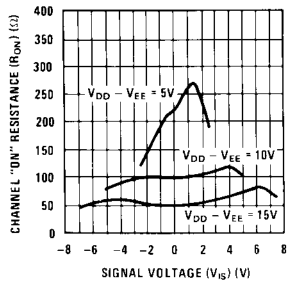
Note 4: A, B are two arbitrary channels with A turned “ON” and B “OFF”.

Special Considerations

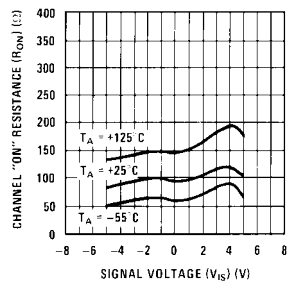
In certain applications the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into IN/OUT pin, the voltage drop across the bidirectional switch must not exceed 0.6V at $T_A \leq 25°C$, or 0.4V at $T_A > 25°C$ (calculated from R_{ON} values shown). No V_{DD} current will flow through R_L if the switch current flows into OUT/IN pin.

Typical Performance Characteristics

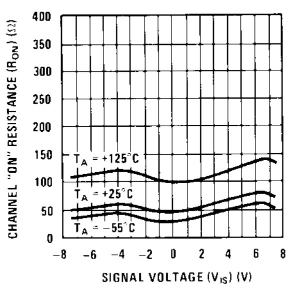
"ON" Resistance vs Signal Voltage for $T_A = 25°C$



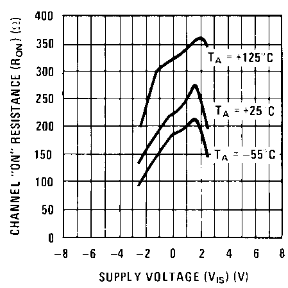
"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 10V$



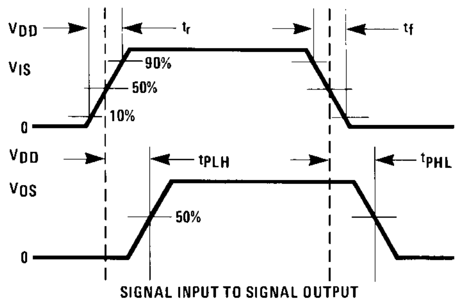
"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 15V$

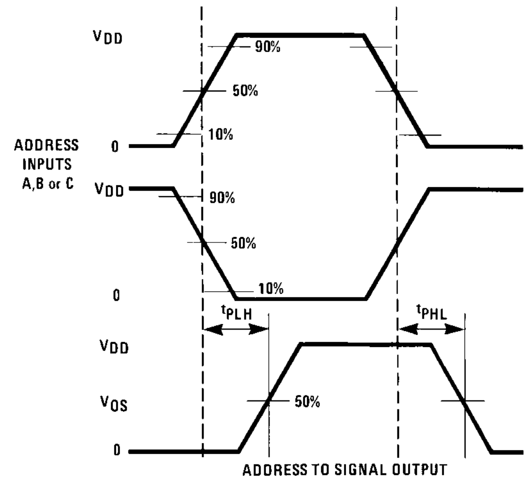


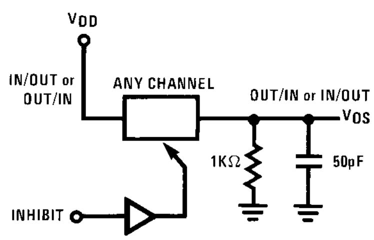
"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 5V$

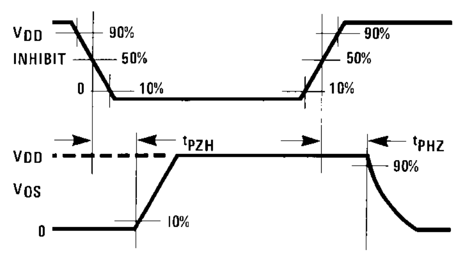


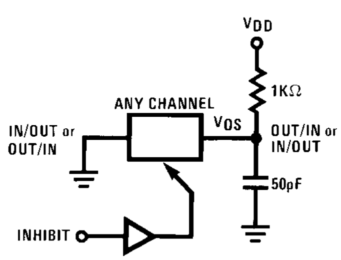
Switching Time Waveforms

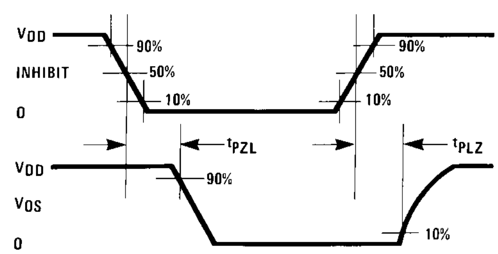




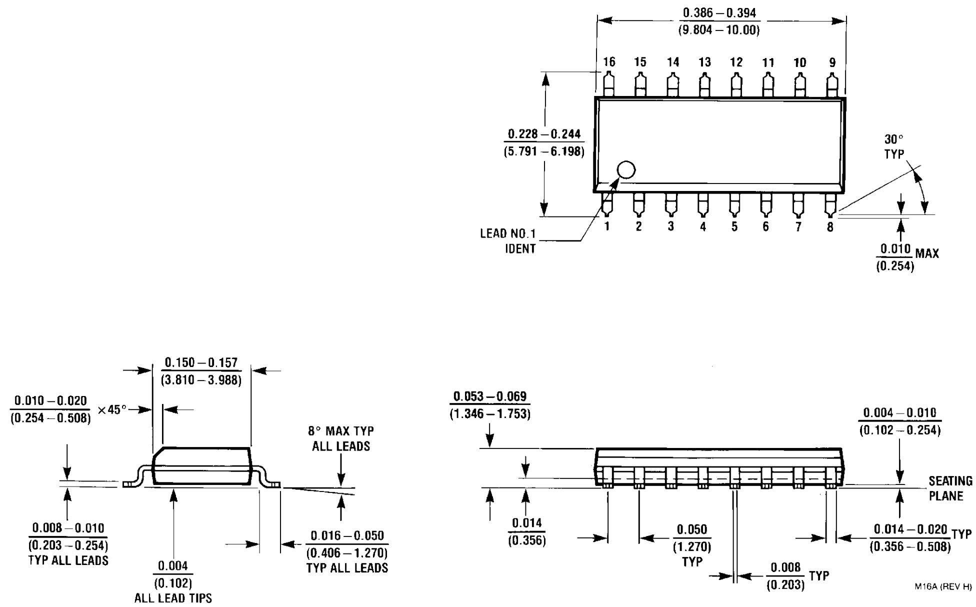






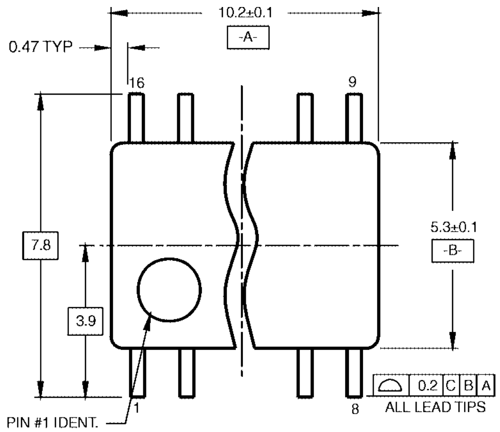


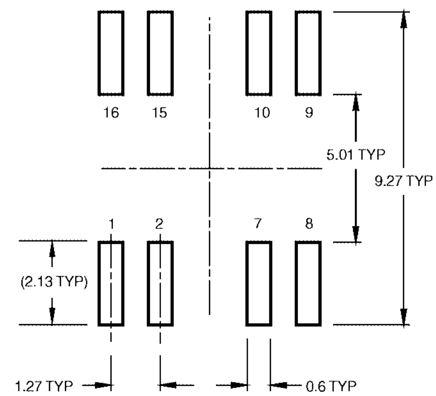
Physical Dimensions inches (millimeters) unless otherwise noted



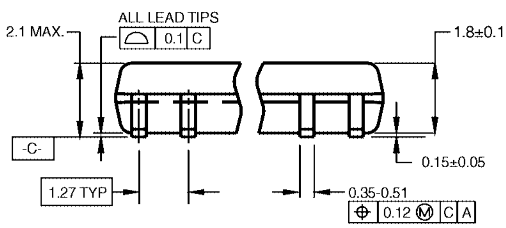
16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A

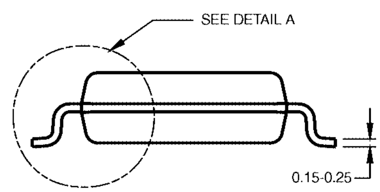
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)





LAND PATTERN RECOMMENDATION





DIMENSIONS ARE IN MILLIMETERS

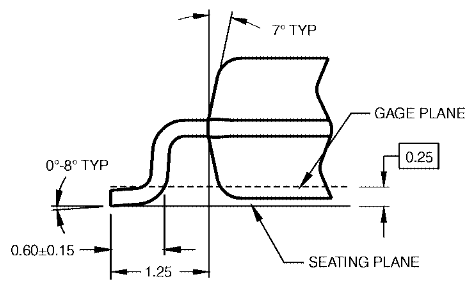
NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

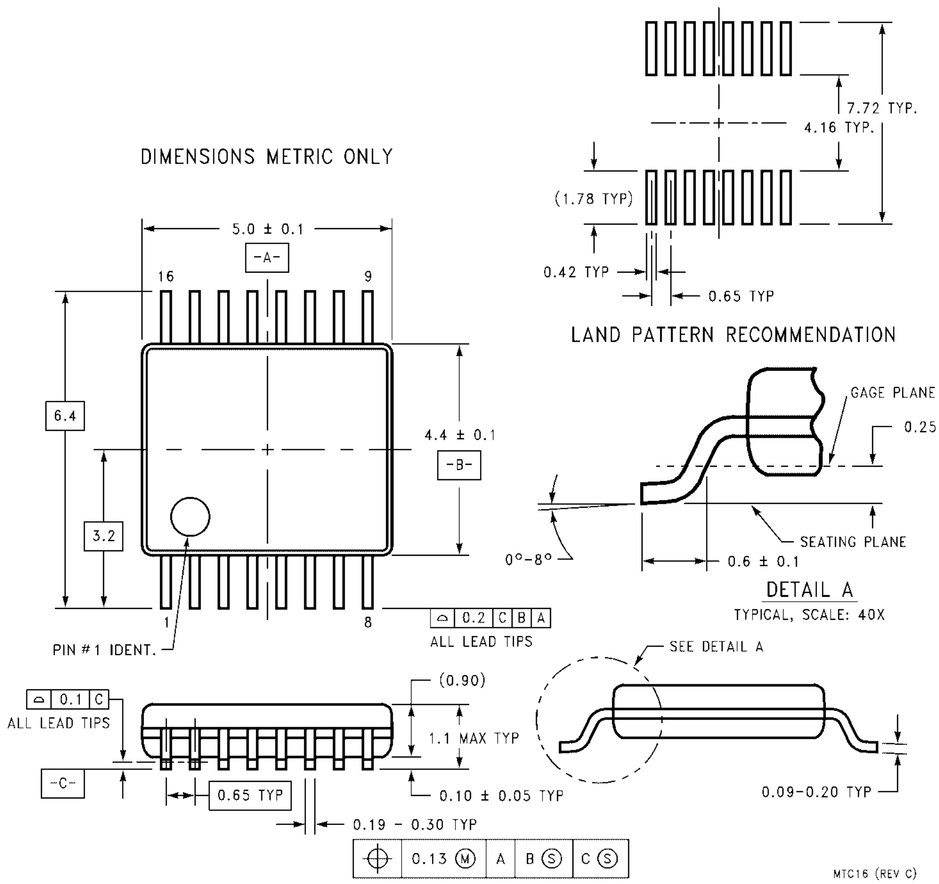
M16DRevB1



DETAIL A

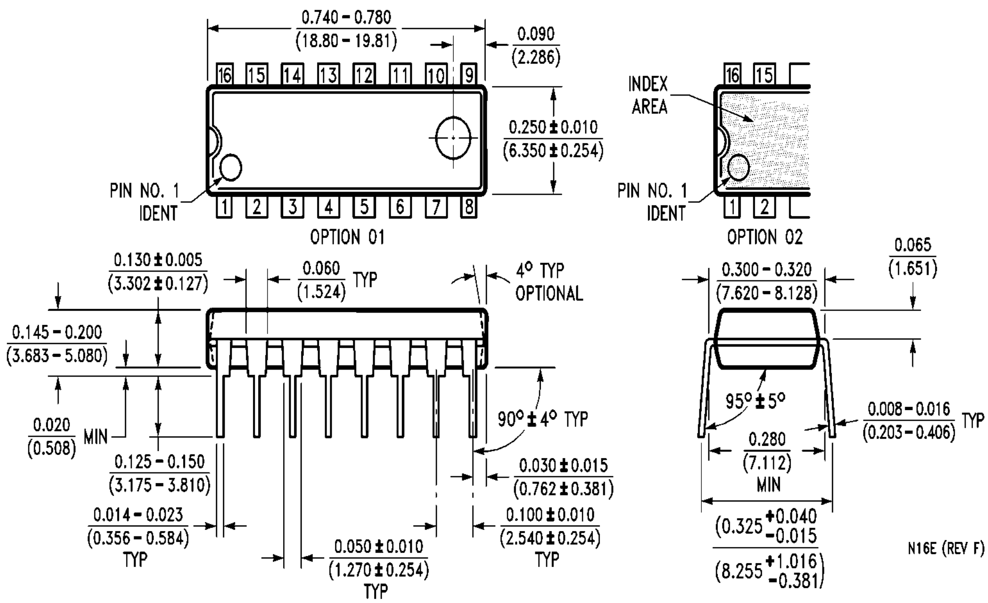
16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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