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NB3V8312C

Ultra-Low Jitter, Low Skew 1:12 LVCMOS/LVTTL Fanout Buffer

The NB3V8312C is a high performance, low skew LVCMOS fanout buffer which can distribute 12 ultra-low jitter clocks from an LVCMOS/LVTTL input up to 250 MHz.

The 12 LVCMOS output pins drive 50 Ω series or parallel terminated transmission lines. The outputs can also be disabled to a high impedance (tri-stated) via the OE input, or enabled when High.

The NB3V8312C provides an enable input, CLK_EN pin, which synchronously enables or disables the clock outputs while in the LOW state. Since this input is internally synchronized to the input clock, changing only when the input is LOW, potential output glitching or runt pulse generation is eliminated.

Separate V_{DD} core and V_{DDO} output supplies allow the output buffers to operate at the same supply as the V_{DD} ($V_{DD} = V_{DDO}$) or from a lower supply voltage. Compared to single-supply operation, dual supply operation enables lower power consumption and output-level compatibility.

The V_{DD} core supply voltage can be set to 3.3 V, 2.5 V or 1.8 V, while the V_{DDO} output supply voltage can be set to 3.3 V, 2.5 V, or 1.8 V, with the constraint that $V_{DD} \geq V_{DDO}$.

This buffer is ideally suited for various networking, telecom, server and storage area networking, RRU LO reference distribution, medical and test equipment applications.

Features

- Power Supply Modes:
 V_{DD} (Core) / V_{DDO} (Outputs)
3.3 V / 3.3 V
3.3 V / 2.5 V
3.3 V / 1.8 V
2.5 V / 2.5 V
2.5 V / 1.8 V
1.8 V / 1.8 V
- 250 MHz Maximum Clock Frequency
- Accepts LVCMOS, LVTTL Clock Inputs
- LVCMOS Compatible Control Inputs
- 12 LVCMOS Clock Outputs
- Synchronous Clock Enable
- Output Enable to High Z State Control
- 150 ps Max. Skew Between Outputs
- Temp. Range -40°C to $+85^{\circ}\text{C}$
- 32-pin LQFP and QFN Packages
- These are Pb-Free Devices

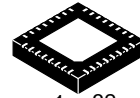


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LQFP-32
FA SUFFIX
CASE 873A



QFN32
MN SUFFIX
CASE 488AM

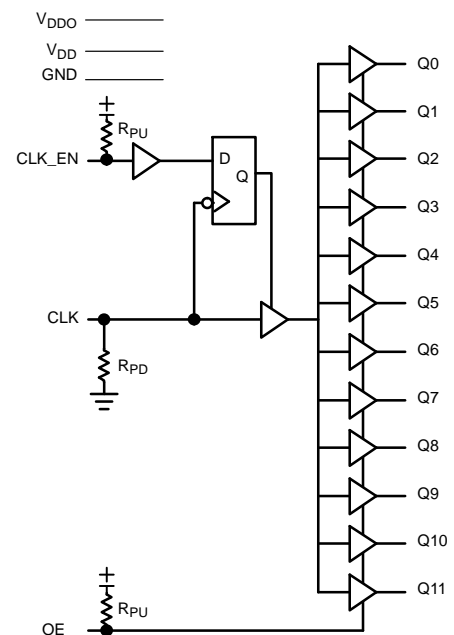


Figure 1. Simplified Logic Diagram

ORDERING AND MARKING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

Applications

- Networking
- Telecom
- Storage Area Network

End Products

- Servers
- Routers
- Switches

NB3V8312C

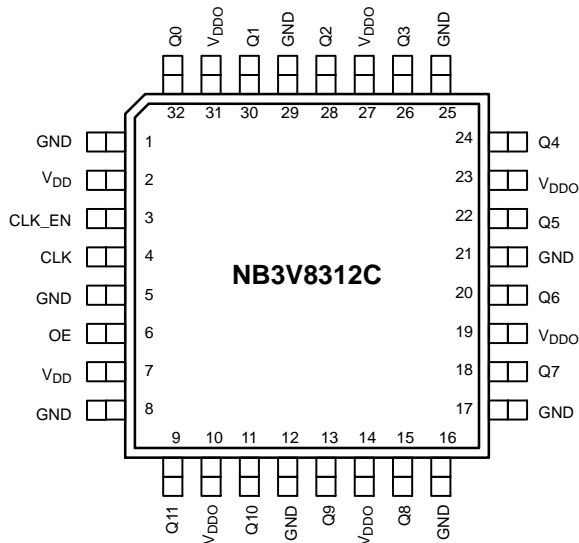


Figure 2. LQFP-32 Pinout Configuration
(Top View)

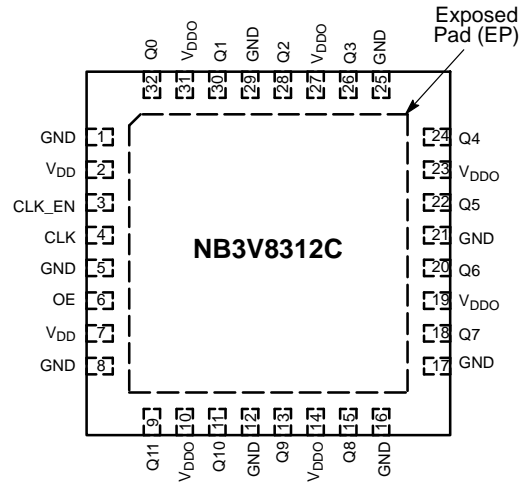


Figure 3. QFN32 Pinout Configuration
(Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Open Default	Description
1, 5, 8, 12, 16, 17, 21, 25, 29	GND	Power		Ground, Negative Power Supply
2, 7	VDD	Power		Positive Supply for Core and Inputs
3	CLK_EN	Input	High	Synchronous Clock Enable Input. When High, outputs are enabled. When Low, outputs are disabled Low. Internal Pullup Resistor.
4	CLK	Input	Low	Single-ended Clock input; LVCMOS/LVTTL. Internal Pull-down Resistor.
6	OE	Input	High	Output Enable. Internal Pullup Resistor.
9, 11, 13, 15, 18, 20, 22, 24, 26, 28, 30, 32	Q11, Q10, Q9, Q8, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0	Output		Single-ended LVCMOS/LVTTL outputs
10, 14, 19, 23, 27, 31	VDDO	Power		Positive Supply for Outputs
–	EP	–	–	The Exposed Pad (EP) on the package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is connected to the die and must only be connected electrically to GND on the PC board.

- All VDD, VDDO and GND pins must be externally connected to a power supply to guarantee proper operation. Bypass each supply pin with 0.01 μ F to GND.

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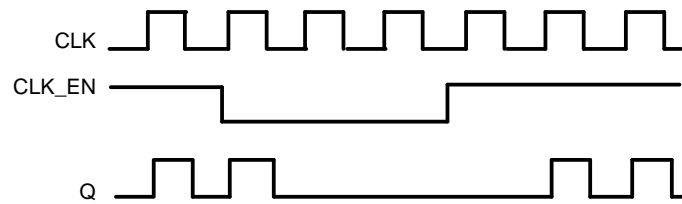


Figure 4. CLK_EN Control Timing Diagram

Table 2. OE, CLK_EN FUNCTION TABLES

Inputs			Outputs
OE	CLK_EN (Note 2)	CLK	Q[0:11]
0	X	X	Hi-Z
1	0	X	Low
1	1	0	Low
1	1	1	High

2. The CLK_EN control input synchronously enables or disables the outputs as shown in Figure 4. This control latches on the falling edge of the selected input CLK. When CLK_EN is LOW, the outputs are disabled in a LOW state. When CLK_EN is HIGH, the outputs are enabled as shown. CLK_EN to CLK Set up and Hold times must be satisfied.

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Table 3. ATTRIBUTES (Note 3)

Characteristics		Value
Internal Input Pullup (R_{PU}) and Pulldown (R_{PD}) Resistor		50 k Ω
Input Capacitance, C_{IN}		4 pF
Power Dissipation Capacitance, C_{PD} (per Output)		20 pF
R_{OUT}		8 Ω
ESD Protection	Human Body Model Machine Model	> 1.5 kV > 200 V
Moisture Sensitivity (Note 3)	LQFP QFN	Level 2 Level 1
Flammability Rating Oxygen Index		UL-94 code V-0 A 1/8" 28 to 34
Transistor Count		464 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

3. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS (Note 4)

Symbol	Parameter	Condition		Rating	Unit
V_{DD} / V_{DDO}	Positive Power Supply	GND = 0 V		4.6	V
V_I	Input Voltage			$-0.5 \leq V_I \leq V_{DD} + 0.5$	V
T_{stg}	Storage Temperature Range			-65 to +150	$^{\circ}\text{C}$
θ_{JA}	Thermal Resistance (Junction-to-Ambient) (Note 5)	0 lfpm 500 lfpm	LQFP-32 LQFP-32	80 55	$^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$
θ_{JC}	Thermal Resistance (Junction-to-Case) (Note 5)	Standard Board	LQFP-32 LQFP-32	12-17	$^{\circ}\text{C}/\text{W}$
θ_{JA}	Thermal Resistance (Junction-to-Ambient) (Note 5)	0 lfpm 500 lfpm	QFN-32 QFN-32	31 27	$^{\circ}\text{C}/\text{W}$
θ_{JC}	Thermal Resistance (Junction-to-Case) (Note 5)	Standard Board	QFN-32	12	$^{\circ}\text{C}/\text{W}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
- JEDEC standard multilayer board – 2S2P (2 signal, 2 power).

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Table 5. LVCMOS/LVTTL DC CHARACTERISTICS ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Symbol	Characteristics		Conditions	Min	Typ	Max	Unit
V_{IH}	Input High Voltage		$V_{DD} = 3.465\text{ V}$	2.0		$V_{DD} + 0.3$	V
			$V_{DD} = 2.625\text{ V}$	1.7		$V_{DD} + 0.3$	V
			$V_{DD} = 2.0\text{ V}$	$0.65 \times V_{DD}$		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		$V_{DD} = 3.465\text{ V}$	-0.3		1.3	V
			$V_{DD} = 2.625\text{ V}$	-0.3		0.7	V
			$V_{DD} = 2.0\text{ V}$	-0.3		$0.35 \times V_{DD}$	V
I_{IH}	Input High Current	CLK	$V_{DD} = V_{IN} = 3.465\text{ V}$ or 2.625 V or 2.0 V			150	μA
		OE, CLK_EN		5			
I_{IL}	Input Low Current	CLK	$V_{DD} = 3.465\text{ V}$ or 2.625 V or 2.0 V , $V_{IN} = 0\text{ V}$	-5			μA
		OE, CLK_EN		-150			
V_{OH}	Output High Voltage (Note 6)		$V_{DDO} = 3.3\text{ V} \pm 5\%$	2.6			V
			$V_{DDO} = 2.5\text{ V} \pm 5\%$	1.8			
			$V_{DDO} = 2.5\text{ V} \pm 5\%$; $I_{OH} = -1\text{ mA}$	2.0			
			$V_{DDO} = 1.8\text{ V} \pm 0.2\text{ V}$	$V_{DD} - 0.4$			
			$V_{DDO} = 1.8\text{ V} \pm 0.2\text{ V}$; $I_{OH} = -100\ \mu\text{A}$	$V_{DD} - 0.2$			
V_{OL}	Output Low Voltage (Note 6)		$V_{DDO} = 3.3\text{ V} \pm 5\%$			0.5	V
			$V_{DDO} = 2.5\text{ V} \pm 5\%$			0.45	
			$V_{DDO} = 2.5\text{ V} \pm 5\%$; $I_{OL} = 1\text{ mA}$			0.4	
			$V_{DDO} = 1.8\text{ V} \pm 0.2\text{ V}$			0.35	
			$V_{DDO} = 1.8\text{ V} \pm 0.2\text{ V}$; $I_{OL} = 100\ \mu\text{A}$			0.2	

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6. Outputs terminated $50\ \Omega$ to $V_{DDO}/2$ unless otherwise specified. See Figure 7.

Table 6. POWER SUPPLY DC CHARACTERISTICS, ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

V_{DD} (Core)	V_{DDO} (Outputs)	Min	Typ	Max	Unit
$3.3\text{ V} \pm 5\%$	$3.3\text{ V} \pm 5\%$			10	mA
$3.3\text{ V} \pm 5\%$	$2.5\text{ V} \pm 5\%$			10	mA
$3.3\text{ V} \pm 5\%$	$1.8\text{ V} \pm 0.2\text{ V}$			10	mA
$2.5\text{ V} \pm 5\%$	$2.5\text{ V} \pm 5\%$			10	mA
$2.5\text{ V} \pm 5\%$	$1.8\text{ V} \pm 0.2\text{ V}$			10	mA
$1.8\text{ V} \pm 0.2\text{ V}$	$1.8\text{ V} \pm 0.2\text{ V}$			10	mA

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Table 7. AC CHARACTERISTICS ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$) (Note 7)

Symbol	Characteristic	Min	Typ	Max	Unit
f_{MAX}	Maximum Operating Frequency $V_{\text{DD}} / V_{\text{DDO}}$ 3.3 V $\pm 5\%$ / 3.3 V $\pm 5\%$ 3.3 V $\pm 5\%$ / 2.5 V $\pm 5\%$ 3.3 V $\pm 5\%$ / 1.8 V ± 0.2 V 2.5 V $\pm 5\%$ / 2.5 V $\pm 5\%$ 2.5 V $\pm 5\%$ / 1.8 V ± 0.2 V 1.8 V ± 0.2 V / 1.8 V ± 0.2 V	250 250 200 250 200 200			MHz
t_{pLH}	Propagation Delay, Low to High; (Note 8) $V_{\text{DD}} / V_{\text{DDO}}$ 3.3 V $\pm 5\%$ / 3.3 V $\pm 5\%$ 3.3 V $\pm 5\%$ / 2.5 V $\pm 5\%$ 3.3 V $\pm 5\%$ / 1.8 V ± 0.2 V 2.5 V $\pm 5\%$ / 2.5 V $\pm 5\%$ 2.5 V $\pm 5\%$ / 1.8 V ± 0.2 V 1.8 V ± 0.2 V / 1.8 V ± 0.2 V	0.9 1.0 1.0 1.3 1.3 2.4		2.2 2.3 3.0 3.1 3.5 4.2	ns
t_{jit}	Additive Phase Jitter, RMS; $f_C = 100$ MHz Integration Range: 12 kHz – 20 MHz See Figure 5 $V_{\text{DD}} / V_{\text{DDO}}$ 3.3 V $\pm 5\%$ / 3.3 V $\pm 5\%$ 3.3 V $\pm 5\%$ / 2.5 V $\pm 5\%$ 3.3 V $\pm 5\%$ / 1.8 V ± 0.2 V 2.5 V $\pm 5\%$ / 2.5 V $\pm 5\%$ 2.5 V $\pm 5\%$ / 1.8 V ± 0.2 V 1.8 V ± 0.2 V / 1.8 V ± 0.2 V		30 40 50 20 100 130		fs
$t_{\text{sk(o)}}$	Output-to-output skew; (Note 9); Figure 6 $V_{\text{DD}} / V_{\text{DDO}}$ 3.3 V $\pm 5\%$ / 3.3 V $\pm 5\%$ 3.3 V $\pm 5\%$ / 2.5 V $\pm 5\%$ 3.3 V $\pm 5\%$ / 1.8 V ± 0.2 V 2.5 V $\pm 5\%$ / 2.5 V $\pm 5\%$ 2.5 V $\pm 5\%$ / 1.8 V ± 0.2 V 1.8 V ± 0.2 V / 1.8 V ± 0.2 V			125 135 145 150 150 140	ps
$t_{\text{sk(pp)}}$	Part-to-Part Skew; (Note 10) $V_{\text{DD}} / V_{\text{DDO}}$ 3.3 V $\pm 5\%$ / 3.3 V $\pm 5\%$ 3.3 V $\pm 5\%$ / 2.5 V $\pm 5\%$ 3.3 V $\pm 5\%$ / 1.8 V ± 0.2 V 2.5 V $\pm 5\%$ / 2.5 V $\pm 5\%$ 2.5 V $\pm 5\%$ / 1.8 V ± 0.2 V 1.8 V ± 0.2 V / 1.8 V ± 0.2 V			250 250 250 250 250 250	ps
t_r/t_f	Output rise and fall times $V_{\text{DD}} / V_{\text{DDO}}$ 3.3 V $\pm 5\%$ / 3.3 V $\pm 5\%$ 3.3 V $\pm 5\%$ / 2.5 V $\pm 5\%$ 3.3 V $\pm 5\%$ / 1.8 V ± 0.2 V 2.5 V $\pm 5\%$ / 2.5 V $\pm 5\%$ 2.5 V $\pm 5\%$ / 1.8 V ± 0.2 V 1.8 V ± 0.2 V / 1.8 V ± 0.2 V	200 200 200 200 200 200		700 700 700 700 700 800	ps
ODC	Output Duty Cycle (Note 11) $V_{\text{DD}} / V_{\text{DDO}}$ $f \leq 200$ MHz, 3.3 V $\pm 5\%$ / 3.3 V $\pm 5\%$ $f \leq 150$ MHz, 3.3 V $\pm 5\%$ / 2.5 V $\pm 5\%$ $f \leq 100$ MHz, 3.3 V $\pm 5\%$ / 1.8 V ± 0.2 V $f \leq 150$ MHz, 2.5 V $\pm 5\%$ / 2.5 V $\pm 5\%$ $f \leq 100$ MHz, 2.5 V $\pm 5\%$ / 1.8 V ± 0.2 V $f \leq 100$ MHz, 1.8 V ± 0.2 V / 1.8 V ± 0.2 V	45 45 45 45 45 45		55 55 55 55 55 55	%

All parameters measured at f_{MAX} unless noted otherwise.

7. Outputs loaded with 50 Ω to $V_{\text{DDO}}/2$; see Figure 7. CLOCK input with 50% duty cycle; minimum input amplitude = 1.2 V at $V_{\text{DD}} = 3.3$ V, 1.0 V at $V_{\text{DD}} = 2.5$ V, $V_{\text{DD}}/2$ at $V_{\text{DD}} = 1.8$ V.

8. Measured from the $V_{\text{DD}}/2$ of the input to $V_{\text{DDO}}/2$ of the output.

9. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{\text{DDO}}/2$.

10. Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions.

Using the same type of input on each device, the output is measured at $V_{\text{DDO}}/2$.

11. Clock input with 50% duty cycles, rail-to-rail amplitude and $t_r/t_f = 500$ ps.

NB3V8312C

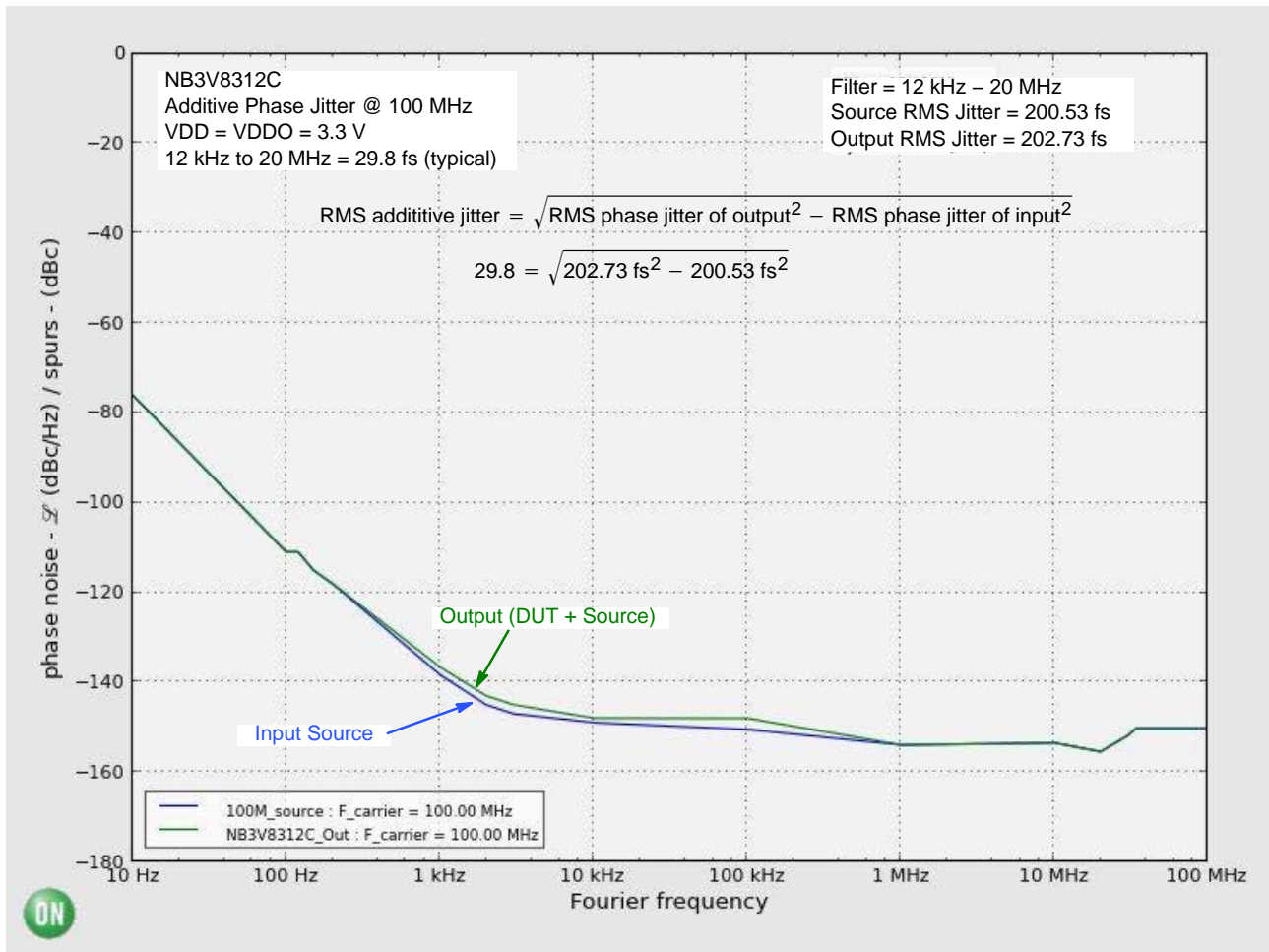


Figure 5. Typical Phase Noise Plot at $f_{\text{carrier}} = 100 \text{ MHz}$ at an Operating Voltage of 3.3 V, Room Temperature

The above phase noise data was captured using Agilent E5052A/B. The data displays the input phase noise and output phase noise used to calculate the additive phase jitter at a specified integration range. The RMS Phase Jitter contributed by the device (integrated between 12 kHz and 20 MHz) is 29.8 fs.

The additive phase jitter performance of the fanout buffer is highly dependent on the phase noise of the input source.

To obtain the most accurate additive phase noise measurement, it is vital that the source phase noise be

notably lower than that of the DUT. If the phase noise of the source is greater than the device under test output, the source noise will dominate the additive phase jitter calculation and lead to an artificially low result for the additive phase noise measurement within the integration range. The Figure above is a good example of the NB3V8312C source generator phase noise having a significantly higher floor such that the DUT output results in an additive phase jitter of 29.8 fs.

$$\text{RMS additive jitter} = \sqrt{\text{RMS phase jitter of output}^2 - \text{RMS phase jitter of input}^2}$$

$$29.8 = \sqrt{202.73 \text{ fs}^2 - 200.53 \text{ fs}^2}$$

NB3V8312C

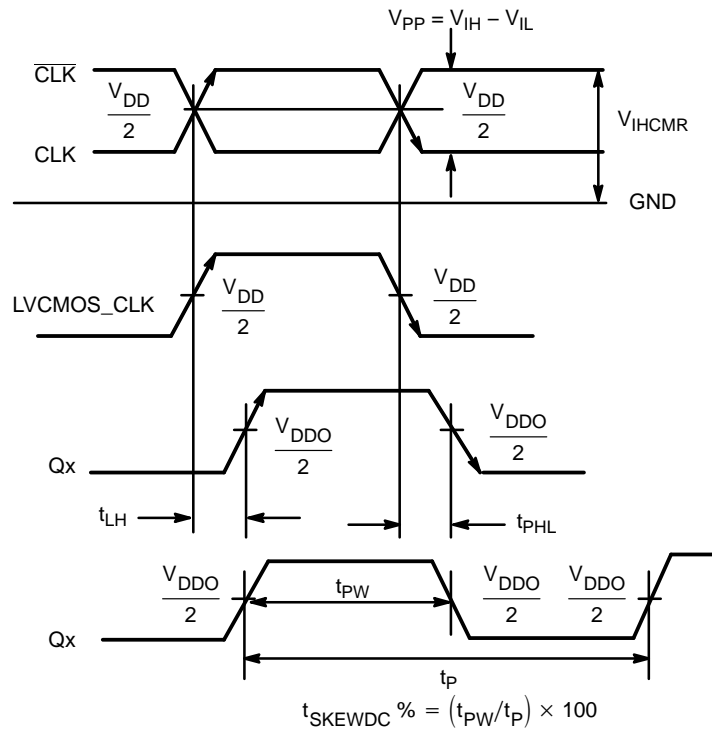


Figure 6. AC Reference Measurement

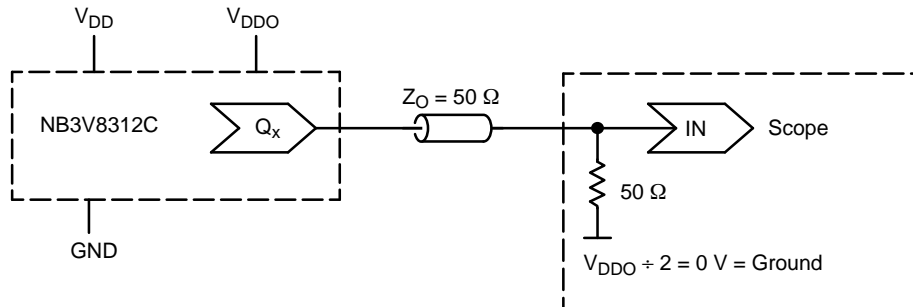


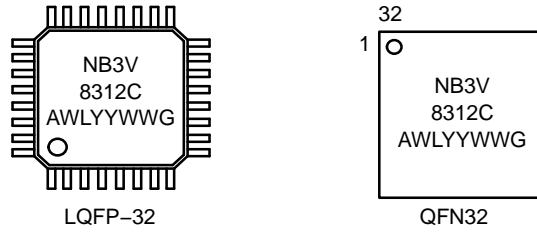
Figure 7. Typical Device Evaluation and Termination Setup – See Table 8

Table 8. TEST SUPPLY SETUP. V_{DDO} SUPPLY MAY BE CENTERED ON 0.0 V (SCOPE GND) TO PERMIT DIRECT CONNECTION INTO “50 Ω TO GND” SCOPE MODULE. V_{DD} SUPPLY TRACKS DUT GND PIN

Spec Condition:	V_{DD} Test Setup	V_{DDO} Test Setup	GND Pin Test Setup
$V_{DD} = 3.3 \text{ V} \pm 5\%$, $V_{DDO} = 3.3 \text{ V} \pm 5\%$	+1.65 $\pm 5\%$	+1.65 V $\pm 5\%$	-1.65 V $\pm 5\%$
$V_{DD} = 3.3 \text{ V} \pm 5\%$, $V_{DDO} = 2.5 \text{ V} \pm 5\%$	+2.05 V $\pm 5\%$	+1.25 V $\pm 5\%$	-1.25 V $\pm 5\%$
$V_{DD} = 3.3 \text{ V} \pm 5\%$, $V_{DDO} = 1.8 \text{ V} \pm 5\%$	+2.4 V $\pm 5\%$	+0.9 V $\pm 0.1 \text{ V}$	-0.9 V $\pm 0.1 \text{ V}$
$V_{DD} = 2.5 \text{ V} \pm 5\%$, $V_{DDO} = 2.5 \text{ V} \pm 5\%$	+1.25 V $\pm 5\%$	+1.25 V $\pm 5\%$	-1.25 V $\pm 5\%$
$V_{DD} = 2.5 \text{ V} \pm 5\%$, $V_{DDO} = 1.8 \text{ V} \pm 0.2 \text{ V}$	+1.6 V $\pm 5\%$	+0.9 V $\pm 0.1 \text{ V}$	-0.9 V $\pm 0.1 \text{ V}$
$V_{DD} = 1.8 \text{ V} \pm 0.2 \text{ V}$, $V_{DDO} = 1.8 \text{ V} \pm 0.2 \text{ V}$	+0.9 V $\pm 0.1 \text{ V}$	+0.9 V $\pm 0.1 \text{ V}$	-0.9 V $\pm 0.1 \text{ V}$

NB3V8312C

MARKING DIAGRAMS*



A = Assembly Location
 WL = Wafer Lot
 YY = Year
 WW = Work Week
 G = Pb-Free Package

(*Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

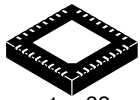
Device	Package	Shipping [†]
NB3V8312CFAG	LQFP-32 (Pb-Free)	250 Units / Tray
NB3V8312CFAR2G	LQFP-32 (Pb-Free)	2000 / Tape & Reel
NB3V8312CMNG	QFN32 (Pb-Free)	74 Units / Rail
NB3V8312CMNR4G	QFN32 (Pb-Free)	1000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

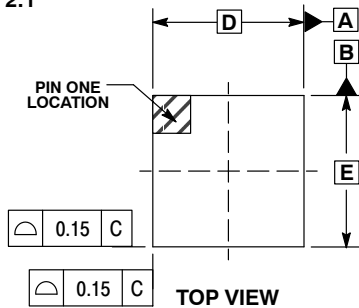


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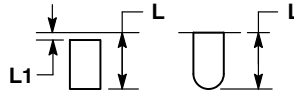
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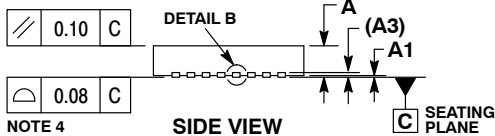
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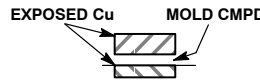
TOP VIEW



DETAIL A
ALTERNATE TERMINAL
CONSTRUCTIONS



SIDE VIEW



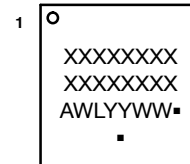
DETAIL B
ALTERNATE
CONSTRUCTION

NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20	REF
b	0.18	0.30
D	5.00	BSC
D2	2.95	3.25
E	5.00	BSC
E2	2.95	3.25
e	0.50	BSC
K	0.20	---
L	0.30	0.50
L1	---	0.15

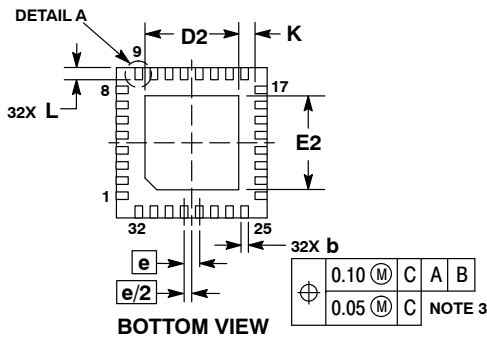
GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

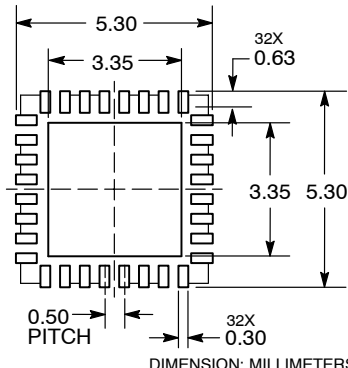


BOTTOM VIEW

⊕	0.10 (M)	C	A	B
	0.05 (M)	C		

NOTE 3

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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