

ON Semiconductor

Is Now

onsemi™

To learn more about onsemi™, please visit our website at
www.onsemi.com

onsemi and **onsemi** and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi** product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner. Other names and brands may be claimed as the property of others.

MC14536B

Programmable Timer

The MC14536B programmable timer is a 24-stage binary ripple counter with 16 stages selectable by a binary code. Provisions for an on-chip RC oscillator or an external clock are provided. An on-chip monostable circuit incorporating a pulse-type output has been included. By selecting the appropriate counter stage in conjunction with the appropriate input clock frequency, a variety of timing can be achieved.

Features

- 24 Flip-Flop Stages – Will Count From 2^0 to 2^{24}
- Last 16 Stages Selectable By Four-Bit Select Code
- 8-Bypass Input Allows Bypassing of First Eight Stages
- Set and Reset Inputs
- Clock Inhibit and Oscillator Inhibit Inputs
- On-Chip RC Oscillator Provisions
- On-Chip Monostable Output Provisions
- Clock Conditioning Circuit Permits Operation with Very Long Rise and Fall Times
- Test Mode Allows Fast Test Sequence
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	-0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	V_{in} , V_{out}	-0.5 to $V_{DD} + 0.5$	V
Input or Output Current (DC or Transient) per Pin	I_{in} , I_{out}	± 10	mA
Power Dissipation per Package (Note 1)	P_D	500	mW
Ambient Temperature Range	T_A	-55 to +125	$^{\circ}C$
Storage Temperature Range	T_{stg}	-65 to +150	$^{\circ}C$
Lead Temperature, (8-Second Soldering)	T_L	260	$^{\circ}C$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Packages: -7.0 mW/ $^{\circ}C$ from 65 $^{\circ}C$ to 125 $^{\circ}C$

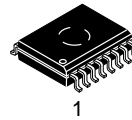
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

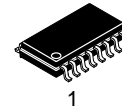


ON Semiconductor®

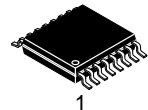
<http://onsemi.com>



SOIC-16 WB
DW SUFFIX
CASE 751G

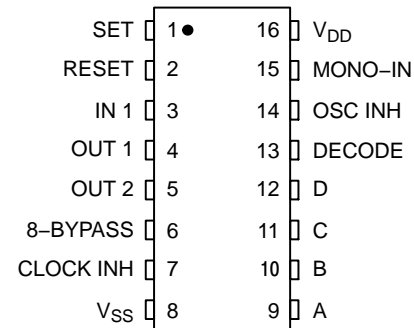


SOEIAJ-16
F SUFFIX
CASE 966

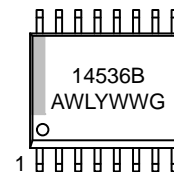


TSSOP-16
DT SUFFIX
CASE 948F

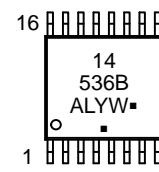
PIN ASSIGNMENT



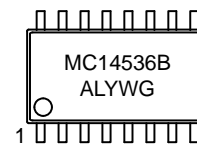
MARKING DIAGRAMS



SOIC-16 WB



TSSOP-16



SOEIAJ-16

- A = Assembly Location
- WL, L = Wafer Lot
- YY, Y = Year
- WW, W = Work Week
- G or ▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

MC14536B

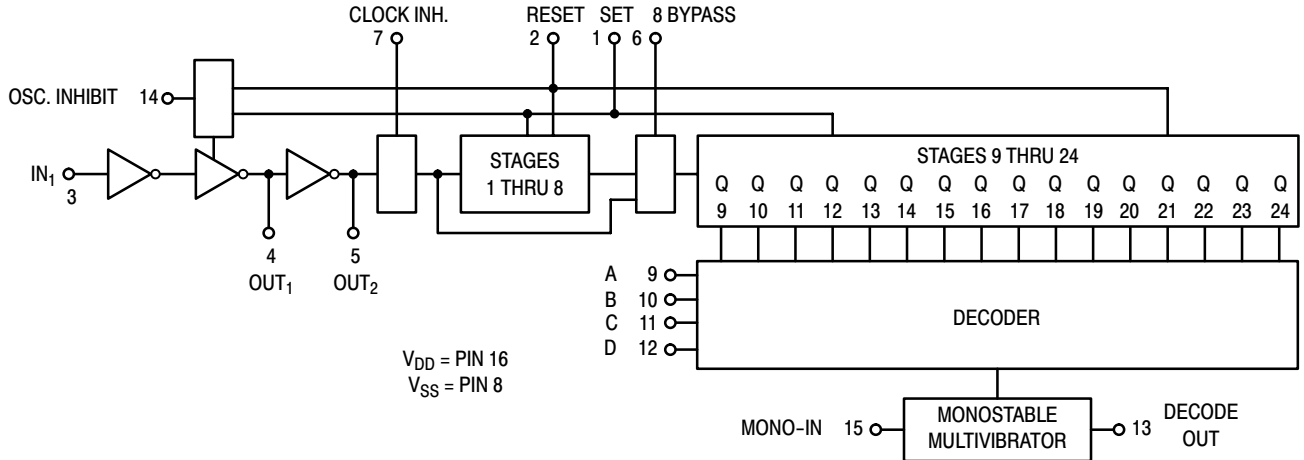


Figure 1. Block Diagram

FUNCTION TABLE

In ₁	Set	Reset	Clock Inh	OSC Inh	Out 1	Out 2	Decode Out
↗	0	0	0	0	↗	↘	No Change
↘	0	0	0	0	↘	↗	Advance to next state
X	1	0	0	0	0	1	1
X	0	1	0	0	0	1	0
X	0	0	1	0	-	-	No Change
X	0	0	0	1	0	1	No Change
0	0	0	0	X	0	1	No Change
1	0	0	0	↗	↘	↗	Advance to next state

X = Don't Care

MC14536B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	- 55°C		25°C			125°C		Unit		
			Min	Max	Min	Typ (Note 2)	Max	Min	Max			
Output Voltage V _{in} = V _{DD} or 0	"0" Level	V _{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc	
			10	–	0.05	–	0	0.05	–	0.05		
15			–	0.05	–	0	0.05	–	0.05			
V _{in} = 0 or V _{DD}	"1" Level	V _{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc	
			10	9.95	–	9.95	10	–	9.95	–		
			15	14.95	–	14.95	15	–	14.95	–		
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	"0" Level	V _{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc	
			10	–	3.0	–	4.50	3.0	–	3.0		
			15	–	4.0	–	6.75	4.0	–	4.0		
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	"1" Level	V _{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc	
			10	7.0	–	7.0	5.50	–	7.0	–		
			15	11	–	11	8.25	–	11	–		
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source Pins 4 & 5	I _{OH}	5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	mAdc	
			5.0	–0.25	–	–0.25	–0.36	–	–0.14	–		
			10	–0.62	–	–0.5	–0.9	–	–0.35	–		
			15	–1.8	–	–1.5	–3.5	–	–1.1	–		
	Source Pin 13	I _{OH}	5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mAdc	
			5.0	–0.64	–	–0.51	–0.88	–	–0.36	–		
			10	–1.6	–	–1.3	–2.25	–	–0.9	–		
			15	–4.2	–	–3.4	–8.8	–	–2.4	–		
	(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Sink	I _{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
				10	1.6	–	1.3	2.25	–	0.9	–	
				15	4.2	–	3.4	8.8	–	2.4	–	
	Input Current	I _{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc	
Input Capacitance (V _{in} = 0)	C _{in}	–	–	–	–	5.0	7.5	–	–	pF		
Quiescent Current (Per Package)	I _{DD}	5.0	–	5.0	–	0.010	5.0	–	150	μAdc		
		10	–	10	–	0.020	10	–	300			
		15	–	20	–	0.030	20	–	600			
Total Supply Current (Note 3, 4) (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.50 μA/kHz) f + I _{DD} I _T = (2.30 μA/kHz) f + I _{DD} I _T = (3.55 μA/kHz) f + I _{DD}						μAdc			
		10										
		15										

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.003.

MC14536B

SWITCHING CHARACTERISTICS (Note 5) ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD}	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time (Pin 13) $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH},$ t_{THL}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q1, 8–Bypass (Pin 6) High $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 1715 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 617 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 425 \text{ ns}$	$t_{PLH},$ t_{PHL}	5.0 10 15	– – –	1800 650 450	3600 1300 1000	ns
Clock to Q1, 8–Bypass (Pin 6) Low $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 3715 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 1467 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 1075 \text{ ns}$	$t_{PLH},$ t_{PHL}	5.0 10 15	– – –	3.8 1.5 1.1	7.6 3.0 2.3	μs
Clock to Q16 $t_{PHL}, t_{PLH} = (1.7 \text{ ns/pF}) C_L + 6915 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.66 \text{ ns/pF}) C_L + 2967 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.5 \text{ ns/pF}) C_L + 2175 \text{ ns}$	$t_{PLH},$ t_{PHL}	5.0 10 15	– – –	7.0 3.0 2.2	14 6.0 4.5	μs
Reset to Q_n $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 1415 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 567 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 425 \text{ ns}$	t_{PHL}	5.0 10 15	– – –	1500 600 450	3000 1200 900	ns
Clock Pulse Width	t_{WH}	5.0 10 15	600 200 170	300 100 85	– – –	ns
Clock Pulse Frequency (50% Duty Cycle)	f_{cl}	5.0 10 15	– – –	1.2 3.0 5.0	0.4 1.5 2.0	MHz
Clock Rise and Fall Time	$t_{TLH},$ t_{THL}	5.0 10 15	No Limit			–
Reset Pulse Width	t_{WH}	5.0 10 15	1000 400 300	500 200 150	– – –	ns

5. The formulas given are for the typical characteristics only at 25°C .

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

PIN DESCRIPTIONS

INPUTS

SET (Pin 1) – A high on Set asynchronously forces Decode Out to a high level. This is accomplished by setting an output conditioning latch to a high level while at the same time resetting the 24 flip–flop stages. After Set goes low (inactive), the occurrence of the first negative clock transition on IN₁ causes Decode Out to go low. The counter’s flip–flop stages begin counting on the second negative clock transition of IN₁. When Set is high, the on–chip RC oscillator is disabled. This allows for very low–power standby operation.

RESET (Pin 2) – A high on Reset asynchronously forces Decode Out to a low level; all 24 flip–flop stages are also reset to a low level. Like the Set input, Reset disables the on–chip RC oscillator for standby operation.

IN₁ (Pin 3) – The device’s internal counters advance on the negative–going edge of this input. IN₁ may be used as an external clock input or used in conjunction with OUT₁ and OUT₂ to form an RC oscillator. When an external clock is used, both OUT₁ and OUT₂ may be left unconnected or used to drive 1 LSTTL or several CMOS loads.

8–BYPASS (Pin 6) – A high on this input causes the first 8 flip–flop stages to be bypassed. This device essentially becomes a 16–stage counter with all 16 stages selectable. Selection is accomplished by the A, B, C, and D inputs. (See the truth tables.)

CLOCK INHIBIT (Pin 7) – A high on this input disconnects the first counter stage from the clocking source. This holds the present count and inhibits further counting. However, the clocking source may continue to run. Therefore, when Clock Inhibit is brought low, no oscillator startup time is required. When Clock Inhibit is low, the counter will start counting on the occurrence of the first negative edge of the clocking source at IN₁.

OSC INHIBIT (Pin 14) – A high level on this pin stops the RC oscillator which allows for very low–power standby operation. May also be used, in conjunction with an external clock, with essentially the same results as the Clock Inhibit input.

MONO–IN (Pin 15) – Used as the timing pin for the on–chip monostable multivibrator. If the Mono–In input is connected to V_{SS}, the monostable circuit is disabled, and Decode Out is directly connected to the selected Q output. The monostable circuit is enabled if a resistor is connected between Mono–In and V_{DD}. This resistor and the device’s internal capacitance will determine the minimum output pulse widths. With the addition of an external capacitor to V_{SS}, the pulse width range may be extended. For reliable operation the resistor value should be limited to the range of 5 kΩ to 100 kΩ and the capacitor value should be limited to a maximum of 1000 pf. (See figures 4, 5, 6, and 11).

A, B, C, D (Pins 9, 10, 11, 12) – These inputs select the flip–flop stage to be connected to Decode Out. (See the truth tables.)

OUTPUTS

OUT₁, OUT₂ (Pin 4, 5) – Outputs used in conjunction with IN₁ to form an RC oscillator. These outputs are buffered and may be used for 2⁰ frequency division of an external clock.

DECODE OUT (Pin 13) – Output function depends on configuration. When the monostable circuit is disabled, this output is a 50% duty cycle square wave during free run.

TEST MODE

The test mode configuration divides the 24 flip–flop stages into three 8–stage sections to facilitate a fast test sequence. The test mode is enabled when 8–Bypass, Set and Reset are at a high level. (See Figure 9.)

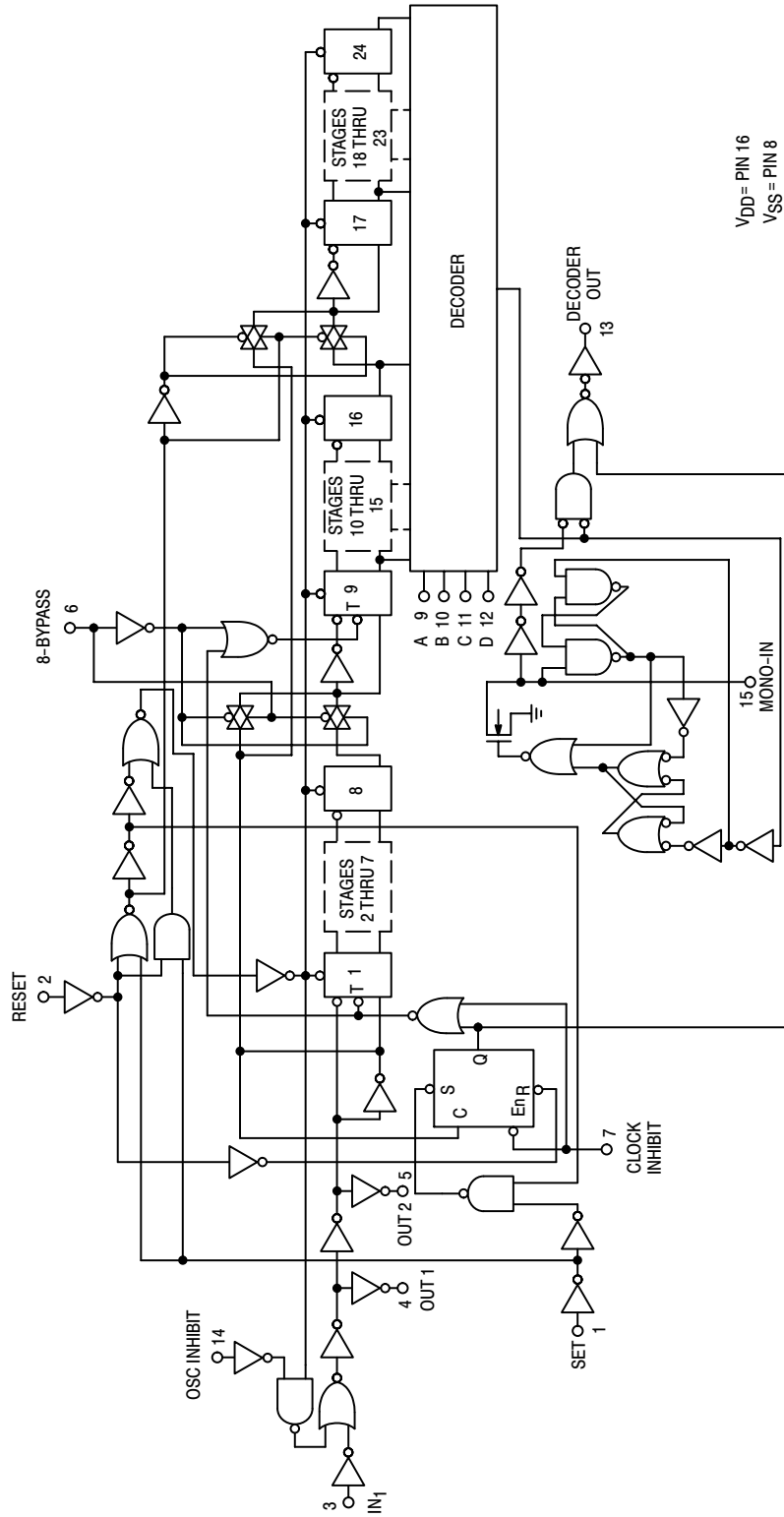
TRUTH TABLES

Input					Stage Selected for Decode Out
8–Bypass	D	C	B	A	
0	0	0	0	0	9
0	0	0	0	1	10
0	0	0	1	0	11
0	0	0	1	1	12
0	0	1	0	0	13
0	0	1	0	1	14
0	0	1	1	0	15
0	0	1	1	1	16
0	1	0	0	0	17
0	1	0	0	1	18
0	1	0	1	0	19
0	1	0	1	1	20
0	1	1	0	0	21
0	1	1	0	1	22
0	1	1	1	0	23
0	1	1	1	1	24

Input					Stage Selected for Decode Out
8–Bypass	D	C	B	A	
1	0	0	0	0	1
1	0	0	0	1	2
1	0	0	1	0	3
1	0	0	1	1	4
1	0	1	0	0	5
1	0	1	0	1	6
1	0	1	1	0	7
1	0	1	1	1	8
1	1	0	0	0	9
1	1	0	0	1	10
1	1	0	1	0	11
1	1	0	1	1	12
1	1	1	0	0	13
1	1	1	0	1	14
1	1	1	1	0	15
1	1	1	1	1	16

MC14536B

LOGIC DIAGRAM



TYPICAL RC OSCILLATOR CHARACTERISTICS
(For Circuit Diagram See Figure 12 In Application)

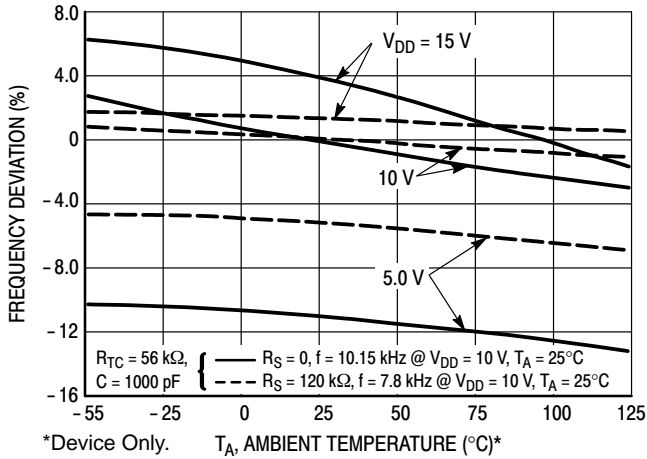


Figure 2. RC Oscillator Stability

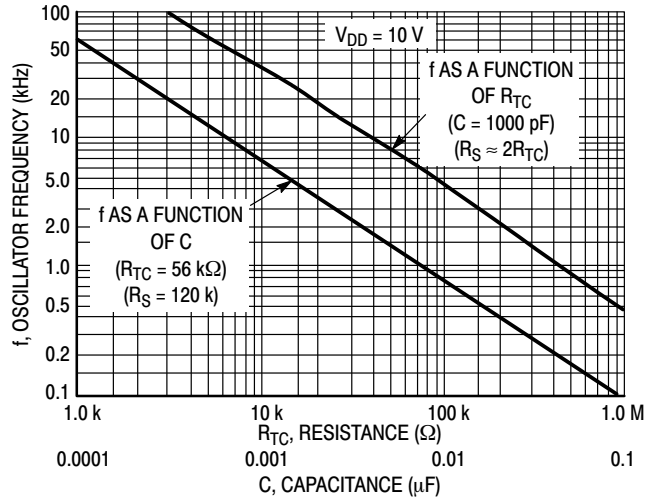


Figure 3. RC Oscillator Frequency as a Function of R_{TC} and C

MONOSTABLE CHARACTERISTICS
(For Circuit Diagram See Figure 11 In Application)

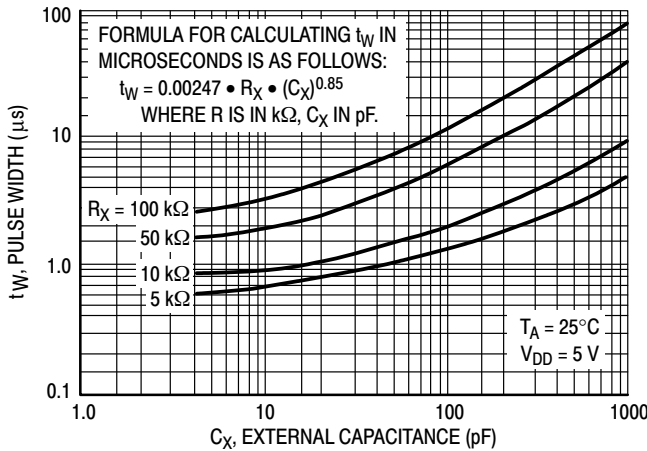


Figure 4. Typical C_X versus Pulse Width @ $V_{DD} = 5.0 \text{ V}$

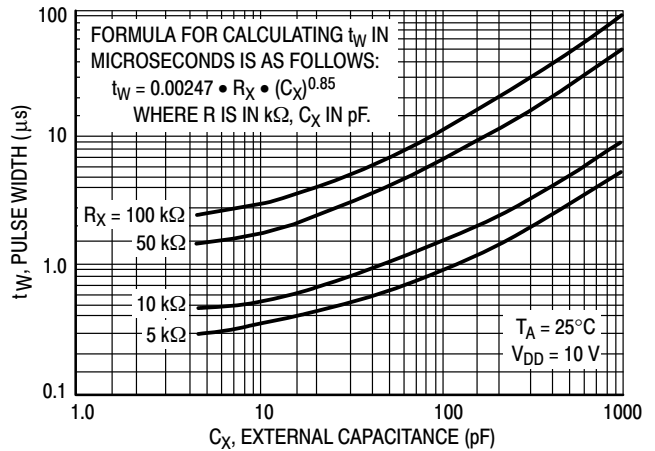


Figure 5. Typical C_X versus Pulse Width @ $V_{DD} = 10 \text{ V}$

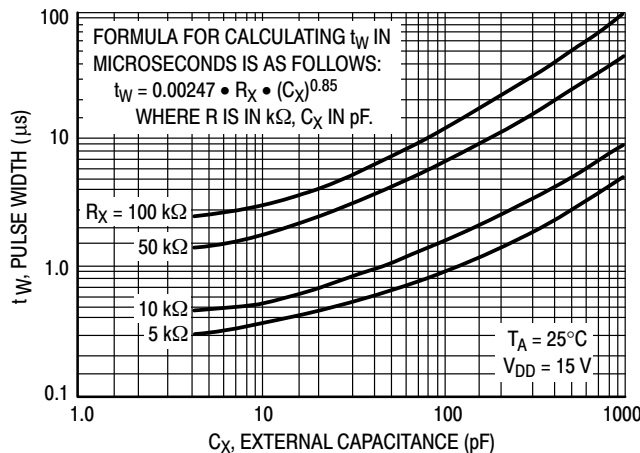


Figure 6. Typical C_X versus Pulse Width @ $V_{DD} = 15 \text{ V}$

MC14536B

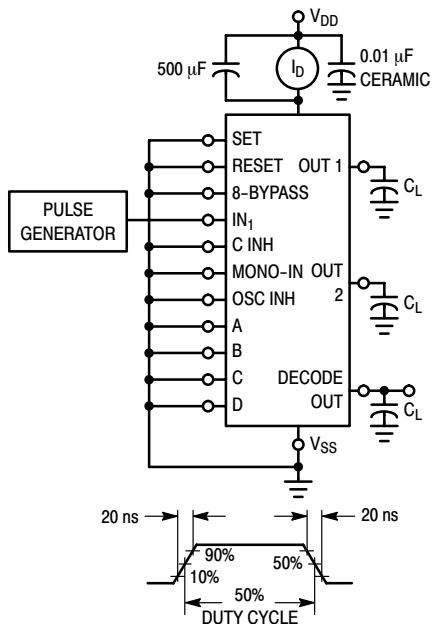


Figure 7. Power Dissipation Test Circuit and Waveform

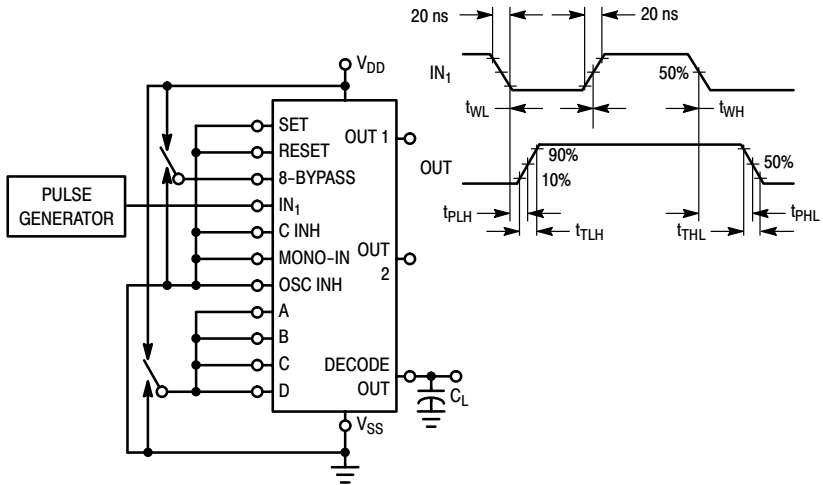


Figure 8. Switching Time Test Circuit and Waveforms

FUNCTIONAL TEST SEQUENCE

Test function (Figure 9) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flops are now at a "1". The counter is now returned to the normal 24-stages in series configuration. One more pulse is entered into In₁ which will cause the counter to ripple from an all "1" state to an all "0" state.

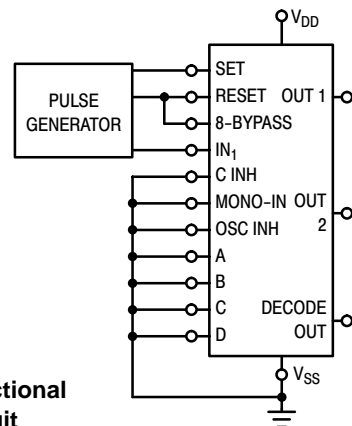
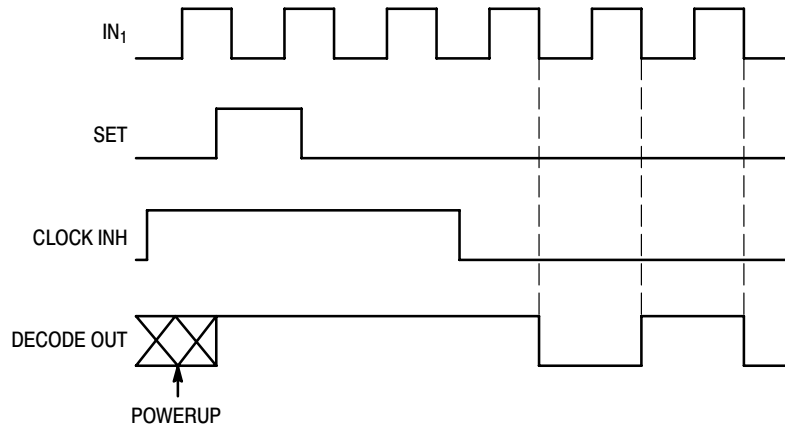
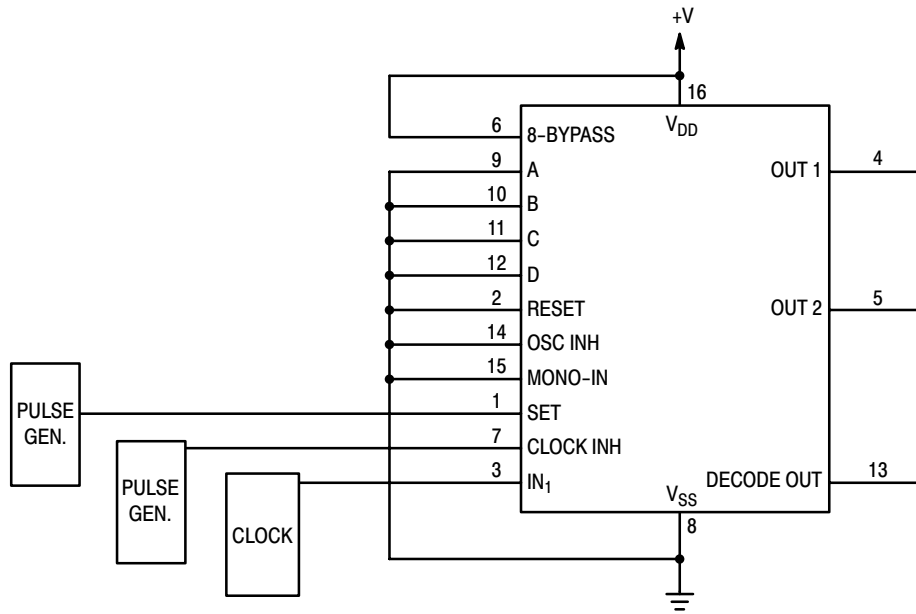


Figure 9. Functional Test Circuit

FUNCTIONAL TEST SEQUENCE

Inputs				Outputs	Comments
In ₁	Set	Reset	8-Bypass	Decade Out Q1 thru Q24	
1	0	1	1	0	All 24 stages are in Reset mode.
1	1	1	1	0	Counter is in three 8 stage sections in parallel mode.
0	1	1	1	0	First "1" to "0" transition of clock.
1 0 - -	1	1	1		255 "1" to "0" transitions are clocked in the counter.
0	1	1	1	1	The 255 "1" to "0" transition.
0	0	0	0	1	Counter converted back to 24 stages in series mode. Set and Reset must be connected together and simultaneously go from "1" to "0".
1	0	0	0	1	In ₁ Switches to a "1".
0	0	0	0	0	Counter Ripples from an all "1" state to an all "0" state.

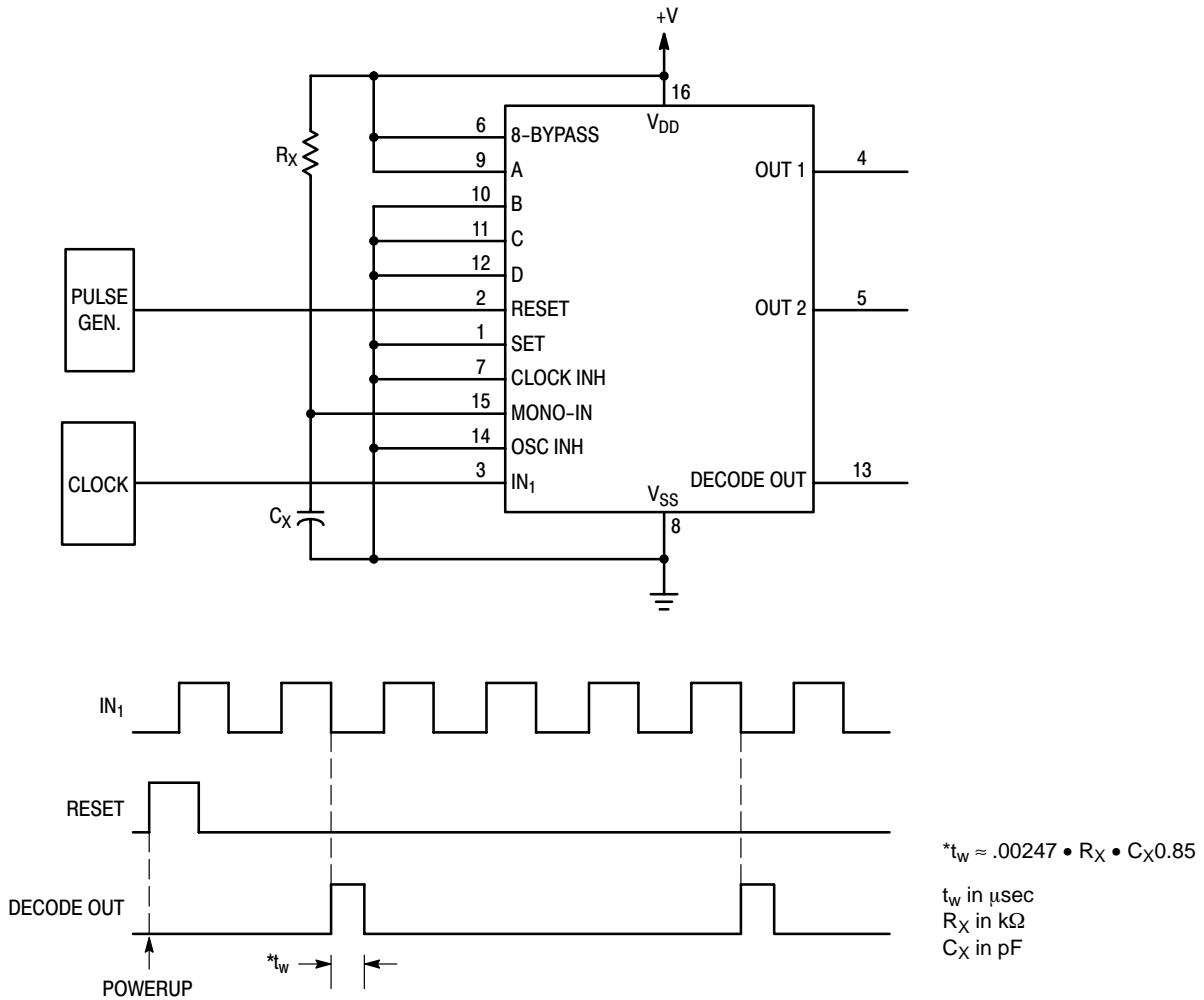
MC14536B



NOTE: When power is first applied to the device, DECODE OUT can be either at a high or low state. On the rising edge of a SET pulse the output goes high if initially at a low state. The output remains high if initially at a high state. Because CLOCK INH is held high, the clock source on the input pin has no effect on the output. Once CLOCK INH is taken low, the output goes low on the first negative clock transition. The output returns high depending on the 8-BYPASS, A, B, C, and D inputs, and the clock input period. A 2^n frequency division (where n = the number of stages selected from the truth table) is obtainable at DECODE OUT. A 2^0 -divided output of IN_1 can be obtained at OUT_1 and OUT_2 .

Figure 10. Time Interval Configuration Using an External Clock, Set, and Clock Inhibit Functions (Divide-by-2 Configured)

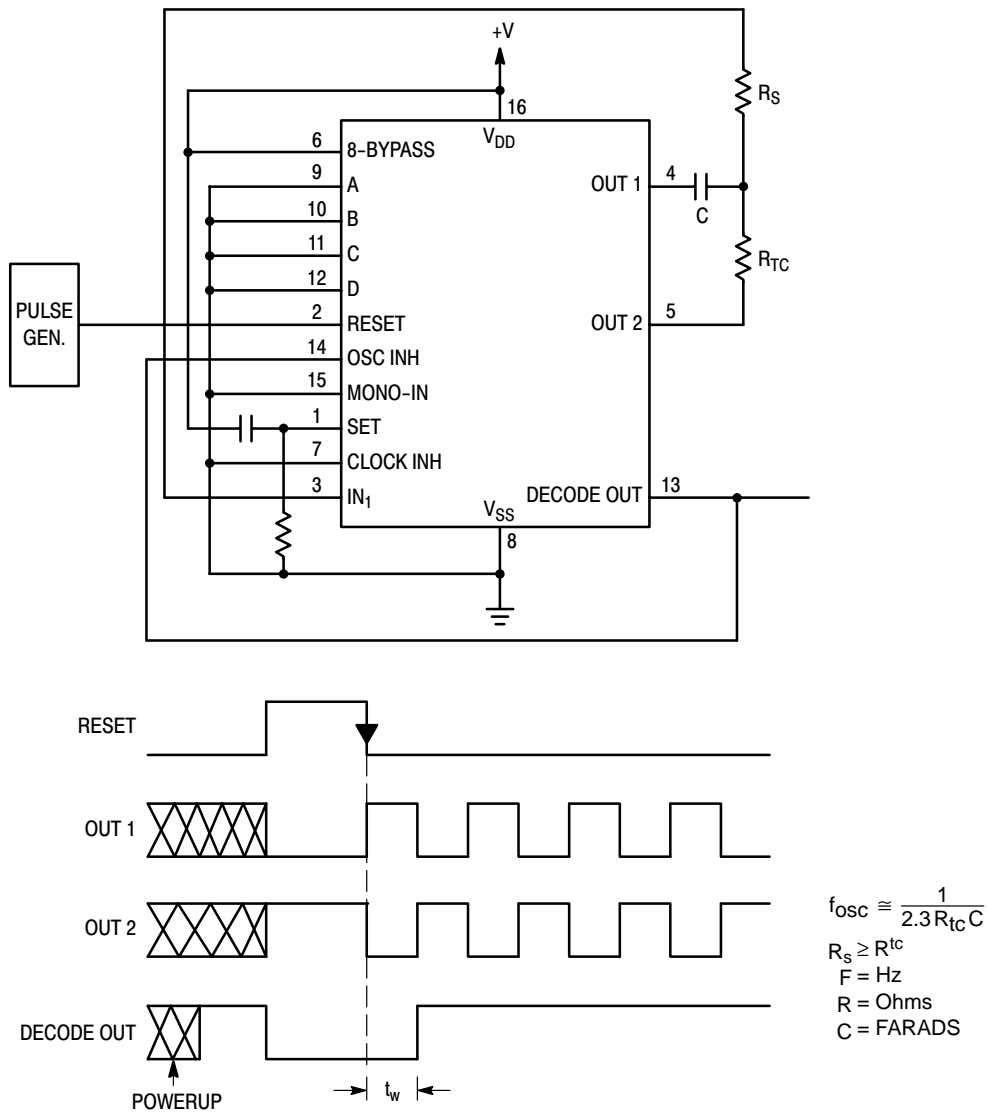
MC14536B



NOTE: When Power is first applied to the device with the RESET input going high, DECODE OUT initializes low. Bringing the RESET input low enables the chip's internal counters. After RESET goes low, the $2^{n/2}$ negative transition of the clock input causes DECODE OUT to go high. Since the MONO-IN input is being used, the output becomes monostable. The pulse width of the output is dependent on the external timing components. The second and all subsequent pulses occur at $2^n \times$ (the clock period) intervals where n = the number of stages selected from the truth table.

Figure 11. Time Interval Configuration Using an External Clock, Reset, and Output Monostable to Achieve a Pulse Output (Divide-by-4 Configured)

MC14536B



NOTE: This circuit is designed to use the on-chip oscillation function. The oscillator frequency is determined by the external R and C components. When power is first applied to the device, DECODE OUT initializes to a high state. Because this output is tied directly to the OSC INH input, the oscillator is disabled. This puts the device in a low-current standby condition. The rising edge of the RESET pulse will cause the output to go low. This in turn causes OSC INH to go low. However, while RESET is high, the oscillator is still disabled (i.e.: standby condition). After RESET goes low, the output remains low for $2^{1/2}$ of the oscillator's period. After the part times out, the output again goes high.

Figure 12. Time Interval Configuration Using On-Chip RC Oscillator and Reset Input to Initiate Time Interval (Divide-by-2 Configured)

MC14536B

ORDERING INFORMATION

Device	Package	Shipping [†]
MC14536BDWG	SOIC-16 WB (Pb-Free)	47 Units / Rail
NLV14536BDWG*	SOIC-16 WB (Pb-Free)	47 Units / Rail
MC14536BDWR2G	SOIC-16 WB (Pb-Free)	1000 / Tape & Reel
NLV14536BDWR2G*	SOIC-16 WB (Pb-Free)	1000 / Tape & Reel
NLV14536BDTR2G* (In Development)	TSSOP-16 (Pb-Free)	2500 / Tape & Reel
MC14536BFELG	SOEIAJ-16 (Pb-Free)	2000 / Tape & Reel

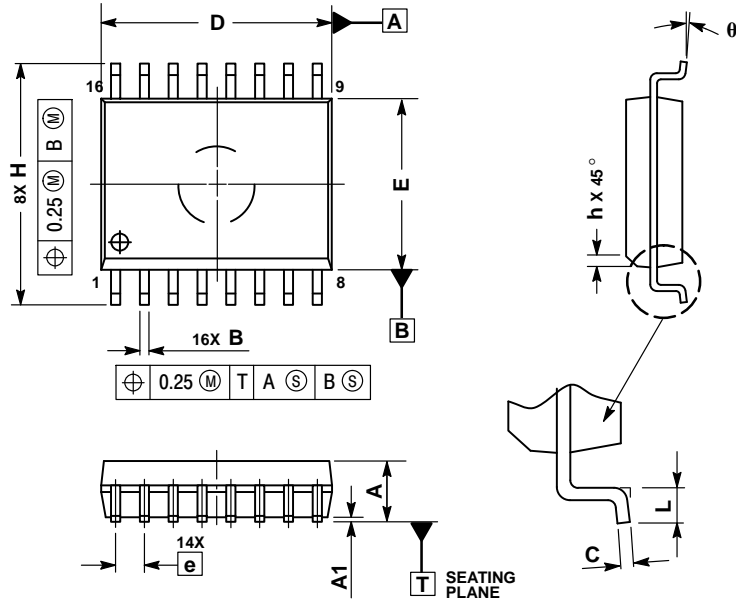
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

MC14536B

PACKAGE DIMENSIONS

SOIC-16 WB
CASE 751G-03
ISSUE D

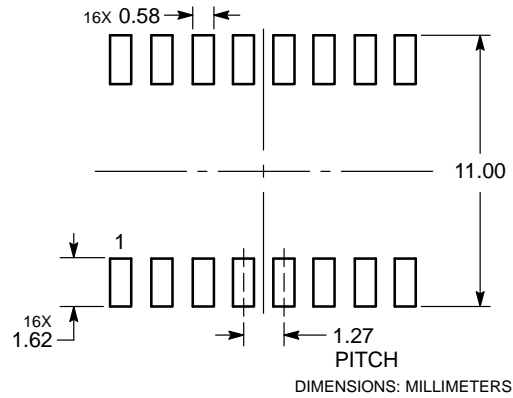


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
q	0 °	7 °

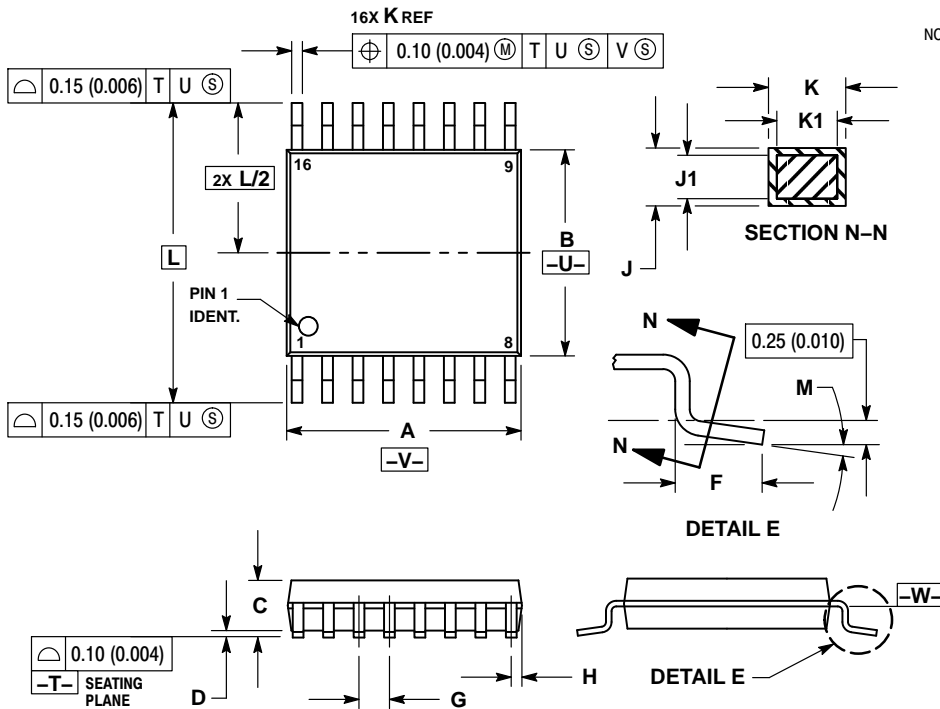
SOLDERING FOOTPRINT



MC14536B

PACKAGE DIMENSIONS

TSSOP-16
CASE 948F
ISSUE B

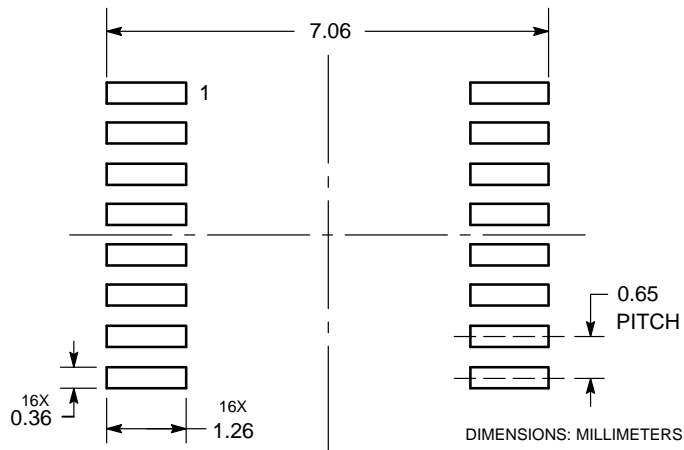


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT*

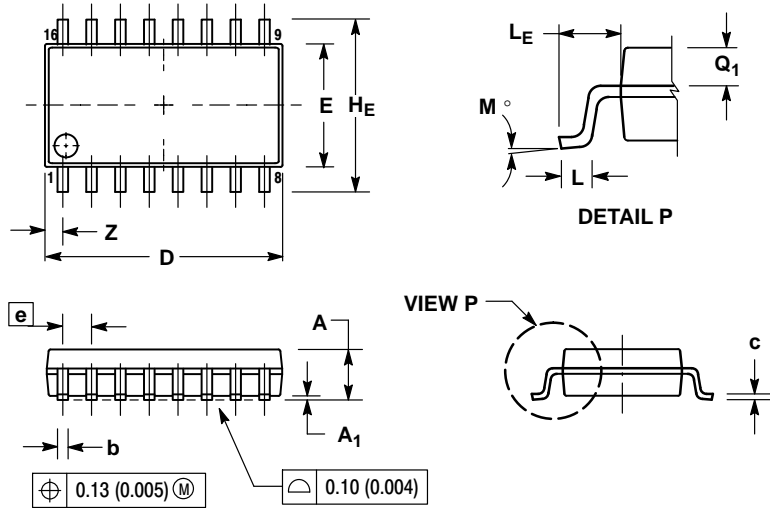


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC14536B

PACKAGE DIMENSIONS

SOEIAJ-16
CASE 966
ISSUE A




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q ₁	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

ECLinPS is a trademark of Semiconductor Components Industries, LLC (SCILLC).

ON Semiconductor and the  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

MC14536B/D