NBSG16VS

2.5 V/3.3 V SiGe Differential Receiver/Driver with Variable Output Swing

ON Semiconductor®

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QFN−16
MN SUFFIX
CASE 485G

Description

The NBSG16VS is a differential receiver/driver targeted for high frequency applications that require variable output swing. The device is functionally equivalent to the EP16VS device with much higher bandwidth and lower EMI capabilities. This device may be used for applications driving VCSEL lasers.

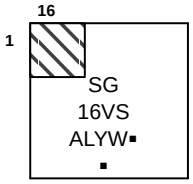
Inputs incorporate internal 50 Ω termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), LVTTL, LVCMOS, CML, or LVDS. The output amplitude is varied by applying a voltage to the V_{CTRL} input pin. Outputs are variable swing ECL from 100 mV to 750 mV amplitude, optimized for operation from $V_{CC} - V_{EE}$ = 3.0 V to 3.465 V.

The V_{BB} and V_{MM} pins are internally generated voltage supplies available to this device only. The V_{BB} is used as a reference voltage for single-ended NECL or PECL inputs and the V_{MM} pin is used as a reference voltage for LVCMOS inputs. For single-ended input operation, the unused complementary differential input is connected to V_{BB} or V_{MM} as a switching reference voltage. V_{BB} or V_{MM} may also rebias AC-coupled inputs. When used, decouple V_{BB} and V_{MM} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} and V_{MM} outputs should be left open.

Features

- Maximum Input Clock Frequency up to 12 GHz Typical
- Maximum Input Data Rate up to 12 Gb/s Typical
- 40 ps Typical Rise and Fall Times ($V_{CTRL} = V_{CC} - 1$ V)
- 120 ps Typical Propagation Delay ($V_{CTRL} = V_{CC} - 1$ V)
- Variable Swing PECL Output with Operating Range: V_{CC} = 2.375 V to 3.465 V with V_{EE} = 0 V
- Variable Swing NECL Output with NECL Inputs with Operating Range: V_{CC} = 0 V with V_{EE} = −2.375 V to −3.465 V
- Output Level (100 mV to 750 mV Peak-to-Peak Output; $V_{CC} - V_{EE}$ = 3.0 V to 3.465 V), Differential Output Only
- 50 Ω Internal Input Termination Resistors
- Compatible with Existing 2.5 V/3.3 V EP Devices
- V_{BB} and V_{MM} Reference Voltage Output
- These are Pb-Free Devices

MARKING DIAGRAMS*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

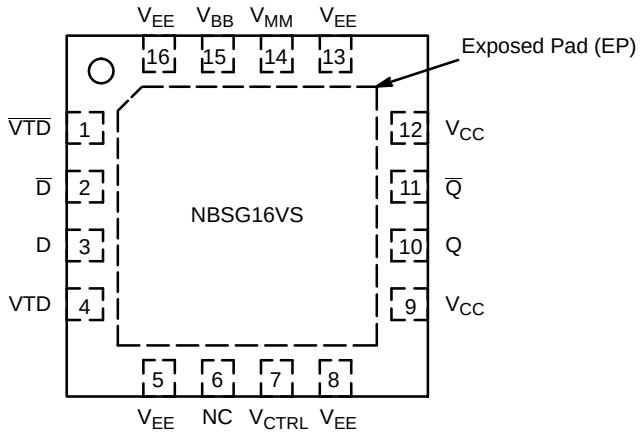


Figure 1. QFN−16 Pinout (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	$\overline{\text{VTD}}$	−	Internal 50 Ω Termination Pin. See Table 2.
2	$\overline{\text{D}}$	ECL, CML, LVCMOS, LVDS, LVTTL Input	Inverted Differential Input. Internal 75 kΩ to V_{EE} and 36.5 kΩ to V_{CC}.
3	D	ECL, CML, LVCMOS, LVDS, LVTTL Input	Noninverted Differential Input. Internal 75 kΩ to V_{EE}.
4	VTD	−	Internal 50 Ω Termination Pin. See Table 2.
5,8,13,16	V_{EE}	−	Negative Supply Voltage
6	NC	−	No Connect
7	V_{CTRL}		Output Amplitude Swing Control. Bypass Pin to V_{CC} through 0.1 μF Capacitor.
9,12	V_{CC}	−	Positive Supply Voltage
10	Q	RSECL Output	Noninverted Differential Output. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2$ V
11	$\overline{\text{Q}}$	RSECL Output	Inverted Differential Output. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2$ V
14	V_{MM}	−	LVCMOS Reference Voltage Output. $(V_{CC} - V_{EE})/2$
15	V_{BB}	−	ECL Reference Voltage Output
−	EP	−	The Exposed Pad (EP) on the QFN−16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is not electrically connected to the die but may be electrically and thermally connected to V_{EE} on the PC board.

1. All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation. The thermally exposed pad on package bottom (see case drawing) must be attached to a heat-sinking conduit.
2. In the differential configuration when the input termination pins (VTD, $\overline{\text{VTD}}$) are connected to a common termination voltage, and if no signal is applied then the device will be susceptible to self-oscillation.

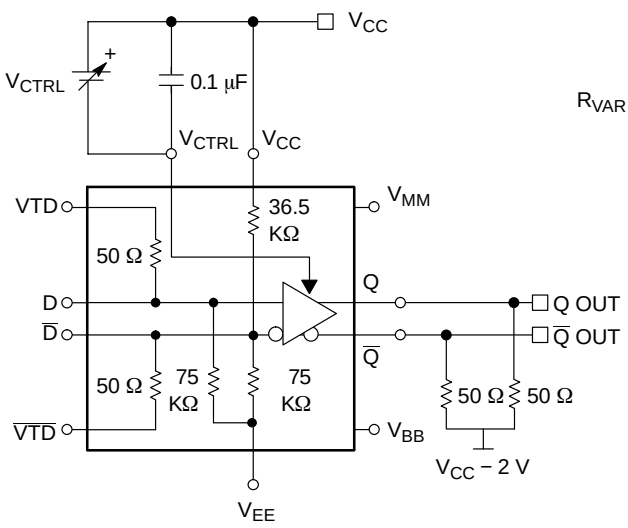


Figure 2. Logic Diagram/ Voltage Source Implementation

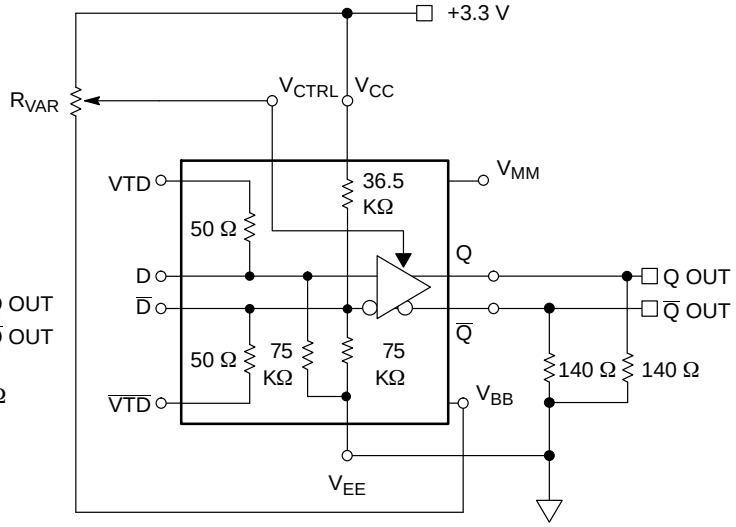


Figure 3. Alternative Voltage Source Implementation

Table 2. INTERFACING OPTIONS

INTERFACING OPTIONS	CONNECTIONS
CML	Connect VTD and $\overline{VTD}$ to V_{CC}
LVDS	Connect VTD and $\overline{VTD}$ Together
AC−COUPLED	Bias VTD and $\overline{VTD}$ Inputs within Common Mode Range (V_{IHCMR})
RSECL, PECL, NECL	Standard ECL Termination Techniques
LVTTL	An external voltage should be applied to the unused complementary differential input. Nominal voltage is 1.5 V for LVTTL.
LVCMOS	V_{MM} should be connected to the unused complementary differential input.

Table 3. ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor (D, $\overline{D}$)		75 kΩ
Internal Input Pullup Resistor ($\overline{D}$)		36.5 kΩ
ESD Protection	Human Body Model Machine Model	> 2 kV > 100 V
Moisture Sensitivity (Note 3)	Pb-Free	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		192
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

3. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	V_{EE} = 0 V		3.6	V
V_{EE}	Negative Power Supply	V_{CC} = 0 V		−3.6	V
V_I	Positive Input Negative Input	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	3.6 −3.6	V V
V_{INPP}	Differential Input Voltage $\lvert D - \overline{D} \rvert$	$V_{CC} - V_{EE} \ge 2.8$ V $V_{CC} - V_{EE} < 2.8$ V		2.8 $\lvert V_{CC} - V_{EE} \rvert$	V V
I_{OUT}	Output Current	Continuous Surge		25 50	mA mA
I_{IN}	Input Current Through R_T (50 Ω Resistor)	Static Surge		45 80	mA mA
I_{BB}	V_{BB} Sink/Source			1	mA
I_{MM}	V_{MM} Sink/Source			1	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient) (Note 4)	0 lfpm 500 lfpm		41.6 35.2	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	2S2P (Note 4)		4.0	°C/W
T_{sol}	Wave Solder Pb-Free			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. JEDEC standards multilayer board − 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 5. DC CHARACTERISTICS, INPUT WITH VARIABLE PECL OUTPUT
(V_{CC} = 2.5 V; V_{EE} = 0 V) (Note 5)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
POWER SUPPLY CURRENT											
I_{EE}	Negative Power Supply Current	18	25	32	18	25	32	18	25	32	mA
VARIABLE PECL OUTPUTS (Note 6)											
V_{OH}	Output HIGH Voltage	1315	1440	1565	1305	1430	1555	1305	1430	1555	mV
V_{OL}	Output LOW Voltage Max Swing $V_{CTRL} = V_{CC} - 600$ mV	 645 1090	 765 1210	 885 1330	 605 1035	 725 1155	 845 1275	 600 1010	 720 1130	 840 1250	mV
DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Figures 9 & 11) (Note 7)											
V_{IH}	Input HIGH Voltage	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{IL}	Input LOW Voltage	0		V_{IH} − 150	0		V_{IH} − 150	0		V_{IH} − 150	mV
V_{th}	Input Threshold Voltage Range (Note 8)	950		V_{CC} − 75	950		V_{CC} − 75	950		V_{CC} − 75	mV
V_{ISE}	Single-Ended Input Voltage ($V_{IH} - V_{IL}$)	150		2600	150		2600	150		260	mV
V_{BB}	PECL Output Voltage Reference	1080	1140	1200	1080	1140	1200	1080	1140	1200	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 10 & 12) (Note 9)											
V_{IHD}	Differential Input HIGH Voltage	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	0		V_{IHD} − 75	0		V_{IHD} − 75	0		V_{IHD} − 75	mV
V_{ID}	Differential Input Voltage ($V_{IHD} - V_{ILD}$)	75		2600	75		2600	75		2600	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 10) (Figure 13)	1200		2500	1200		2500	1200		2500	mV
I_{IH}	Input HIGH Current (@V_{IH})		30	100		30	100		30	100	μA
I_{IL}	Input LOW Current (@V_{IL})		25	50		25	50		25	50	μA
LVCMOS CONTROL PIN											
V_{MM}	CMOS Output Voltage Reference ($V_{CC} - V_{EE}$) / 2	1100	1250	1400	1100	1250	1400	1100	1250	1400	mV
TERMINATION RESISTORS											
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Input and output parameters vary 1:1 with V_{CC}.
6. All loading with 50 Ω to V_{CC} − 2.0 V.
7. V_{th}, V_{IH}, V_{IL}, and V_{ISE} parameters must be complied with simultaneously.
8. V_{th} is applied to the complementary input when operating in single-ended mode. $V_{th} = (V_{IH} - V_{IL}) / 2$.
9. V_{IHD}, V_{ILD}, V_{ID} and V_{IHCMR} parameters must be complied with simultaneously.
10. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 6. DC CHARACTERISTICS, INPUT WITH VARIABLE PECL OUTPUT
(V_{CC} = 3.3 V; V_{EE} = 0 V) (Note 11)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
POWER SUPPLY CURRENT											
I_{EE}	Negative Power Supply Current	20	27	34	20	27	34	20	27	34	mA
VARIABLE PECL OUTPUTS (Note 12)											
V_{OH}	Output HIGH Voltage	2095	2220	2345	2085	2210	2335	2075	2200	2325	mV
V_{OL}	Output LOW Voltage Max Swing $V_{CTRL} = V_{CC} - 600$ mV	 1275 1750	 1395 1870	 1515 1990	 1285 1730	 1405 1850	 1525 1970	 1295 1715	 1415 1835	 1535 1955	mV
DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Figures 9 & 11) (Note 13)											
V_{IH}	Input HIGH Voltage	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{IL}	Input LOW Voltage	0		V_{IH} − 150	0		V_{IH} − 150	0		V_{IH} − 150	mV
V_{th}	Input Threshold Voltage Range (Note 14)	950		V_{CC} − 75	950		V_{CC} − 75	950		V_{CC} − 75	mV
V_{ISE}	Single-Ended Input Voltage ($V_{IH} - V_{IL}$)	150		2600	150		2600	150		260	mV
V_{BB}	PECL Output Voltage Reference	1800	1940	2000	1800	1940	2000	1800	1940	2000	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 10 & 12) (Note 15)											
V_{IHD}	Differential Input HIGH Voltage	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	0		V_{IHD} − 75	0		V_{IHD} − 75	0		V_{IHD} − 75	mV
V_{ID}	Differential Input Voltage ($V_{IHD} - V_{ILD}$)	75		2600	75		2600	75		2600	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 16) (Figure 13)	1200		3300	1200		3300	1200		3300	mV
I_{IH}	Input HIGH Current (@V_{IH})		30	100		30	100		30	100	μA
I_{IL}	Input LOW Current (@V_{IL})		25	50		25	50		25	50	μA
LVCMOS CONTROL PIN											
V_{MM}	CMOS Output Voltage Reference ($V_{CC} - V_{EE}$) / 2	1500	1650	1800	1500	1650	1800	1500	1650	1800	mV
TERMINATION RESISTORS											
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

11. Input and output parameters vary 1:1 with V_{CC}.
12. All loading with 50 Ω to V_{CC} − 2.0 V.
13. V_{th}, V_{IH}, V_{IL}, and V_{ISE} parameters must be complied with simultaneously.
14. V_{th} is applied to the complementary input when operating in single-ended mode. $V_{th} = (V_{IH} - V_{IL}) / 2$.
15. V_{IHD}, V_{ILD}, V_{ID} and V_{IHCMR} parameters must be complied with simultaneously.
16. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 7. DC CHARACTERISTICS, INPUT WITH VARIABLE NECL OUTPUT
(V_{CC} = 0 V; V_{EE} = −3.465 V to −2.375 V) (Note 17)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
POWER SUPPLY CURRENT											
I_{EE}	Negative Power Supply Current	20	27	34	20	27	34	20	27	34	mA
VARIABLE NECL OUTPUTS (Note 18)											
V_{OH}	Output HIGH Voltage	−1205 −1185	−1080 −1060	−955 −935	−1215 −1195	−1090 −1070	−965 −945	−1225 −1195	−1100 −1070	−975 −945	mV
V_{OL}	Output LOW Voltage Max Swing $V_{CTRL} = V_{CC}$ − 600 mV −3.0 V < V_{EE} ≤ −2.375 V Max Swing $V_{CTRL} = V_{CC}$ − 600 mV	 −2000 −1560 −1855 −1410	 −1910 −1440 −1620 −1215	 −1820 −1320 −1290 −1000	 −1990 −1580 −1895 −1460	 −1900 −1460 −1705 −1290	 −1810 −1340 −1425 −1100	 −1980 −1595 −1900 −1490	 −1890 −1475 −1730 −1330	 −1800 −1355 −1470 −1150	mV
DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Figures 9 & 11) (Note 19)											
V_{IH}	Input HIGH Voltage	V_{EE} + 1200		V_{CC}	V_{EE} + 1200		V_{CC}	V_{EE} + 1200		V_{CC}	mV
V_{IL}	Input LOW Voltage	V_{EE}		V_{IH} − 150	V_{EE}		V_{IH} − 150	V_{EE}		V_{IH} − 150	mV
V_{th}	Input Threshold Voltage Range (Note 20)	V_{EE} + 950		V_{CC} − 75	V_{EE} + 950		V_{CC} − 75	V_{EE} + 950		V_{CC} − 75	mV
V_{ISE}	Single-Ended Input Voltage (V_{IH} − V_{IL})	150		2600	150		2600	150		260	mV
V_{BB}	NECL Output Voltage Reference	−1420	−1360	−1300	−1420	−1360	−1300	−1420	−1360	−1300	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 10 & 12) (Note 21)											
V_{IHD}	Differential Input HIGH Voltage	V_{EE} + 1200		V_{CC}	V_{EE} + 1200		V_{CC}	V_{EE} + 1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	V_{EE}		V_{IHD} − 75	V_{EE}		V_{IHD} − 75	V_{EE}		V_{IHD} − 75	mV
V_{ID}	Differential Input Voltage (V_{IHD} − V_{ILD})	75		2600	75		2600	75		2600	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 22) (Figure 13)	V_{EE} + 1200		0	V_{EE} + 1200		0	V_{EE} + 1200		0	mV
I_{IH}	Input HIGH Current (@V_{IH})		30	100		30	100		30	100	μA
I_{IL}	Input LOW Current (@V_{IL})		25	50		25	50		25	50	μA
LVCMOS CONTROL PIN (Note 23)											
V_{MM}	CMOS Output Voltage Reference	V_{MM} − 150	V_{MM}	V_{MM} + 150	V_{MM} − 150	V_{MM}	V_{MM} + 150	V_{MM} − 150	V_{MM}	V_{MM} + 150	mV
TERMINATION RESISTORS											
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

17. Input and output parameters vary 1:1 with V_{CC}.
18. All loading with 50 Ω to V_{CC} − 2.0 V.
19. V_{th}, V_{IH}, V_{IL}, and V_{ISE} parameters must be complied with simultaneously.
20. V_{th} is applied to the complementary input when operating in single-ended mode. V_{th} = (V_{IH} − V_{IL}) / 2.
21. V_{IHD}, V_{ILD}, V_{ID} and V_{IHCMR} parameters must be complied with simultaneously.
22. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
23. V_{MM} typical = |V_{CC} − V_{EE}| / 2 + V_{EE} = V_{MMT}

Table 8. AC CHARACTERISTICS

(V_{CC} = 0 V; V_{EE} = −3.465 V to −3.0 V or V_{CC} = 3.0 V to 3.465 V; V_{EE} = 0 V)

		−40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Input Clock Frequency (See Figure 7) (Note 24)	10 (Note 27)	12		10 (Note 27)	12		10 (Note 27)	12		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential										ps
	(V_{CTRL} = V_{CC} − 2 V) D → Q, $\overline{Q}$	100	140	180	100	140	180	100	140	180	
	(V_{CTRL} = V_{CC} − 1 V) D → Q, $\overline{Q}$	100	135	180	100	135	180	80	135	220	
t_{SKEW}	Duty Cycle Skew (Note 25)		3	20		3	15		3	10	ps
t_{JITTER}	RMS Random Clock Jitter										ps
	f_{in} < 10 GHz		0.5	2		0.5	2		0.5	2	
	Peak−to−Peak Data Dependent Jitter										
	f_{in} < 10 Gb/s		5			5			5		
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 26)	75		2600	75		2600	75		2600	mV
t_r t_f	Output Rise/Fall Times (20% − 80%) @ 1 GHz										ps
	(V_{CTRL} = V_{CC} − 2 V) Q, $\overline{Q}$	30	45	55	30	45	55	30	45	55	
	(V_{CTRL} = V_{CC} − 1 V) Q, $\overline{Q}$	30	40	50	30	40	50	30	40	50	

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

24. Measured using a 500 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC} − 2.0 V. Input edge rates 40 ps (20% − 80%).
25. t_{SKEW} = $|t_{PLH} - t_{PHL}|$ for a nominal 50% differential clock input waveform. See Figure 14.
26. $V_{INPP(MAX)}$ cannot exceed V_{CC} − V_{EE} (applicable only when V_{CC} − V_{EE} < 2600 mV).
27. Conditions include input amplitude of 500 mV and V_{CTRL} = V_{CC} − 2 V. Minimum output amplitude guarantee of 100 mV (see Output P−P Spec in Figure 7).

Table 9. AC CHARACTERISTICS

(V_{CC} = 0 V; −3.0 V < V_{EE} ≤ −2.375 V or 2.375 V ≤ V_{CC} < 3.0 V; V_{EE} = 0 V)

		−40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Input Clock Frequency (See Figure 8) (Note 28)	10 (Note 31)	12		10 (Note 31)	12		10 (Note 31)	12		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential										ps
	(V_{CTRL} = V_{CC} − 2 V) D → Q, $\overline{Q}$	100	140	180	100	140	180	80	140	180	
	(V_{CTRL} = V_{CC} − 1 V) D → Q, $\overline{Q}$	100	135	180	100	135	180	100	135	220	
t_{SKEW}	Duty Cycle Skew (Note 29)		3	20		3	15		3	10	ps
t_{JITTER}	RMS Random Clock Jitter										ps
	f_{in} < 10 GHz		0.5	3		0.5	3		0.5	3	
	Peak−to−Peak Data Dependent Jitter										
	f_{in} < 10 Gb/s		5			5			5		
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 30)	75		2600	75		2600	75		2600	mV
t_r t_f	Output Rise/Fall Times (20% − 80%) @ 1 GHz										ps
	(V_{CTRL} = V_{CC} − 2 V) Q, $\overline{Q}$	25	50	70	25	50	70	25	50	70	
	(V_{CTRL} = V_{CC} − 1 V) Q, $\overline{Q}$	22	45	60	22	45	60	22	45	60	

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

28. Measured using a 500 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC} − 2.0 V. Input edge rates 40 ps (20% − 80%).
29. t_{SKEW} = $|t_{PLH} - t_{PHL}|$ for a nominal 50% differential clock input waveform. See Figure 14.
30. $V_{INPP(MAX)}$ cannot exceed V_{CC} − V_{EE} (applicable only when V_{CC} − V_{EE} < 2600 mV).
31. Conditions include input amplitude of 500 mV and V_{CTRL} = V_{CC} − 2 V. Minimum output amplitude guarantee of 100 mV (see Output P−P Spec in Figure 8), 80 mV at −40°C..

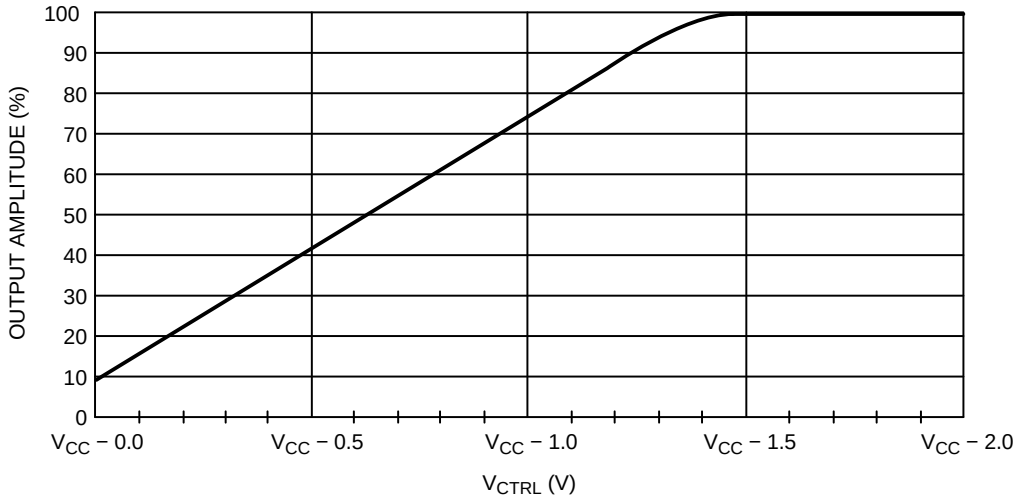


Figure 4. Output Amplitude % vs. V_{CTRL} (pin #A3)

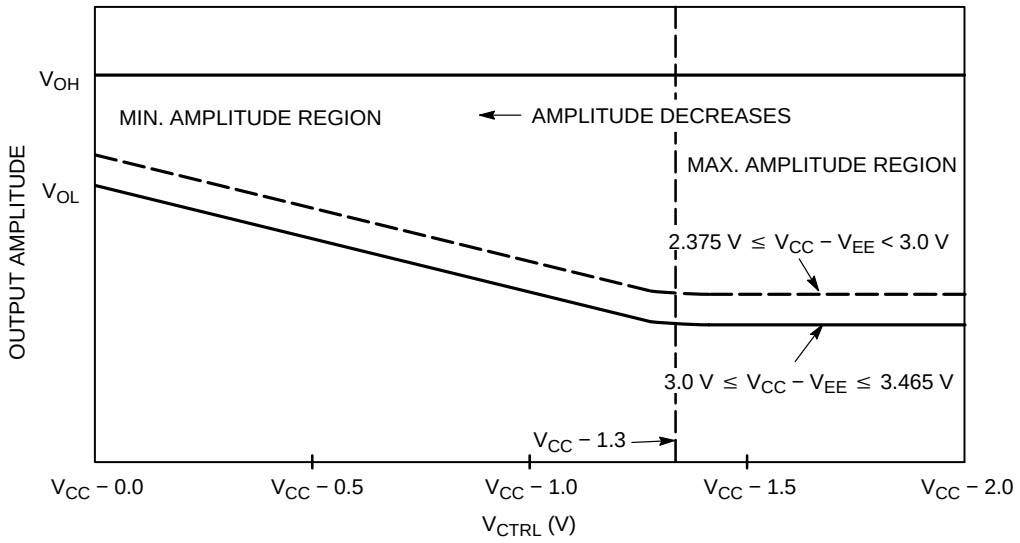


Figure 5. Output Amplitude vs. V_{CTRL} (pin #A3)

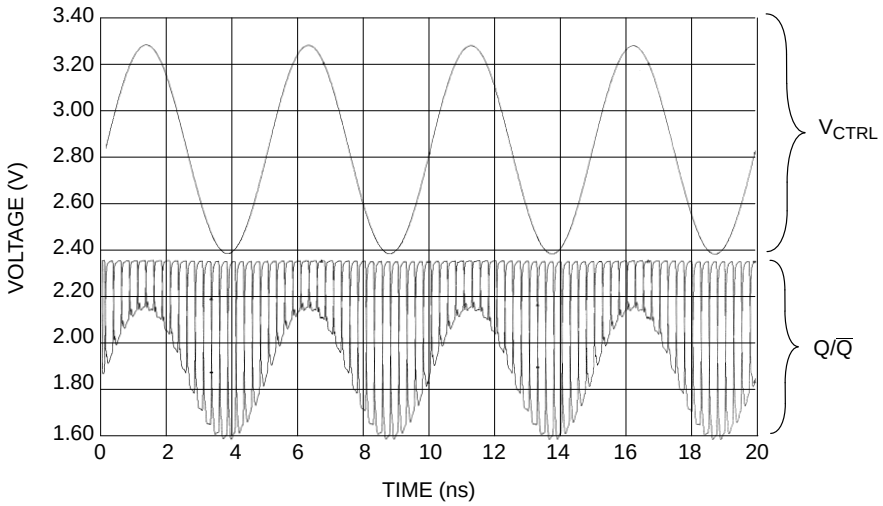


Figure 6. Output Response Under Amplitude Modulation of V_{CTRL} (Conditions Include $V_{CC} - V_{EE}$ = 3.3 V at 25°C, f_{IN} (V_{CTRL}) = 200 MHz, and f_{IN} (D, $\overline{D}$) = 2 GHz)

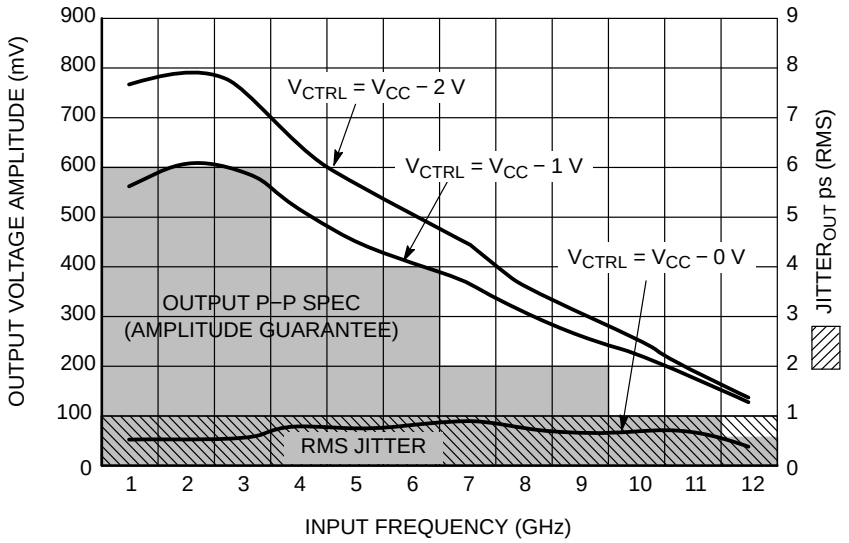


Figure 7. Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) at Ambient Temperature (Typical) See Table 8 (V_{CC} = 0 V; V_{EE} = −3.465 V to −3.0 V or V_{CC} = 3.0 V to 3.465 V; V_{EE} = 0 V

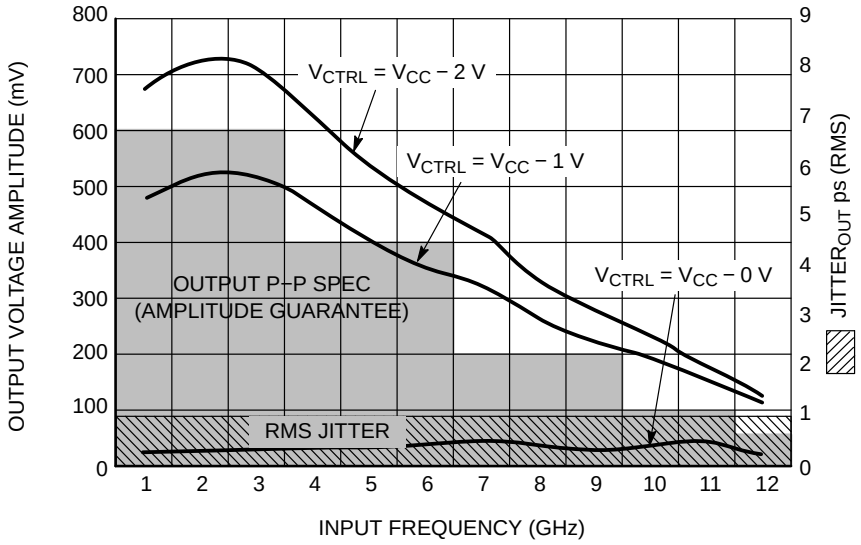


Figure 8. Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) at Ambient Temperature (Typical) See Table 9 (V_{CC} = 0 V; −3.0 V V_{EE} −2.375 V or 2.375 V V_{CC} 3.0 V; V_{EE} = 0 V)

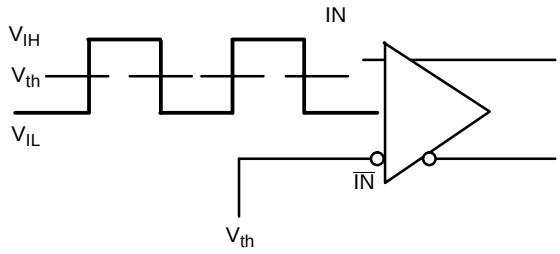


Figure 9. Differential Input Driven Single-Ended

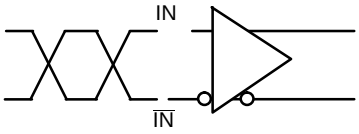


Figure 10. Differential Inputs Driven Differentially

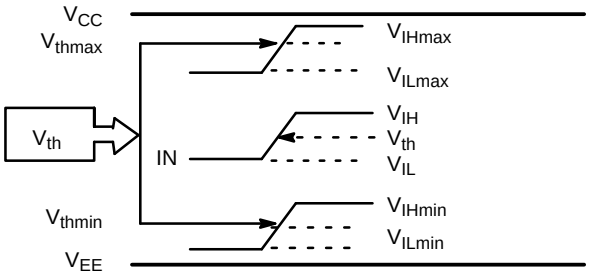


Figure 11. V_{th} Diagram

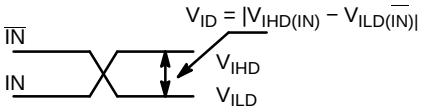


Figure 12. Differential Inputs Driven Differentially

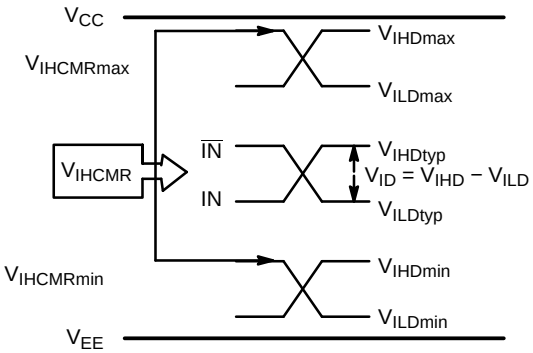


Figure 13. V_{IHCMR} Diagram

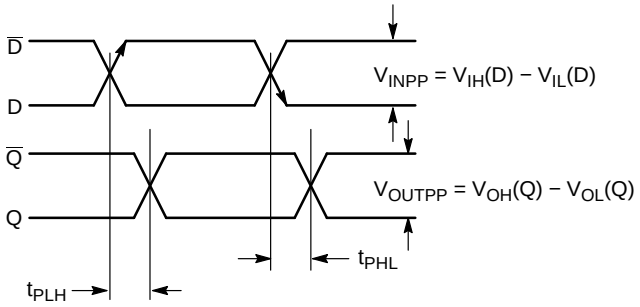


Figure 14. AC Reference Measurement

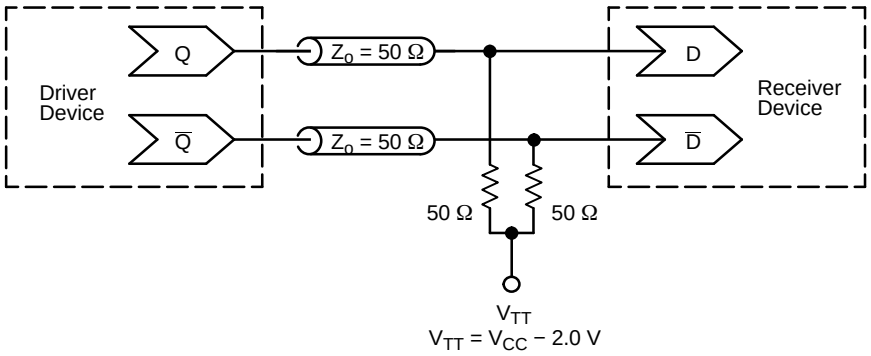


Figure 15. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)

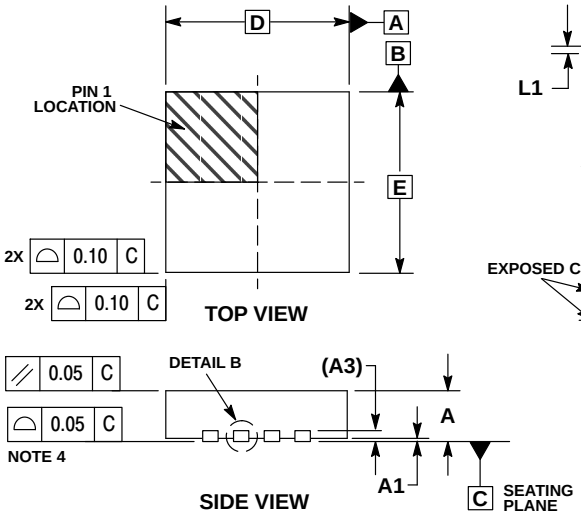
ORDERING INFORMATION

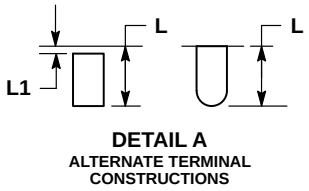
Device	Package	Shipping†
NBSG16VSMNG	QFN-16 (Pb-Free / Halide-Free)	123 Units / Tube
NBSG16VSMNR2G	QFN-16 (Pb-Free / Halide-Free)	3000 / Tape & Reel
NBSG16VSMNHTBG	QFN-16 (Pb-Free / Halide-Free)	100 / Tape & Reel

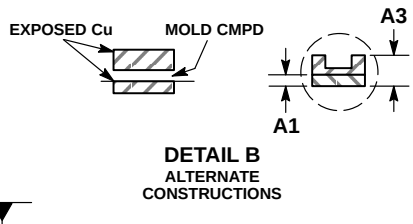
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

QFN16 3x3, 0.5P
CASE 485G
ISSUE F

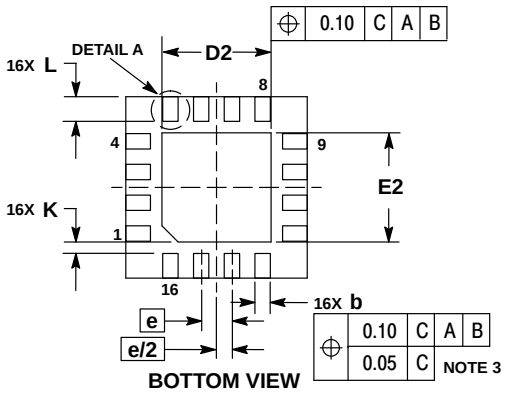




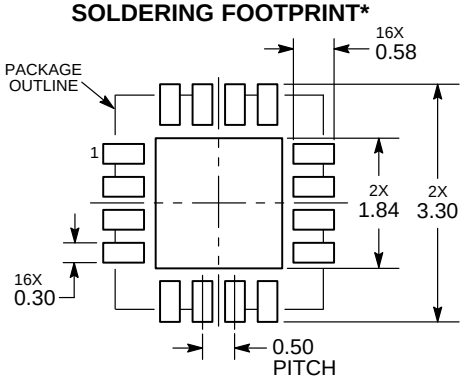


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3		0.20 REF	
b	0.18	0.24	0.30
D		3.00 BSC	
D2	1.65	1.75	1.85
E		3.00 BSC	
E2	1.65	1.75	1.85
e		0.50 BSC	
K		0.18 TYP	
L	0.30	0.40	0.50
L1	0.00	0.08	0.15



RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

The products described herein (NBSG16VS), may be covered by U.S. patents including 6,362,644. There may be other patents pending.

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