FAIRCHILD SEMICONDUCTOR™

September 1195
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CGS3321 • CGS3322
CMOS Crystal Clock Generators

General Description

The CGS3321 and CGS3322 devices are designed for Clock Generation and Support (CGS) applications up to 110 MHz. The CGS332x series of devices are crystal controlled CMOS oscillators requiring a minimum of external components. The 332x devices provide selectable output divide ratio. The circuit is designed to operate over a wide frequency range using fundamental mode or overtone crystals.

Features

- Fairchild's CGS family of devices for high frequency clock source applications
- Crystal frequency operation range:
  fundamental: 10 MHz to 100 MHz typical
  3rd or 5th overtone: 10 MHz to 95 MHz
- 1000V ESD protection on OCS_IN and OSC_OUT pins.
  2000V ESD protection on all other pins
- Output current drive of 48 mA for I_{OL}/I_{OH}
- FACT™ CMOS output levels
- Output has high speed short circuit protection
- Intended for Pierce oscillator applications
- Hysteresis inputs to improve noise margin
- CGS3321 has duty cycle adjust
- CGS3322 has 1, 2, 4 divide ratio

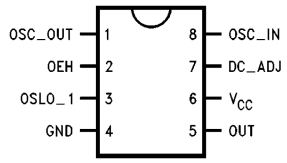
Ordering Code:

Order Number	Package Number	Package Description
CGS3321M	M08A	8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CGS3322M	M08A	8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

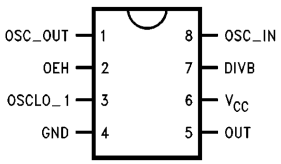
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

CGS3321



CGS3322



Truth Table

Division Selection

DIVB	OEH	Divider Output
F	X	Divide-by 1
1	1	Divide-by 2
0	1	Divide-by 4

Note: Actual value of the floating DIVB input is $V_{CC/2}$

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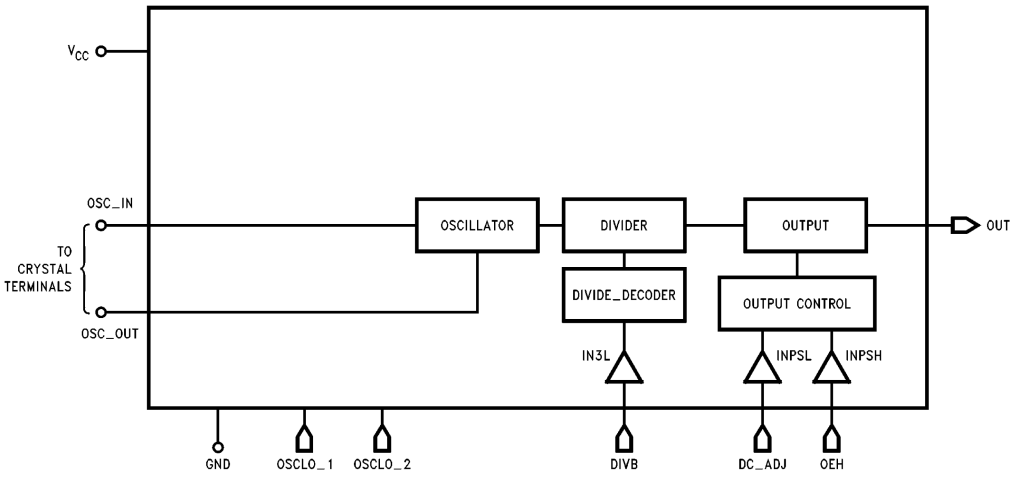
Pin Descriptions

Note: Pin out varies for each device.

OSC_IN	Input to Oscillator Inverter. The output of the crystal would be connected here.	OEH	Active HIGH 3-STATE enable pin. This pin pulls to a HIGH value when left floating and 3-STATEs the output when forced LOW. This pin has TTL compatible input levels.
OSC_OUT	Resistive Buffered Output of the Oscillator Inverter	OUT	This pin is the main clock output on the device.
DIVB	(CGS3322 only) 3-Level input used to select Binary Divide-by value of output frequency.	OSCLO_1	The Oscillator LOW pin is the ground for the Oscillator.
DC_ADJ	(CGS3321 only) Active high input that controls output duty cycle. Logic high level will delay the HL transition edge approximately 0.3 ns.	V_{CC}	The power pin for the chip.
		GND	The ground pin for all sections of the circuitry except the oscillator and oscillator related circuitry.

Note: Pin out varies for each device.

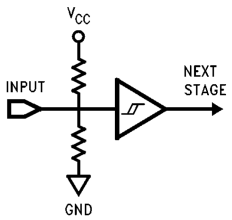
Block Diagrams



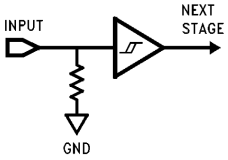
Note: Pin numbers vary for each device

Block Diagrams (Continued)

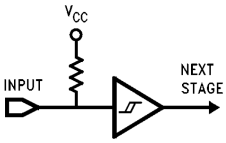
IN3L



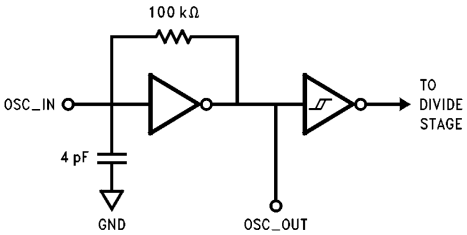
INPSL



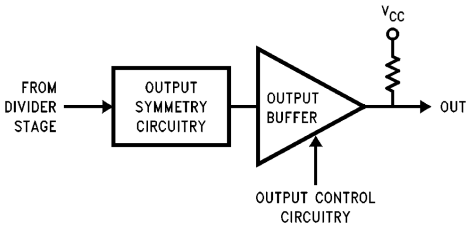
INPSH

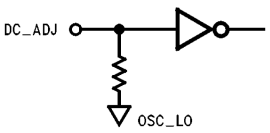


Oscillator Stage



Output Stage





Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to 7.0V
DC Input Voltage Diode Current (I_{IK})	±9 mA
DC Input Voltage (V_I)	−0.5V to 7.0V
DC Output Diode Current (I_{OK})	±20 mA
DC Output Voltage (V_O)	-0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±70 mA
Storage Temperature (T_{STG})	−55°C to 150°C
Junction Temperature (T_J)	
SOIC	140°C/W

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	0V to V_{CC} V
Operating Temperature (T_A)	−40° to +85°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = +25°C			T_A = −40° C to +85°C		Units	Conditions
			Typ	Guaranteed Limits					
				Min	Max	Min	Max		
V_{IHTTL}	Minimum HIGH Level Input Voltage, TTL Level Inputs (OEH, OEL)	4.5		2.0		2.0		V	
		5.5		2.0		2.0			
V_{ILTTL}	Maximum LOW Level Input Voltage, TTL Level Inputs (OEH, OEL)	4.5			0.8		0.8	V	
		5.5			0.8		0.8		
V_{IHCMOS}	Minimum HIGH Level Input Voltage. CMOS Level Inputs (DC_ADJ)	4.5		3.15		3.15		V	
		5.5		3.85		3.85			
V_{ILCMOS}	Maximum LOW Level Input voltage. CMOS Level Inputs (DC_ADJ)	4.5			1.35		1.35	V	
		5.5			1.65		1.65		
V_{IN3L_H}	Minimum Logic 1 Input for Three Level Input (DIVB)	4.5		4.05		4.05		V	
		5.5		4.95		4.95			
$V_{IN3L\_1/2}$	Minimum Logic 1/2 Input for Three Level Input (DIVB)	4.5		1.8	2.7	1.8	2.7	V	
		5.5		2.2	3.3	2.2	3.3		
V_{IN3L_L}	Maximum Logic 0 Input Level Three Level Input (DIVB)	4.5			0.45		0.45	V	
		5.5			0.45		0.45		
V_{OH}	Minimum HIGH Level Output Voltage	4.5	4.49	4.40		4.40		V	I_{OUT} = −50µA
		5.5	5.49	5.40		5.40			
		4.5		3.86		3.76			I_{OH} = −48 mA
		5.5		4.86		4.76			V_{IN} = V_{IH} or V_{IH}
V_{OL}	Minimum LOW Level Output Voltage	4.5	0.001		0.1		0.1	V	I_{OUT} = 50µA
		5.5	0.001		0.1		0.1		
		4.5			0.44		0.44		I_{OL} = +48mA
		5.5			0.44		0.44		V_{IN} = V_{IL} or V_{IH}
I_{IHRES}	Input Current for Pins DIVB	5.5		220	360	200	380	µA	V_{IN} = 5.5V
I_{ILRES}	Input Current for Pins DIVB	5.5		−220	−360	−200	−380	µA	VIN = 0.0V
I_{IHENAB}	Input Current for Enable Pin OEL	5.5		90	160	85	175	µA	V_{IN} = 5.5V
I_{ILENAB}	Input Current for Enable Pin OEH	5.5		−90	−160	−85	−175	µA	V_{IN} = 0.0V
I_{IHOSC}	Input Current for OSC_IN Pin (Indicates Bias Resistance)	5.5		20	100	20	125	µA	V_{IN} = 5.5V
I_{ILOSC}	Input Current for OSC_IN Pin (Indicates Bias Resistance)	5.5		−20	−100	−20	−125	µA	V_{IN} = 0.0V
I_{OZH}	Output Disabled Current (Output HIGH)	4.5			3.0		5.0	µA	V_{OUT} = V_{CC}
		5.5			3.0		5.0		
I_{OZL}	Output Disabled Current (Output LOW)	4.5			−140		−150	µA	V_{OUT} = 0.0V
		5.5			−170		−180		

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$	$T_A = -40°C$ to $+85°C$				Units	Conditions
			Typ	Guaranteed Limits					
				Min	Max	Min	Max		
I_{OLD}	Minimum Dynamic Output Current	5.5		75		75		mA	V_{OLD} = 1.65V
I_{OHD}	Minimum Dynamic Output Current	5.5		−75		−75		mA	V_{OHD} = 3.85V
I_{CCT}	Additional Maximum I_{CC} per Input (OEH, OEL Pins)	5.5			1.5		1.5	mA	$V_{IN} = V_{CC} - 2.1V$
I_{CC3L}	Additional Maximum I_{CC} per Input (DIVB)	5.5			1.5		1.5	mA	DIVB, OSC_DR Inputs Equal to $V_{CC/2}$

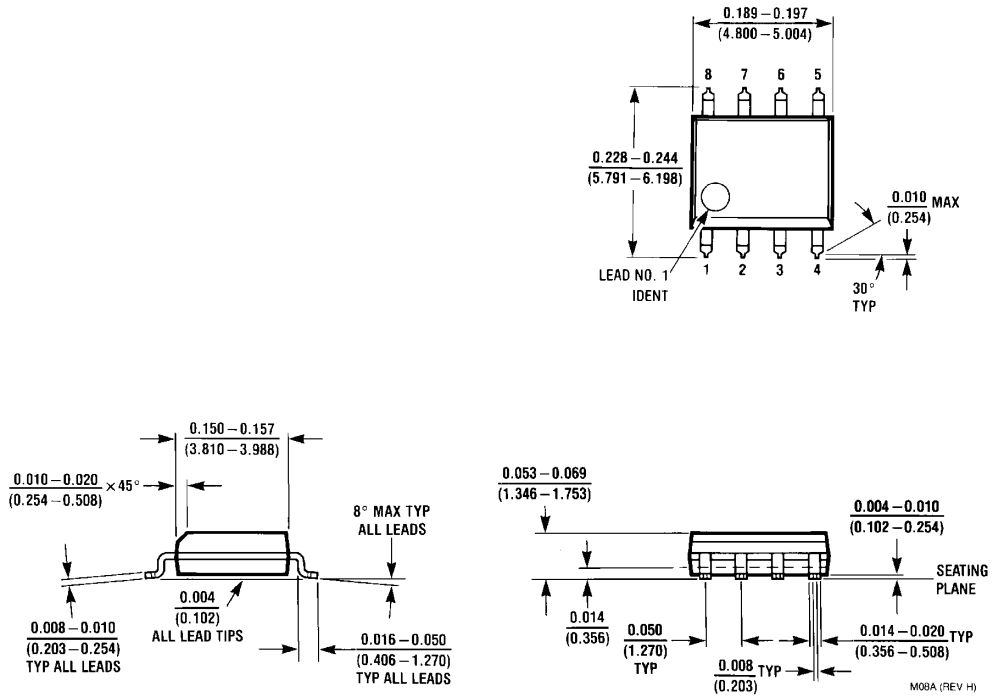
AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	V_{CC} (V) (Note 2)	$T_A = -40°C$ to $+85°C$ C_L = 50 pF			Units
			Min	Type	Max	
f_{MAX}	Frequency Maximum	5.0	95	110		MHz
t_{PZH}	Output HIGH Enable Time	5.0	1.0		31.5	ns
t_{PZL}	Output LOW Enable Time	5.0	1.0		28.0	ns
t_{PHZ}	Output HIGH Disable Time	5.0	1.0		21.5	ns
t_{PLZ}	Output LOW Disable Time	5.0	1.0		16.0	ns
t_{RISE} t_{FALL}	Rise/Fall Time 30 pF (20% to 80%)	5.0		1.0		ns

Note 2: Voltage Range 5.0 is 5.0V ± 0.5V

Physical Dimensions inches (millimeters) unless otherwise noted



8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M08A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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