

## FIN3385 / FIN3383 / FIN3384 / FIN3386 Low-Voltage 28-Bit Flat Panel Display Link Serializer / Deserializer

### Features


- Low Power Consumption
- 20MHz to 85MHz Shift Clock Support
- ±1V Common-Mode Range around 1.2V
- Narrow Bus Reduces Cable Size and Cost
- High Throughput (up to 2.38Gbps)
- Internal PLL with No External Component
- Compatible with TIA/EIA-644 Specification
- 56-Lead TSSOP Package

### Description

The FIN3385 and FIN3383 transform 28-bit wide parallel LVTTTL (Low-Voltage TTL) data into four serial LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data stream over a separate LVDS link. Every cycle of transmit clock, 28 bits of input LVTTTL data are sampled and transmitted.

The FIN3386 and FIN3384 receive and convert the 4/3 serial LVDS data streams back into 28/21 bits of LVTTTL data. Refer to Table 1 for a matrix summary of the serializers and deserializers available. For the FIN3385, at a transmit clock frequency of 85MHz, 28-bits of LVTTTL data are transmitted at a rate of 595Mbps per LVDS channel. These chipsets solve EMI and cable size problems associated with wide and high-speed TTL interfaces.

### Ordering Information

Part Number	Operating Temperature Range	 Eco Status	Package	Packing Method
FIN3383MTDX	-10 to +70°C	RoHS	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153,6.1mm Wide	Tape and Reel
FIN3384MTDX				
FIN3385MTDX				
FIN3386MTDX				

 For Fairchild's definition of Eco Status, please visit: [http://www.fairchildsemi.com/company/green/rohs\\_green.html](http://www.fairchildsemi.com/company/green/rohs_green.html).

**Table 1. Display Panel Link Serializer / Deserializer Chip Matrix**

Part	CLK Frequency	LVTTTL In	LVDS Out	LVDS In	LVTTTL Out	Package
FIN3385	85	28	4			56 TSSOP
FIN3383	66	28	4			
FIN3386	85			4	28	
FIN3384	66			4	28	

## Block Diagrams

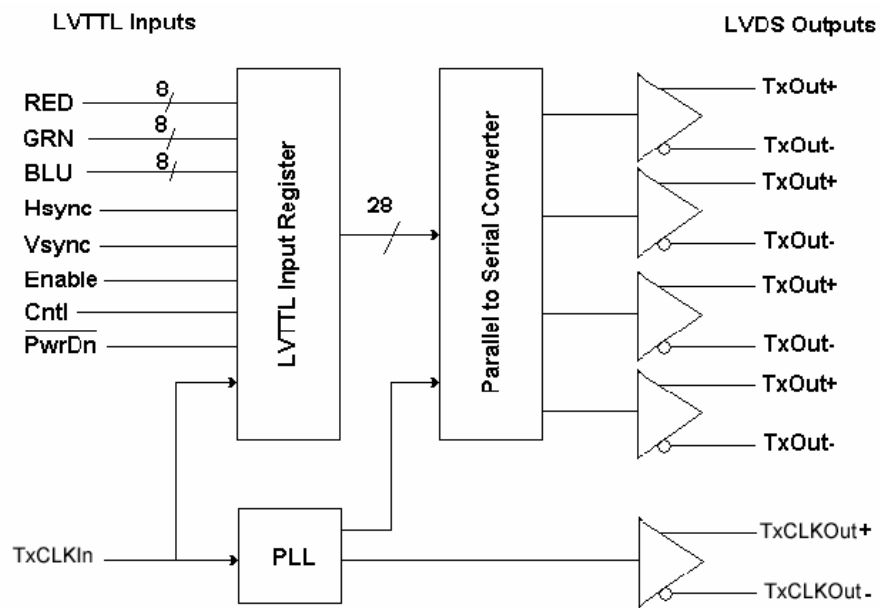


Figure 1. FIN3385 and FIN3383 Transmitter Functional Diagram

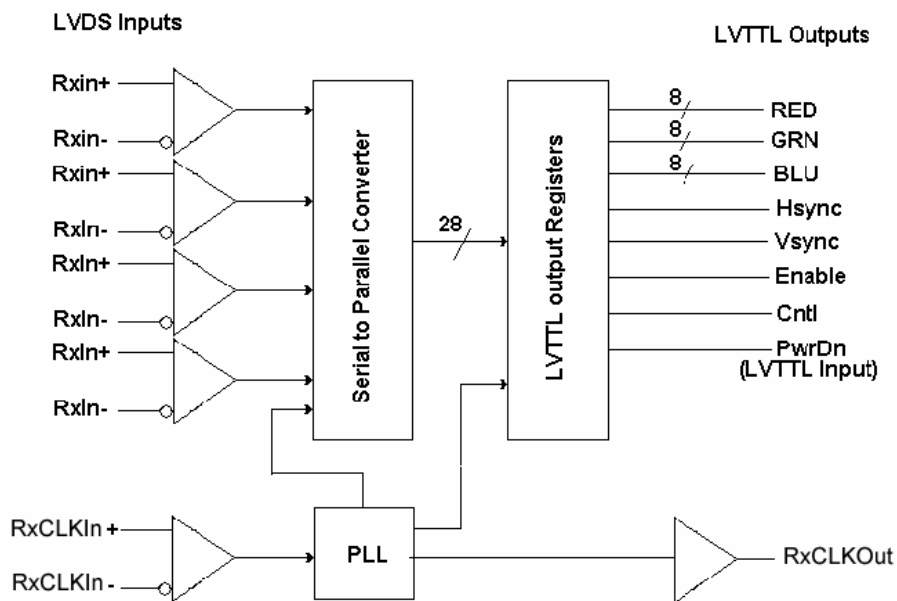


Figure 2. FIN3386 and FIN3384 Receiver Functional Diagram

## Transmitters

### Pin Configuration

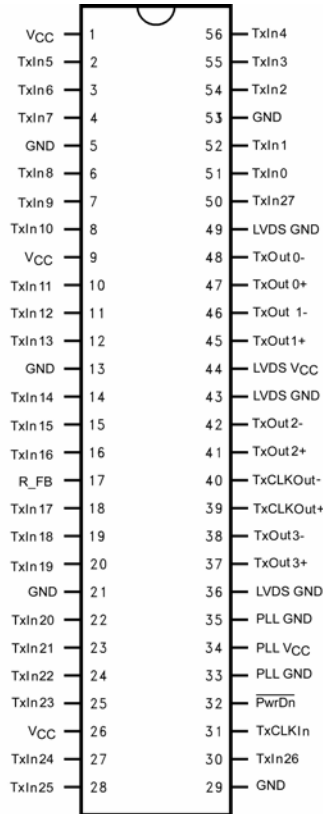


Figure 3. FIN3383 and FIN3385 (28:4 Transmitter) Pin Assignment

### Truth Table

Inputs			Outputs	
TxIn	TxCLKIn	/PwrDn <sup>(1)</sup>	TxOut±	TxCLKOut±
Active	Active	HIGH	LOW/ HIGH	LOW/ HIGH
Active	LOW/ HIGH/ High Impedance	HIGH	LOW/ HIGH	Don't Care <sup>(2)</sup>
Floating	Active	HIGH	LOW	LOW/ HIGH
Floating	Floating	HIGH	LOW	Don't Care <sup>(2)</sup>
Don't Care	Don't Care	LOW	High Impedance	High Impedance

#### Notes:

1. The outputs of the transmitter or receiver remains in a high-impedance state until  $V_{CC}$  reaches 2V.
2. TxCLKOut± settles at a free-running frequency when the part is powered up, /PwrDn is HIGH, and the TxCLKIn is a steady logic level (LOW / HIGH / High-Impedance).

### Pin Definitions

Pin Names	I/O Types	Number of Pins	Description of Signals
TxIn	I	28/21	LVTTL Level Input
TxCLKIn	I	1	LVTTL Level Clock Input, the rising edge is for data strobe
TxOut+	O	4/3	Positive LVDS Differential Data Output
TxOut-	O	4/3	Negative LVDS Differential Data Output
TxCLKOut+	O	1	Positive LVDS Differential Clock Output
TxCLKOut-	O	1	Negative LVDS Differential Clock Output
R_FB	I	1	Rising Edge Data Strobe: Assert HIGH ( $V_{CC}$ ) Falling Edge Data Strobe: Assert LOW (Ground)
/PwrDn	I	1	LVTTL Level Power-Down Input Assertion (LOW) puts the outputs in high-impedance state
PLL V <sub>cc</sub>	I	1	Power Supply Pin for PLL
PLL GND	I	2	Ground Pins for PLL
LVDS V <sub>cc</sub>	I	1	Power Supply Pin for LVDS Output
LVDS GND	I	3	Ground Pins for LVDS Output
V <sub>cc</sub>	I	3	Power Supply Pins for LVTTL Input
GND	I	5	Ground Pin for LVTTL Input

## Receivers

### Pin Configuration

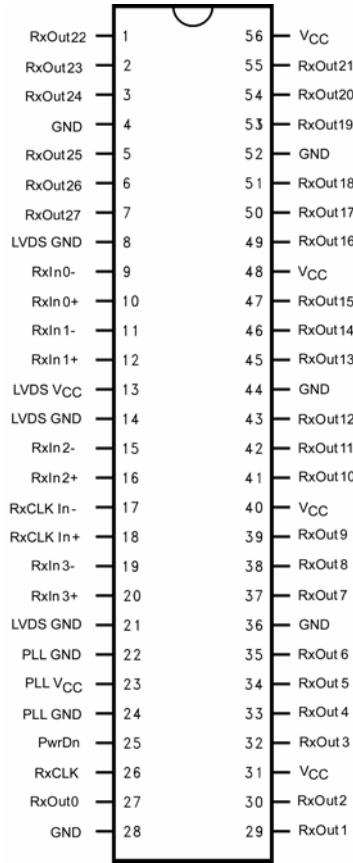


Figure 4. FIN3386 and FIN3384(28:4 Receiver) Pin Assignment

### Pin Definitions

Pin Names	I/O Types	Number of Pins	Description of Signals
RxIn	I	4/3	Negative LVDS Differential Data Output
RxIn+	I	4/3	Positive LVDS Differential Data Output
RxCLKIn-	I	1	Negative LVDS Differential Data Input
RxCLKIn+	I	1	Positive LVDS Differential Clock Input
RxOut	O	28/21	LVTTTL Level Data Output, goes HIGH for /PwrDn LOW
RxCLKOut-	O	1	LVTTTL Clock Output
/PwrDn	I	1	LVTTTL Level Input. Refer to Transmitter and Receiver Power-Up and Power-Down Operation Truth Table
PLL V <sub>CC</sub>	I	1	Power Supply Pin for PLL
PLL GND	I	2	Ground Pins for PLL
LVDS V <sub>CC</sub>	I	1	Power Supply Pin for LVDS Input
LVDS GND	I	3	Ground Pins for LVDS Input
V <sub>CC</sub>	I	4	Power Supply for LVTTTL Output
GND	I	5	Ground Pins for LVTTTL Output

## Transmitter and Receiver Power-Up / Power-Down Operation Truth Tables

The outputs of the transmitter remain in the high-impedance state until the power supply reaches 2V. The following table shows the operation of the transmitter during power-up and power-down and operation of the /PwrDn pin.

### Transmitter

			PwrDn	Normal			
	V <sub>CC</sub>	<2V	>2V	>2V	>2V	>2V	>2V
	TxIN	Don't Care	Don't Care	Active	Active		
	TxOUT	High Impedance	High Impedance	Active	Don't Care		
	TxCLKIn	Don't Care	Don't Care	Active	LOW/HIGH/ High Impedance		
	TxCLKOut±	High Impedance	High Impedance	Active	Note 3		
	/PwrDn	LOW	LOW	HIGH	HIGH	HIGH	

#### Notes:

- If the transmitter is powered up, /PwrDn is inactive HIGH, and the clock input goes to any state LOW, HIGH, or high-impedance; the internal PLL goes to a known low frequency and stays until the clock starts normal operation again.

### Receiver

			/PwrDn				
	RxIn±	Don't Care	Don't Care	Active	Active	Note 4	Note 4
	RxOut	High Impedance	LOW	LOW/HIGH	Last Valid State	HIGH	Last Valid State
	RxCLKIn±	Don't Care	Don't Care	Active	Note 4	Note 4	Note 4
	RxCLKOut	High Impedance	Note 5	Active	Note 5	Note 5	Note 5
	/PwrDn	LOW	LOW	HIGH	HIGH	HIGH	HIGH
	V <sub>CC</sub>	<2V	<2V	<2V	<2V	<2V	<2V

#### Notes:

- If the input is terminated and un-driven (high-impedance) or shorted or open (fail-safe condition).
- For /PwrDn or fail-safe condition the RxCLKOut pin goes LOW for Panel Link devices and HIGH for channel link devices.
- Shorted means (± inputs are shorted to each other, or ± inputs are shorted to each other and ground or V<sub>CC</sub>, or either ± inputs are shorted to ground or V<sub>CC</sub>) with no other current/voltage sources (noise) applied. If the V<sub>ID</sub> is still in the valid range (greater than 100mV) and V<sub>CM</sub> is in the valid range (0V to 2.4V), the input signal is still recognized and the part responds normally.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
$V_{CC}$	Power Supply Voltage	-0.3	+4.6	V
$V_{ID\_TTL}$	TTL/CMOS Input/Output Voltage	-0.5	+4.6	V
$V_{IO\_LVDS}$	LVDS Input/Output Voltage	-0.3	+4.6	V
$I_{OSD}$	LVDS Output Short-Circuit Current	Continuous		
$T_{STG}$	Storage Temperature Range	-65	+150	°C
$T_J$	Maximum Junction Temperature		+150	°C
$T_L$	Lead Temperature, Soldering, 4 Seconds		+260	°C
ESD	Human Body Model, JESD22-A114 (1.5k $\Omega$ ,100pF)	I/O to GND	>10.0	kV
		All Pins	>6.5	
	Machine Model, JESD22-A115 (0 $\Omega$ , 200pF)	>400	V	

### Note:

- Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
$V_{CC}$	Supply Voltage	3.0	3.6	V
$T_A$	Operating Temperature	-10	+70	°C
$V_{CCNPP}$	Maximum Supply Noise Voltage <sup>(8)</sup>		100	mV <sub>PP</sub>

### Note:

- 100mV  $V_{CC}$  noise should be tested for frequency at least up to 2MHz. All the specifications should be met under such a noise.

## Transmitter DC Electrical Characteristics

Typical values are at  $T_A=25^\circ\text{C}$  and with  $V_{CC}=3.3\text{V}$ ; minimum and maximum are at over supply voltages and operating temperatures ranges, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	
<b>Transmitter LVTTTL Input Characteristics</b>							
$V_{IH}$	Input HIGH Voltage		2.0		$V_{CC}$	V	
$V_{IL}$	Input LOW Voltage		GND		0.8	V	
$V_{IK}$	Input Clamp Voltage	$I_{IK}=-18\text{mA}$		-0.79	-1.50	V	
$I_{IN}$	Input Current	$V_{IN}=0.4\text{V to }4.6\text{V}$		1.8	10.0	$\mu\text{A}$	
		$V_{IN}=\text{GND}$	-10	0			
<b>Transmitter LVDS Output Characteristics<sup>(9)</sup></b>							
$V_{OD}$	Output Differential Voltage	$R_L=100\Omega$ , Figure 5	250		450	mV	
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change from Differential LOW-to-HIGH				35	mV	
$V_{OS}$	Offset Voltage		1.125	1.250	1.375	V	
$\Delta V_{OS}$	Offset Magnitude Change from Differential LOW-to-HIGH			25		mV	
$I_{OS}$	Short-Circuit Output Current	$V_{OUT}=0\text{V}$		-3.5	-5.0	mA	
$I_{OZ}$	Disabled Output Leakage Current	$DO=0\text{V to }4.6\text{V}$ , $/PwrDn=0\text{V}$		$\pm 1$	$\pm 10$	$\mu\text{A}$	
<b>Transmitter Supply Current</b>							
$I_{CCWT}$	28:4 Transmitter Power Supply Current for Worst-Case Pattern (with Load) <sup>(10)</sup>	$R_L=100\Omega$ Figure 8	32.5MHz		31.0	49.5	mA
			40MHz		32.0	55.0	
			66MHz		37.0	60.5	
			85MHz		42.0	66.0	
$I_{CCPDT}$	Powered-Down Supply Current	$/PwrDn=0.8\text{V}$		10.0	55.0	$\mu\text{A}$	
$I_{CCGT}$	28:4 Transmitter Supply Current for 16 Grayscale <sup>(10)</sup>	Figure 23 <sup>(11)</sup>	32.5MHz		29.0	41.8	mA
			40MHz		30.0	44.0	
			66MHz		35.0	49.5	
			85MHz		39.0	55.0	

### Notes:

9. Positive current values refer to the current flowing into device and negative values means current flowing out of pins. Voltages are referenced to ground unless otherwise specified (except  $\Delta V_{OD}$  and  $V_{OD}$ ).
10. The power supply current for both transmitter and receiver can vary with the number of active I/O channels.
11. The 16-grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical strips across the display.

## Transmitter AC Electrical Characteristics

Typical values are at  $T_A=25^\circ\text{C}$  and with  $V_{CC}=3.3\text{V}$ ; minimum and maximum are at over supply voltages and operating temperatures ranges, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{TCP}$	Transmit Clock Period	Figure 9	11.76	T	50.00	ns
$t_{TCH}$	Transmit Clock (TxCLKIn) HIGH Time		0.35	0.50	0.65	T
$t_{TCL}$	Transmit Clock LOW Time		0.35	0.50	0.65	T
$t_{CLKT}$	TxCLKIn Transition Time (Rising and Falling)	(10% to 90%) Figure 10	1.0		6.0	ns
$t_{JIT}$	TxCLKIn Cycle-to-Cycle Jitter				3.0	
$t_{XIT}$	TxIn Transition Time		1.5		6.0	ns

### LVDS Transmitter Timing Characteristics

$t_{TLH}$	Differential Output Rise Time (20% to 80%)	Figure 8		0.75	1.50	ns
$t_{THL}$	Differential Output Fall Time (20% to 80%)			0.75	1.50	ns
$t_{STC}$	TxIn Setup to TxCLNIn	Figure 9 $f=85\text{MHz}$	2.5			ns
$t_{HTC}$	TxIn Holds to TxCLNIn		0			ns
$t_{TPDD}$	Transmitter Power-Down Delay	Figure 14 <sup>(12)</sup>			100	ns
$t_{CCD}$	Transmitter Clock Input to Clock Output Delay	( $T_A=25^\circ\text{C}$ and with $V_{CC}=3.3\text{V}$ ) Figure 13	2.8	5.5	6.8	ns

### Transmitter Output Data Jitter ( $f=40\text{MHz}$ )<sup>(13)</sup>

$t_{TPPB0}$	Transmitter Output Pulse Position of Bit 0	Figure 20 $a = \frac{1}{f \times 7}$	-0.25	0	0.25	ns
$t_{TPPB1}$	Transmitter Output Pulse Position of Bit 1		a-0.25	a	a+0.25	ns
$t_{TPPB2}$	Transmitter Output Pulse Position of Bit 2		2a-0.25	2a	2a+0.25	ns
$t_{TPPB3}$	Transmitter Output Pulse Position of Bit 3		3a-0.25	3a	3a+0.25	ns
$t_{TPPB4}$	Transmitter Output Pulse Position of Bit 4		4a-0.25	4a	4a+0.25	ns
$t_{TPPB5}$	Transmitter Output Pulse Position of Bit 5		5a-0.25	5a	5a+0.25	ns
$t_{TPPB6}$	Transmitter Output Pulse Position of Bit 6		6a-0.25	6a	6a+0.25	ns

### Transmitter Output Data Jitter ( $f=65\text{MHz}$ )<sup>(13)</sup>

$t_{TPPB0}$	Transmitter Output Pulse Position of Bit 0	Figure 20 $a = \frac{1}{f \times 7}$	-0.2	0	0.2	ns
$t_{TPPB1}$	Transmitter Output Pulse Position of Bit 1		a-0.2	a	a+0.2	ns
$t_{TPPB2}$	Transmitter Output Pulse Position of Bit 2		2a-0.2	2a	2a+0.2	ns
$t_{TPPB3}$	Transmitter Output Pulse Position of Bit 3		3a-0.2	3a	3a+0.2	ns
$t_{TPPB4}$	Transmitter Output Pulse Position of Bit 4		4a-0.2	4a	4a+0.2	ns
$t_{TPPB5}$	Transmitter Output Pulse Position of Bit 5		5a-0.2	5a	5a+0.2	ns
$t_{TPPB6}$	Transmitter Output Pulse Position of Bit 6		6a-0.2	6a	6a+0.2	ns

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## Transmitter AC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified.

Transmitter Output Data Jitter (f=85MHz) <sup>(13)</sup>						
t <sub>TPPB0</sub>	Transmitter Output Pulse Position of Bit 0	Figure 20 $a = \frac{1}{f \times 7}$	-0.2	0	0.2	ns
t <sub>TPPB1</sub>	Transmitter Output Pulse Position of Bit 1		a-0.2	a	a+0.2	ns
t <sub>TPPB2</sub>	Transmitter Output Pulse Position of Bit 2		2a-0.2	2a	2a+0.2	ns
t <sub>TPPB3</sub>	Transmitter Output Pulse Position of Bit 3		3a-0.2	3a	3a+0.2	ns
t <sub>TPPB4</sub>	Transmitter Output Pulse Position of Bit 4		4a-0.2	4a	4a+0.2	ns
t <sub>TPPB5</sub>	Transmitter Output Pulse Position of Bit 5		5a-0.2	5a	5a+0.2	ns
t <sub>TPPB6</sub>	Transmitter Output Pulse Position of Bit 6		6a-0.2	6a	6a+0.2	ns
t <sub>JCC</sub>	FIN3385 Transmitter Clock Out Jitter, Cycle-to-Cycle Figure 20	f=40MHz		350	370	ps
		f=65MHz		210	230	
		f=85MHz		110	150	
t <sub>TPLLS</sub>	Transmitter Phase Lock Loop Set Time <sup>(14)</sup>	Figure 26 <sup>(13)</sup>			10	ms

### Notes:

12. Outputs of all transmitters stay in 3-STATE until power reaches 2V. Clock and data output begins to toggle 10ms after V<sub>CC</sub> reaches 3V and /PwrDn pin is above 1.5V.
13. This output data pulse position works for both transmitters for TTL inputs, except the LVDS output bit mapping difference (see Figure 18). Figure 20 shows the skew between the first data bit and clock output. A two-bit cycle delay is guaranteed when the MSB is output from transmitter.
14. This jitter specification is based on the assumption that PLL has a reference clock with cycle-to-cycle input jitter of less than 2ns.

## Receiver DC Electrical Characteristics

Typical values are at  $T_A=25^\circ\text{C}$  and with  $V_{CC}=3.3\text{V}$ . Minimum and maximum values are over supply voltage and operating temperature ranges unless otherwise specified. Positive current values refer to the current flowing into device and negative values means current flowing out of pins. Voltages are referenced to ground unless otherwise specified (except  $\Delta V_{OD}$  and  $V_{OD}$ ).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	
<b>LVTTTL/CMOS DC Characteristics</b>							
$V_{IH}$	Input High Voltage		2.0		$V_{CC}$	V	
$V_{IL}$	Input Low Voltage		GND		0.8	V	
$V_{OH}$	Output High Voltage	$I_{OH}=-0.4\text{mA}$	2.7	3.3		V	
$V_{OL}$	Output Low Voltage	$I_{OL}=2\text{mA}$		0.06	0.30	V	
$V_{IK}$	Input Clamp Voltage	$I_{IK}=-18\text{mA}$		-0.79	-1.50	V	
$I_{IN}$	Input Current	$V_{IN}=0\text{V}$ to 4.6V	-10		10	$\mu\text{A}$	
$I_{OFF}$	Input/Output Power-Off Leakage Current	$V_{CC}=0\text{V}$ , All LVTTTL Inputs / Outputs 0V to 4.6V			$\pm 10$	$\mu\text{A}$	
$I_{OS}$	Output Short-Circuit Current	$V_{OUT}=0\text{V}$		-60	-120	mA	
<b>Receiver LVDS Input Characteristics</b>							
$V_{TH}$	Differential Input Threshold HIGH	Figure 6, Table 2			100	mV	
$V_{TL}$	Differential Input Threshold LOW	Figure 6, Table 2	-100			mV	
$V_{ICM}$	Input Common Mode Range	Figure 6, Table 2	0.05		2.35	V	
$I_{IN}$	Input Current	$V_{IN}=2.4\text{V}$ , $V_{CC}=3.6\text{V}$ or 0V			$\pm 10$	$\mu\text{A}$	
		$V_{IN}=0\text{V}$ , $V_{CC}=3.6\text{V}$ or 0V			$\pm 10$		
<b>Receiver Supply Current</b>							
$I_{CCWR}$	4:28 Receiver Power Supply Current for Worst Case Pattern with Load <sup>(15)</sup>	$C_L=8\text{pF}$ , Figure 7	32.5MHz			70	mA
			40MHz			75	
			66MHz			114	
			85MHz			135	
	3:21 Receiver Power Supply Current for Worst Case Pattern with Load <sup>(15)</sup>		32.5MHz		49	60	
			40MHz		53	65	
			66MHz		78	100	
			85MHz		90	115	
$I_{CCPDT}$	Powered-Down Supply Current	/PwrDn=0.8V (RxOut stays LOW)		NA	55	$\mu\text{A}$	

**Receiver DC Electrical Characteristics** (Continued)

Typical values are at  $T_A=25^\circ\text{C}$  and with  $V_{CC}=3.3\text{V}$ ; minimum and maximum are at over supply voltages and operating temperatures ranges, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{RCOP}$	Receiver Clock Output (RxCLKOut) Period		11.76	T	50.00	
$t_{RCOL}$	RxCLKOut LOW Time	Figure 12 Rising Edge Strobe $f=85\text{MHz}$	4.0	5.0	6.0	ns
$t_{RCOH}$	RxCLKOut HIGH Time		4.5	5.0	6.5	ns
$t_{RSRC}$	RxOut Valid Prior to RxCLKOut		3.5			ns
$t_{RHRC}$	RxOut Valid After RxCLKOut		3.5			ns
$t_{ROLH}$	Output Rise Time (20% to 80%)	$C_L=8\text{pF}$ , Figure 8		2.0	3.5	ns
$t_{ROHL}$	Output Rise Time (80% to 20%)			1.8	3.5	
$t_{RCCD}$	Receiver Clock Input to Clock Output Delay <sup>(16)</sup>	$T_A=25^\circ\text{C}$ and $V_{CC}=3.3\text{V}$ Figure 24	3.5	5.0	7.5	ns
$t_{RPPD}$	Receiver Power-Down Delay	Figure 17			1.0	$\mu\text{s}$
$t_{RSPB0}$	Receiver Input Strobe Position of Bit 0	Figure 21 $f=85\text{MHz}$	0.49	0.84	1.19	ns
$t_{RSPB1}$	Receiver Input Strobe Position of Bit 1		2.17	2.52	2.87	ns
$t_{RSPB2}$	Receiver Input Strobe Position of Bit 2		3.85	4.20	4.55	ns
$t_{RSPB3}$	Receiver Input Strobe Position of Bit 3		5.53	5.88	6.23	ns
$t_{RSPB4}$	Receiver Input Strobe Position of Bit 4		7.21	7.56	7.91	ns
$t_{RSPB5}$	Receiver Input Strobe Position of Bit 5		8.89	9.24	9.59	ns
$t_{RSPB6}$	Receiver Input Strobe Position of Bit 6		10.57	10.92	11.27	ns
$t_{RSKM}$	RxIN Skew Margin <sup>(17)</sup>	Figure 21	290			ps
$t_{RPLLS}$	Receiver Phase Lock Loop Set Time	Figure 21		10		ms

**Notes:**

15. The power supply current for the receiver can be different with the number of I/O channels.
16. Total channel latency from serializer to deserializer is  $(T + t_{RCCD})$ . There is a clock period.
17. Receiver skew margin is defined as the valid sampling window after considering potential setup/hold time and minimum/maximum bit position.

### Receiver AC Electrical Characteristics (66MHz)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t <sub>RCOP</sub>	Receiver Clock Output (RxCLKOut) Period	Figure 12	15	T	50	ns
t <sub>RCOL</sub>	RxCLKOut LOW Time	Figure 12 Rising Edge Strobe f=40MHz	10.0	11.0		ns
t <sub>RCOH</sub>	RxCLKOut HIGH Time		10.0	12.2		
t <sub>RSRC</sub>	RxOUT Valid Prior to RxCLKOut		6.5	11.6		
t <sub>RHRC</sub>	RxOUT Valid After RxCLKOut		6.0	11.6		
t <sub>RCOL</sub>	RxCLKOut LOW Time	Figure 12 Rising Edge Strobe <sup>(18)</sup> f=66MHz	5.0	6.3	9.0	ns
t <sub>RCOH</sub>	RxCLKOut HIGH Time		5.0	7.6	9.0	
t <sub>RSRC</sub>	RxOUT Valid Prior to RxCLKOut		4.5	7.3		
t <sub>RHRC</sub>	RxOUT Valid After RxCLKOut		4.0	6.3		
t <sub>ROLH</sub>	Output Rise Time (20% to 80%)	C <sub>L</sub> =8pF <sup>(18)</sup>		2.0	5.0	ns
t <sub>ROHL</sub>	Output Fall Time (20% to 80%)	Figure 12		1.8	5.0	
t <sub>RCCD</sub>	Receiver Clock Input to Clock Output Delay <sup>(19)</sup>	Figure 14 T <sub>A</sub> =25°C and V <sub>CC</sub> =3.3v	3.5	5.0	7.5	ns
t <sub>RPDD</sub>	Receiver Power-Down Delay	Figure 17			1.0	μs
t <sub>RSPB0</sub>	Receiver Input Strobe Position of Bit 0	Figure 21 f=40MHz	1.00	1.40	2.15	ns
t <sub>RSPB1</sub>	Receiver Input Strobe Position of Bit 1		4.5	5.0	5.8	
t <sub>RSPB2</sub>	Receiver Input Strobe Position of Bit 2		8.10	8.50	9.15	
t <sub>RSPB3</sub>	Receiver Input Strobe Position of Bit 3		11.6	11.9	12.6	
t <sub>RSPB4</sub>	Receiver Input Strobe Position of Bit 4		15.1	15.6	16.3	
t <sub>RSPB5</sub>	Receiver Input Strobe Position of Bit 5		18.8	19.2	19.9	
t <sub>RSPB6</sub>	Receiver Input Strobe Position of Bit 6		22.5	22.9	23.6	
t <sub>RSPB0</sub>	Receiver Input Strobe Position of Bit 0	Figure 21 f=66MHz	0.7	1.1	1.4	ns
t <sub>RSPB1</sub>	Receiver Input Strobe Position of Bit 1		2.9	3.3	3.6	
t <sub>RSPB2</sub>	Receiver Input Strobe Position of Bit 2		5.1	5.5	5.8	
t <sub>RSPB3</sub>	Receiver Input Strobe Position of Bit 3		7.3	7.7	8.0	
t <sub>RSPB4</sub>	Receiver Input Strobe Position of Bit 4		9.5	9.9	10.2	
t <sub>RSPB5</sub>	Receiver Input Strobe Position of Bit 5		11.7	12.1	12.4	
t <sub>RSPB6</sub>	Receiver Input Strobe Position of Bit 6		13.9	14.3	14.6	
t <sub>RSKM</sub>	RxIn Skew Margin <sup>(20)</sup>	f=40MHz, Figure 21	490			ps
		f=66MHz, Figure 21	400			
t <sub>RPLLS</sub>	Receiver Phase Lock Loop Set Time	Figure 15			10.0	ms

**Notes:**

18. For the receiver with falling-edge strobe, the definition of setup/hold time is slightly different from the one with rising-edge strobe. The clock reference point is the time when the clock falling edge passes through 2V. For hold time t<sub>RHRC</sub>, the clock reference point is the time when falling edge passes through +0.8V.
19. Total channel latency from serializer to deserializer is (T + t<sub>RCCD</sub>) (2•T + t<sub>RCCD</sub>). There is the clock period.
20. Receiver skew margin is defined as the valid sampling window after considering potential setup/hold time and minimum / maximum bit position.

## Test Circuits

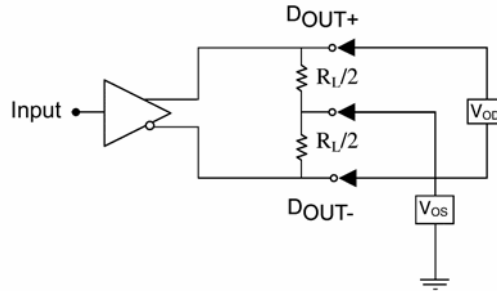
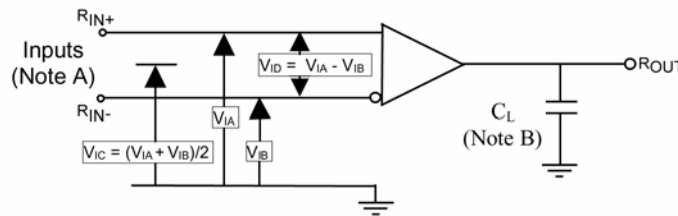


Figure 5. Differential LVDS Output DC Test Circuit



**Notes:**

- A: For all input pulses,  $t_R$  or  $t_F \leq 1$  ns.
- B:  $C_L$  includes all probe and jig capacitance.

Figure 6. Differential Receiver Voltage Definitions, Propagation Delay, and Transition Time Test Circuit

Table 2. Receiver Minimum and Maximum Input Threshold Test Voltages

Applied Voltages (V)		Resulting Differential Input Voltage (mV)	Resulting Common Mode Input Voltage (V)
$V_{IA}$	$V_{IB}$	$V_{ID}$	$V_{ICM}$
1.25	1.15	100	1.20
1.15	1.25	-100	1.20
2.40	2.30	100	2.35
2.30	2.40	-100	2.35
0.10	0	100	0.05
0	0.10	-100	0.05
1.50	0.90	600	1.20
0.90	1.50	-600	1.20
2.40	1.80	600	2.10
1.80	2.40	-600	2.10
0.60	0	600	0.30
0	0.60	-600	0.30

## AC Loadings and Waveforms

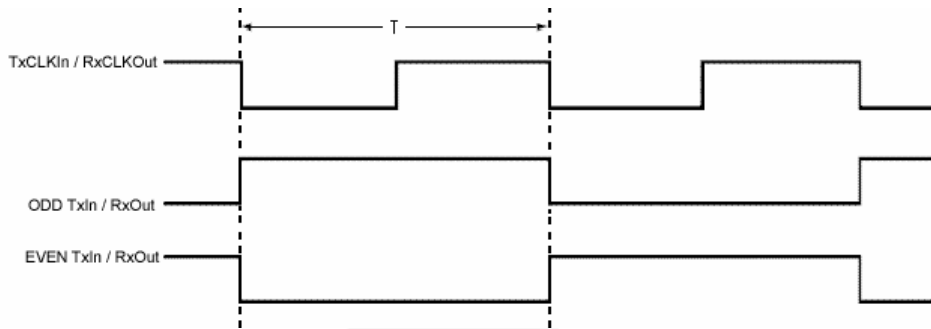


Figure 7. Worst-Case Test Pattern

**Note:**

21. The worst-case test pattern produces a maximum toggling of digital circuits, LVDS I/O, and LVTTTL/CMOS I/O. Depending on the valid strobe edge of transmitter, the TxCLKIn can be either rising or falling edge data strobe.

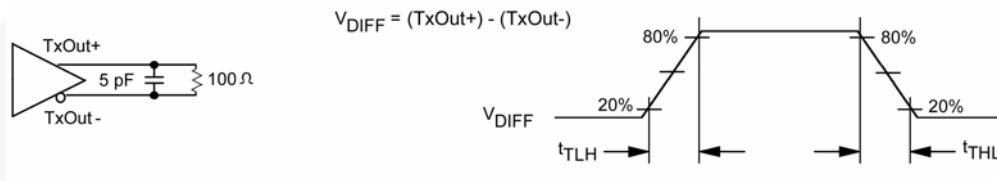


Figure 8. Transmitter LVDS Output Load and Transition Times

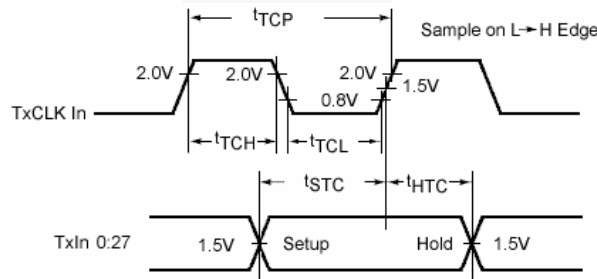


Figure 9. Transmitter Setup/Hold and HIGH/LOW Times (Rising-Edge Strobe)

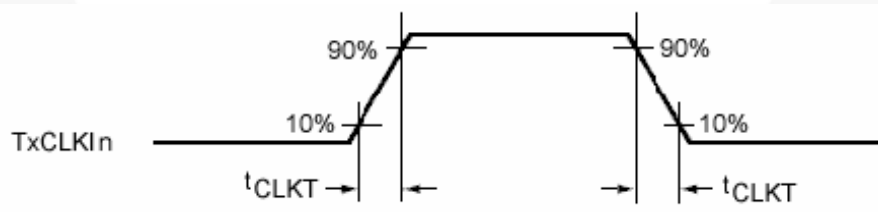


Figure 10. Transmitter Input Clock Transition Time

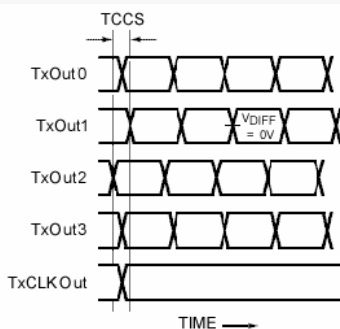
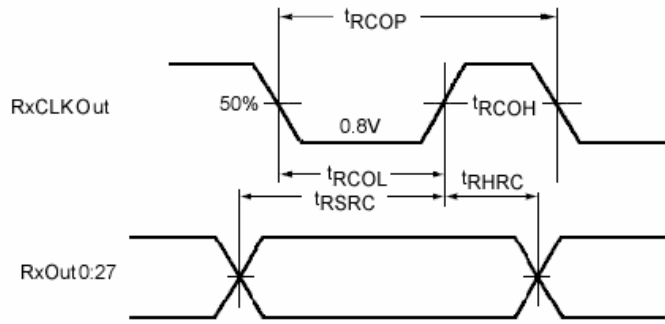


Figure 11. Transmitter Outputs Channel-to-Channel Skew

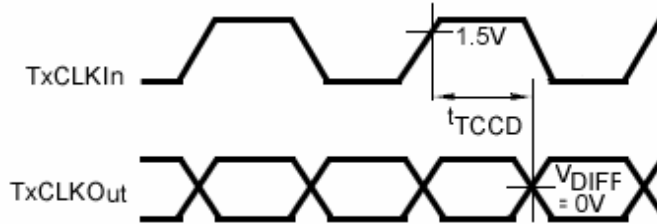
### AC Loadings and Waveforms (Continued)



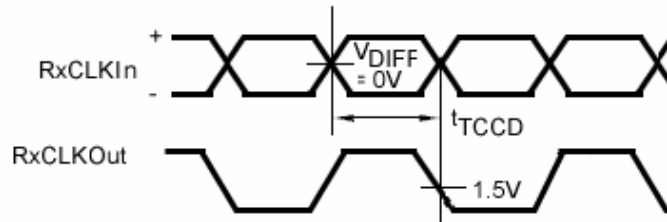
**Figure 12. Receiver Setup/Hold and HIGH/LOW Times**

**Note:**

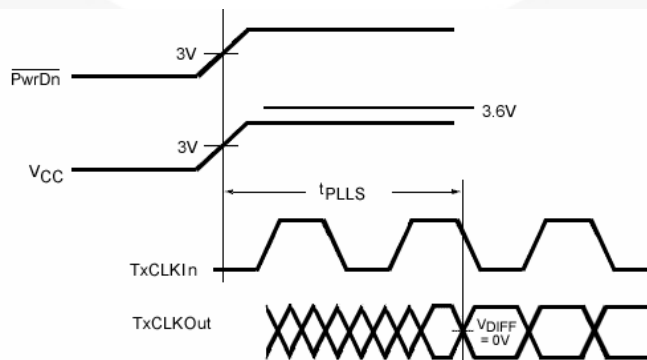
22. For the receiver with falling-edge strobe, the definition of setup/hold time is slightly different from the one with rising-edge strobe. The clock reference point is the time when the clock falling edge passes through 2V. For hold time  $t_{RHRC}$ , the clock reference point is the time when falling edge passes through +0.8V.



**Figure 13. Transmitter Clock-In to Clock-Out Delay (Rising-Edge Strobe)**

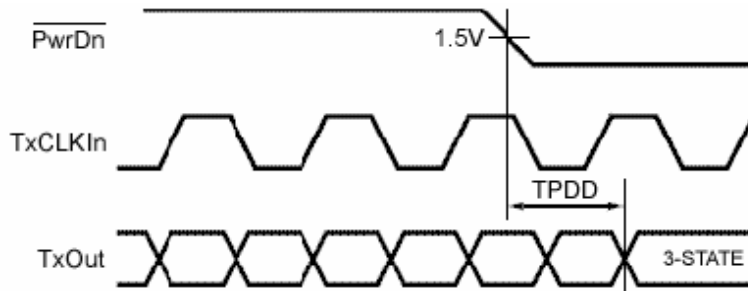


**Figure 14. Receiver Clock-In to Clock-Out Delay (Falling-Edge Strobe)**

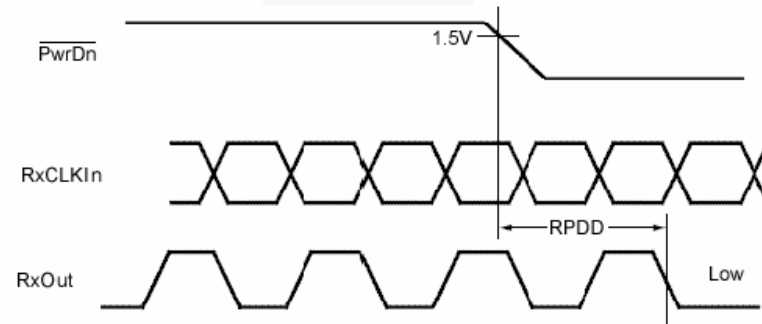


**Figure 15. Receiver Phase Lock Loop Set Time**

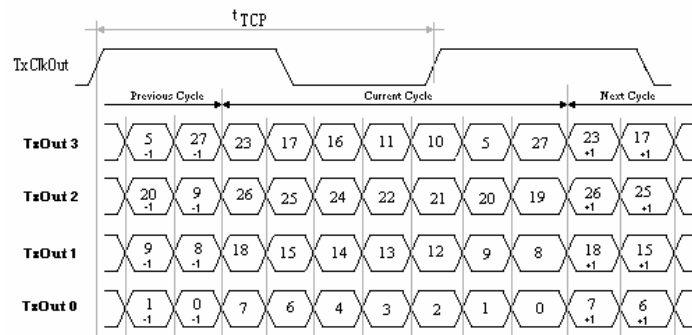
**AC Loadings and Waveforms (Continued)**



**Figure 16. Transmitter Power-down Delay**



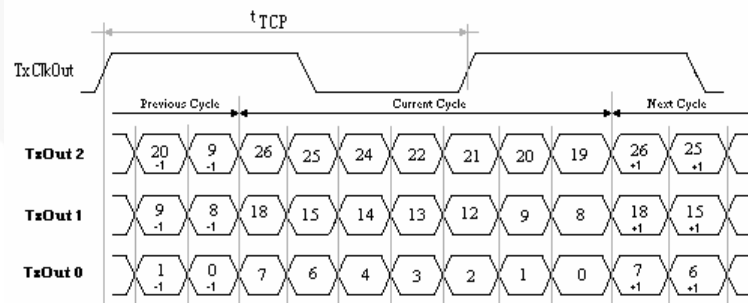
**Figure 17. Receiver Power-Down Delay**



**Figure 18. 28 Parallel LVTTTL Inputs Mapped to Four Serial LVDS Outputs**

**Note:**

23. The information in this diagram shows the difference between clock out and the first data bit. A 2-bit cycle delay is guaranteed when the MSB is output from the transmitter.



**Figure 19. 21 Parallel LVTTTL Inputs Mapped to Three Serial Outputs**

**Note:**

24. This output data pulse position works for both transmitters with 21 TTL inputs, except the LVDS output bit mapping difference. Two-bit cycle delay is guaranteed with the MSB is output from transmitter.



## AC Loadings and Waveforms (Continued)

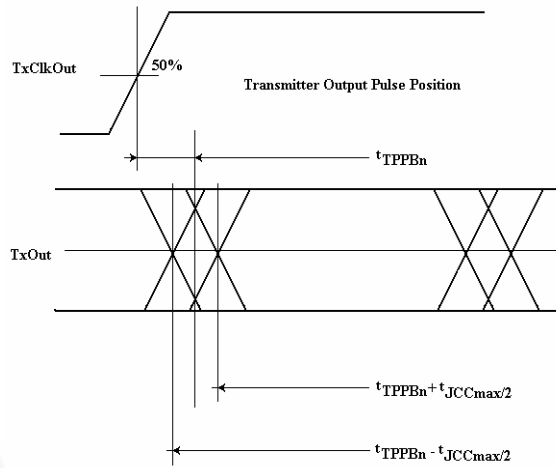


Figure 20. Transmitter Output Pulse Bit Position

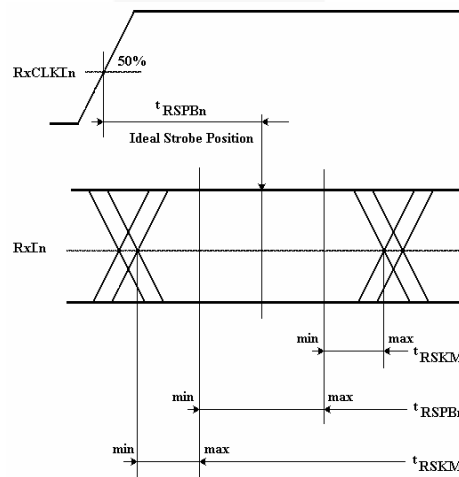


Figure 21. Receiver Input Bit Position

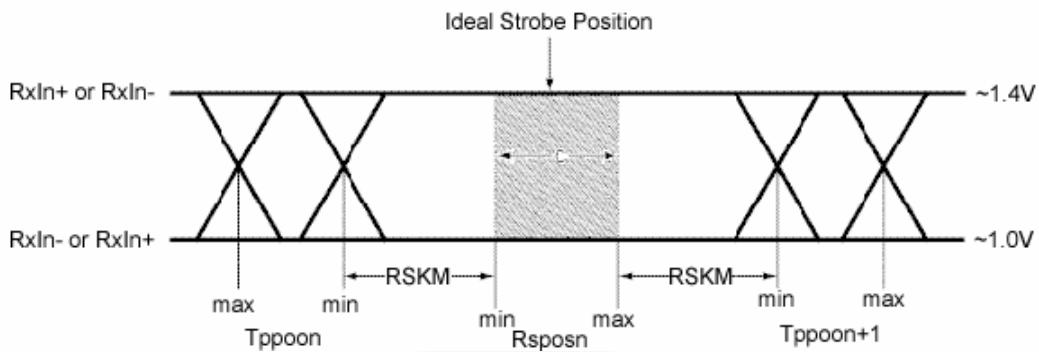
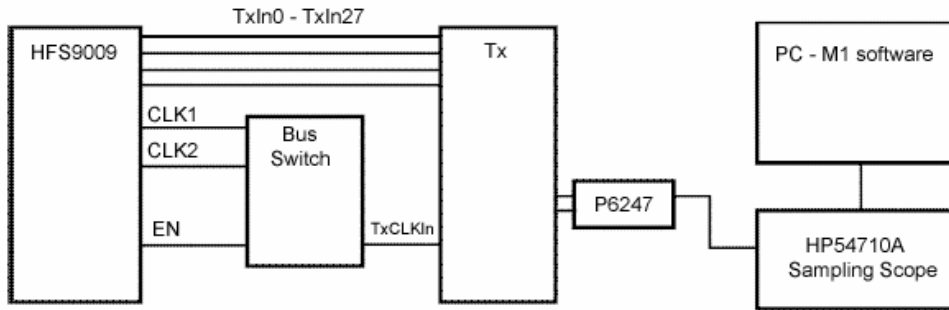


Figure 22. Receiver LVDS Input Skew Margin

**Note:**

25.  $t_{RSKM}$  is the budget for the cable skew and source clock skew plus Inter-Symbol Interference (ISI). The minimum and maximum pulse position values are based on the bit position of each of the seven bits within the LVDS data stream across PVT (Process, Voltage Supply, and Temperature).

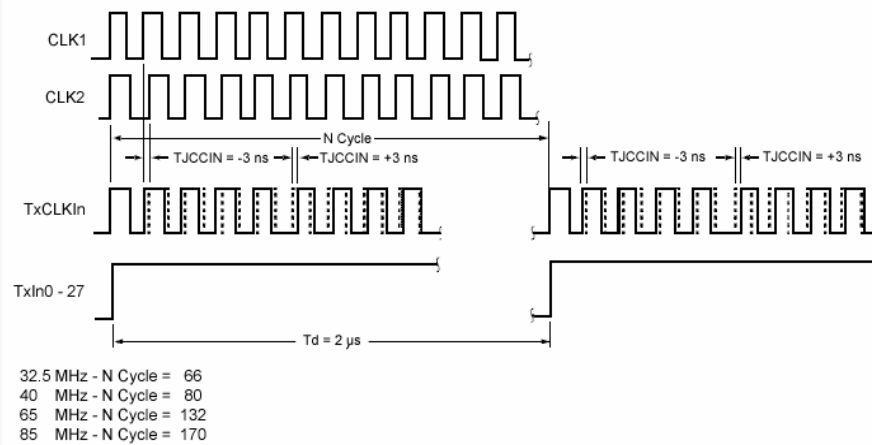
## AC Loadings and Waveforms (Continued)



**Figure 23. Transmitter Clock Out Jitter Measurement Setup**

**Note:**

26. Test setup used considers no requirement for separation of RMS and deterministic jitter. Other hardware setup, such as Wavecrest boxes, can be used if no M1 software is available, but the test methodology in Figure 24 should be followed.

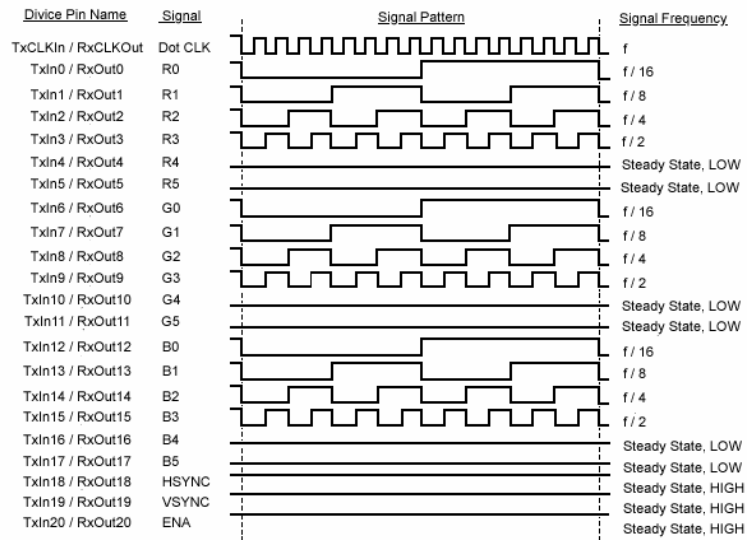


**Figure 24. Timing Diagram of Transmitter Clock Input with Jitter**

**Note:**

27. This jitter pattern is used to test the jitter response (clock out) of the device over the power supply range with worst jitter  $\pm 3\text{ns}$  (cycle-to-cycle) clock input. The specific test methodology is as follows:
28. Switching input data TxIn0 to TxIn20 at 0.5MHz and the input clock is shifted to left -3ns and to the right +3ns when data is HIGH.
29. The  $\pm 3\text{ns}$  cycle-to-cycle input jitter is the static phase error between the two clock sources. Jumping between two clock sources to simulate the worst-case of clock-edge jump (3ns) from graphical controllers. Cycle-to-cycle jitter at TxCLKOut pin should be measured cross  $V_{CC}$  range with 100mV noise ( $V_{CC}$  noise frequency  $< 2\text{MHz}$ ).

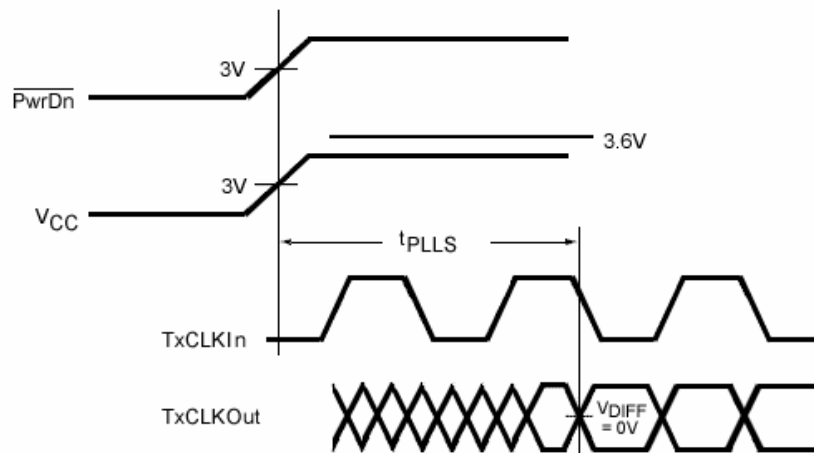
## AC Loadings and Waveforms (Continued)



**Figure 25. "16 Grey-Scale" Test Pattern**

**Note:**

30. The 16-grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical strips across the display.



**Figure 26. Transmitter Phase-Lock-Loop Time**

## Physical Dimensions

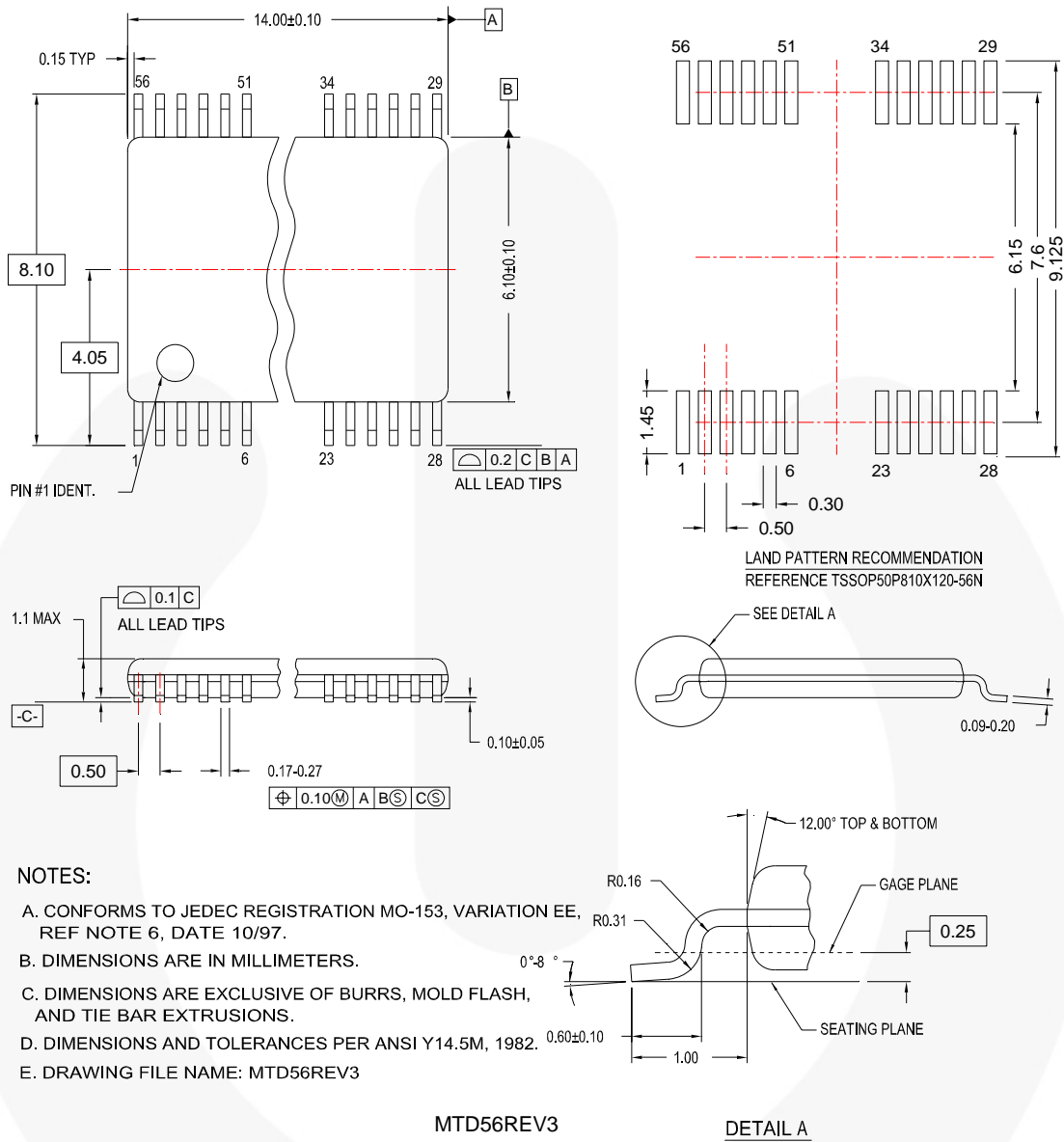


Figure 27. 56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide





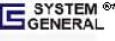
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