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74AC646 • 74ACT646 Octal Transceiver/Register with 3-STATE Outputs

General Description

The AC/ACT646 consist of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CPAB or CPBA). The four fundamental data handling functions available are illustrated in Figures 1, 2, 3, and Figure 4.

Features

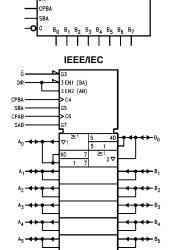
- Independent registers for A and B buses
- Multiplexed real-time and stored data transfers
- 3-STATE outputs
- 300 mil dual-in-line package
- Outputs source/sink 24 mA
- ACT646 has TTL compatible inputs

Ordering Code:

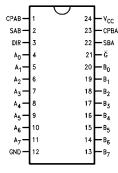
Order Number	Package Number	Package Description
74AC646SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74AC646SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
74ACT646SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74ACT646SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Pin Descriptions

Pin Names	Description
A ₀ -A ₇	Data Register A Inputs
	Data Register A Outputs
B ₀ -B ₇	Data Register B Inputs
	Data Register B Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
G	Output Enable Input
DIR	Direction Control Input

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DS010132

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Function Table

		Inp	uts			Data I/O	(Note 1)	
G	DIR	СРАВ	СРВА	SAB	SBA	A ₀ -A ₇	B ₀ -B ₇	Function
Н	Х	H or L	H or L	Х	Х			Isolation
Н	Χ	~	Χ	X	Χ	Input	Input	Clock A _n Data into A Register
Н	Χ	Χ	~	X	Χ			Clock B _n Data into B Register
L	Н	Х	Х	L	Х		A _n to B _n —Real Time (Transparent Mode	
L	Н	~	Χ	L	Χ	Input	Output	Clock A _n Data into A Register
L	Н	H or L	Χ	Н	Χ			A Register to B _n (Stored Mode)
L	Н	~	Χ	Н	Χ			Clock A _n Data into A Register and Output to B _n
L	L	Х	Х	Х	L			B _n to A _n —Real Time (Transparent Mode)
L	L	Χ	~	Х	L	Output	Input	Clock B _n Data into B Register
L	L	Χ	H or L	X	Н			B Register to A _n (Stored Mode)
L	L	Х	~	Х	Н			Clock B _n Data into B Register and Output to A _n

H = HIGH Voltage Level L = LOW Voltage Level

Note 1: The data output functions may be enabled or disabled by various signals at the \overline{G} and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

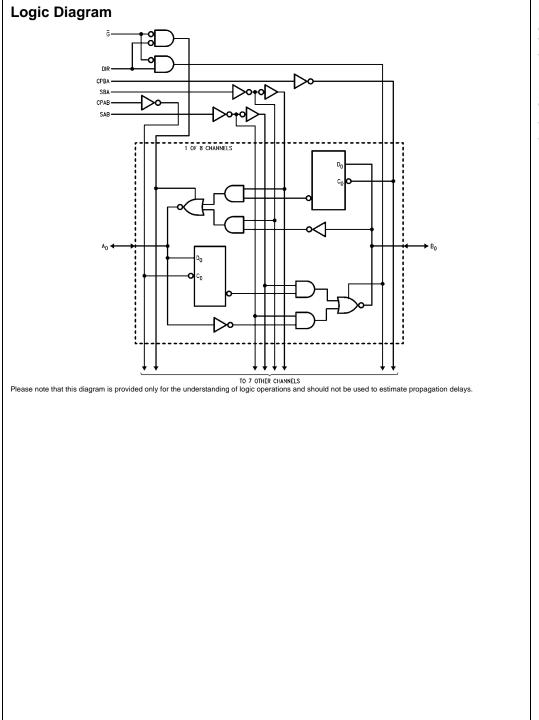
Real Time Transfer Real Time Transfer A-Bus to B-Bus B-Bus to A-Bus A-Bus A-Bus REG B-Bus B-Bus FIGURE 1. FIGURE 2. Storage from Transfer from Bus to Register Register to Bus A-Bus A-Bus REG REG REG B-Bus B-Bus

REG

OR REG

FIGURE 4.

FIGURE 3.



Absolute Maximum Ratings(Note 2)

 $\begin{array}{c} \text{V}_{\text{I}} = -0.5 \text{V} & -20 \text{ mA} \\ \text{V}_{\text{I}} = \text{V}_{\text{CC}} + 0.5 \text{V} & +20 \text{ mA} \\ \text{DC Input Voltage (V}_{\text{I}}) & -0.5 \text{V to V}_{\text{CC}} + 0.5 \text{V} \end{array}$

DC Output Diode Current (I_{OK})

 $V_{O} = -0.5V$ -20 mA $V_{O} = V_{CC} + 0.5V$ +20 mA

DC Output Voltage (V_O) $-0.5 \text{V to V}_{\text{CC}} + 0.5 \text{V}$

DC Output Source

or Sink Current (I_O) $\pm 50 \text{ mA}$

DC V_{CC} or Ground Current

per Output Pin (I_{CC} or I_{GND}) ± 50 mA Storage Temperature (T_{STG}) -65° C to +150 $^{\circ}$ C Junction Temperature (T_{J})

PDIP 140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})

AC 2.0V to 6.0V

ACT 4.5V to 5.5V

Input Voltage (V₁) 0V to V_{CC}

Output Voltage (V₂) 0V to V₂

Output Voltage (V_O) 0V to V_{CC} Operating Temperature (T_A) -40°C to +85°C

Minimum Input Edge Rate $(\Delta V/\Delta t)$

AC Devices

 $V_{\mbox{\footnotesize{IN}}}$ from 30% to 70% of $V_{\mbox{\footnotesize{CC}}}$

 $V_{CC} @ 3.3V, 4.5V, 5.5V$ 125 mV/ns

Minimum Input Edge Rate ($\Delta V/\Delta t$)

ACT Devices

 V_{IN} from 0.8V to 2.0V

V_{CC} @ 4.5V, 5.5V 125 mV/ns

140°C Note 2: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for AC

Symbol	Parameter	V _{CC}	T _A =	+25°C	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	Units	Conditions
Symbol	Parameter	(V)	Тур	Gu	aranteed Limits	Units	Conditions
V _{IH}	Minimum HIGH Level	3.0	1.5	2.1	2.1		V _{OUT} = 0.1V
	Input Voltage	4.5	2.25	3.15	3.15	V	or V _{CC} – 0.1V
		5.5	2.75	3.85	3.85		
V _{IL}	Maximum LOW Level	3.0	1.5	0.9	0.9		V _{OUT} = 0.1V
	Input Voltage	4.5	2.25	1.35	1.35	V	or V _{CC} – 0.1V
		5.5	2.75	1.65	1.65		
V _{OH}	Minimum HIGH Level	3.0	2.99	2.9	2.9		
	Output Voltage	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50 \mu A$
		5.5	5.49	5.4	5.4		
							$V_{IN} = V_{IL}$ or V_{IH}
		3.0		2.56	2.46		$I_{OH} = -12 \text{ mA}$
		4.5		3.86	3.76	V	$I_{OH} = -24 \text{ mA}$
		5.5		4.86	4.76		$I_{OH} = -24 \text{ mA (Note 3)}$
V _{OL}	Maximum LOW Level	3.0	0.002	0.1	0.1		
	Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50 \mu A$
		5.5	0.001	0.1	0.1		
							$V_{IN} = V_{IL}$ or V_{IH}
		3.0		0.36	0.44		I _{OH} = 12 mA
		4.5		0.36	0.44	V	$I_{OL} = 24 \text{ mA}$
		5.5		0.36	0.44		I _{OH} = 24 mA (Note 3)
I _{IN} (Note 5)	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μΑ	$V_I = V_{CC}$, GND
I _{OLD}	Minimum Dynamic	5.5			75	mA	V _{OLD} = 1.65V Max
I _{OHD}	Output Current (Note 4)	5.5			-75	mA	V _{OHD} = 3.85V Min
I _{CC} (Note 5)	Maximum Quiescent Supply Current	5.5		8.0	80.0	μΑ	$V_{IN} = V_{CC}$ or GND
I _{OZT}	Maximum I/O						V_{I} (OE) = V_{IL} , V_{IH}
	Leakage Current	5.5		±0.6	±6.0	μΑ	$V_I = V_{CC}$, GND
							$V_O = V_{CC}$, GND

Note 3: All outputs loaded; thresholds on input associated with output under test.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

Note 5: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} .

Symbol	Parameter Minimum HIGH Level	V _{CC}	$T_A = +25^{\circ}C$		$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	Units	Conditions
Symbol		(V)	Тур	Gu	aranteed Limits	Units	Conditions
V _{IH}		4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1V
	Input Voltage	5.5	1.5	2.0	2.0	V	or V _{CC} – 0.1V
V _{IL}	Maximum LOW Level	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1V
	Input Voltage	5.5	1.5	0.8	0.8	V	or $V_{CC} - 0.1V$
V _{OH}	Minimum HIGH Level	4.5	4.49	4.4	4.4	V	I _{OUT} = -50 μA
	Output Voltage	5.5	5.49	5.4	5.4	V	
							$V_{IN} = V_{IL}$ or V_{IH}
		4.5		3.86	3.76	V	I _{OH} = -24 mA
		5.5		4.86	4.76		I _{OH} = -24 mA (Note 6
V _{OL}	Maximum LOW Level	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA
	Output Voltage	5.5	0.001	0.1	0.1	V	100T = 50 μΑ
							$V_{IN} = V_{IL}$ or V_{IH}
		4.5		0.36	0.44	V	I _{OL} = 24 mA
		5.5		0.36	0.44		I _{OL} = 24 mA (Note 6
I _{IN}	Maximum Input	5.5		± 0.1	± 1.0	μА	$V_I = V_{CC}$, GND
	Leakage Current	5.5		± 0.1	± 1.0	μΛ	VI = VCC, GND
I _{CCT}	Maximum	5.5	0.6		1.5	mA	$V_{I} = V_{CC} - 2.1V$
	I _{CC} /Input	5.5	0.0		1.5	IIIA	v1 = vCC = 2.1v
I _{OLD}	Minimum Dynamic	5.5			75	mA	V _{OLD} = 1.65V Max
I _{OHD}	Output Current (Note 7)	5.5			-75	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent	5.5		8.0	80.0	μА	$V_{IN} = V_{CC}$
	Supply Current	3.3		0.0	00.0	μΛ	or GND
I _{OZT}	Maximum I/O						V_{I} (OE) = V_{IL} , V_{IH}
	Leakage Current	5.5		±0.6	±6.0	μΑ	$V_I = V_{CC}$, GND
		1					$V_O = V_{CC}$, GND

Note 6: All outputs loaded; thresholds on input associated with output under test.

Note 7: Maximum test duration 2.0 ms, one output loaded at a time.

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Ò				Vcc	

		V _{CC}		T _A = +25°C		T _A = -40°		
Symbol	Parameter	(V)		C _L = 50 pF		C _L =	50 pF	Units
		(Note 8)	Min	Тур	Max	Min	Max	
t _{PLH}	Propagation Delay	3.3	4.0	10.5	16.5	3.0	18.5	
	Clock to Bus	5.0	2.5	7.5	12.0	2.0	13.0	ns
t _{PHL}	Propagation Delay	3.3	3.0	9.5	14.5	2.5	16.0	
	Clock to Bus	5.0	2.0	6.5	10.5	1.5	11.5	ns
t _{PLH}	Propagation Delay	3.3	2.5	7.5	12.0	2.0	13.5	
	Bus to Bus	5.0	1.5	5.0	8.0	1.0	9.0	ns
t _{PHL}	Propagation Delay	3.3	1.5	7.5	12.5	1.5	13.5	
	Bus to Bus	5.0	1.5	5.0	9.0	1.0	9.5	ns
t _{PLH}	Propagation Delay	3.3	2.0	8.5	13.5	1.5	15.5	
	SBA or SAB to A _n or B _n	5.0	1.5	6.0	10.0	1.5	11.0	ns
	(w/ A _n or B _n HIGH or LOW)							
t _{PHL}	Propagation Delay	3.3	1.5	8.5	13.5	1.5	15.0	
	SBA or SAB to A _n or B _n	5.0	1.5	6.0	10.0	1.5	11.0	ns
	(w/ A _n or B _n HIGH or LOW)							
t _{PZH}	Enable Time	3.3	2.5	7.0	11.5	2.0	12.5	20
	G to A _n or B _n	5.0	1.5	5.0	8.5	1.5	9.0	ns
t _{PZL}	Enable Time	3.3	2.5	7.5	12.5	2.0	14.0	
	G to A _n or B _n	5.0	1.5	5.5	9.0	1.5	10.0	ns
t _{PHZ}	Disable Time	3.3	3.0	8.0	12.5	2.5	13.5	no
	G to A _n or B _n	5.0	2.0	6.5	10.0	2.0	11.0	ns
t _{PLZ}	Disable Time	3.3	2.0	7.5	12.0	2.0	13.5	ns
	G to A _n or B _n	5.0	1.5	6.0	9.5	1.5	10.5	115
t _{PZH}	Enable Time	3.3	2.0	6.5	11.0	1.5	12.0	
	DIR to A _n or B _n	5.0	1.5	5.0	7.5	1.0	8.5	ns
t _{PZL}	Enable Time	3.3	2.5	7.0	11.5	2.0	13.0	20
	DIR to A _n or B _n	5.0	1.5	5.0	8.0	1.0	9.0	ns
t _{PHZ}	Disable Time	3.3	2.5	7.5	11.5	1.5	12.5	no
	DIR to A _n or B _n	5.0	1.5	5.5	9.5	1.5	10.0	ns
t _{PLZ}	Disable Time	3.3	1.5	7.5	12.0	1.5	13.5	
	DIR to A _n or B _n	5.0	1.5	5.5	9.5	1.5	10.5	ns

Note 8: Voltage Range 3.3 is $3.3V \pm 0.3V$ Voltage Range 5.0 is 5.0V \pm 0.5V

AC Operating Requirements for AC

Symbol	Parameter	V _{CC} (V)	T _A = +25°C C _L = 50 pF		$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $C_L = 50 \text{ pF}$	Units	
		(Note 9)	Тур	Guai	ranteed Minimum		
t _S	Setup Time, HIGH or LOW	3.3	2.0	5.0	5.5	no	
	Bus to Clock	5.0	1.5	4.0	4.5	ns	
t _H	Hold Time, HIGH or LOW	3.3	-1.5	0	0	no	
	Bus to Clock	5.0	-0.5	0.5	1.0	ns	
t _W	Clock Pulse Width	3.3	2.0	3.5	4.5	ns	
	HIGH or LOW	5.0	2.0	3.5	3.5	115	

Note 9: Voltage Range 3.3 is 3.3V ± 0.3V Voltage Range 5.0 is 5.0V $\pm\,0.5\text{V}$

		V _{cc}		$T_A = +25^{\circ}C$		T _A = -40°		
Symbol	Parameter	(V)	C _L = 50 pF			C _L =	50 pF	Units
		(Note 10)	Min	Тур	Max	Min	Max	
t _{PLH}	Propagation Delay Clock to Bus	5.0	3.5	12.0	14.5	3.0	16.0	ns
PHL	Propagation Delay Clock to Bus	5.0	4.0	12.0	14.5	3.5	16.0	ns
PLH	Propagation Delay Bus to Bus	5.0	3.0	8.5	10.5	2.5	11.5	ns
t _{PHL}	Propagation Delay Bus to Bus	5.0	2.5	8.5	10.5	2.0	11.5	ns
^t PLH	Propagation Delay SBA or SAB to A _n to B _n (w/A _n or B _n , HIGH or LOW)	5.0	3.0	9.5	11.5	2.5	12.5	ns
PHL	Propagation Delay SBA or SAB to A _n to B _n (w/A _n or B _n , HIGH or LOW)	5.0	3.0	9.5	11.5	2.5	12.5	ns
t _{PZH}	Enable Time G to A _n or B _n	5.0	2.0	9.0	11.0	1.5	12.0	ns
PZL	Enable Time G to A _n or B _n	5.0	3.5	9.0	11.0	3.0	12.0	ns
PHZ	Disable Time G to A _n or B _n	5.0	5.0	10.5	13.0	4.5	14.5	ns
PLZ	Disable Time G to A _n or B _n	5.0	3.5	10.0	12.5	3.0	14.0	ns
PZH	Enable Time DIR to A _n or B _n	5.0	2.0	6.5	10.5	1.5	11.5	ns
PZL	Enable Time DIR to A _n or B _n	5.0	3.5	6.5	10.5	3.0	11.5	ns
PHZ	Disable Time DIR to A _n or B _n	5.0	5.0	8.5	12.5	4.5	13.5	ns
PLZ	Disable Time DIR to A _n or B _n	5.0	3.5	8.5	12.5	3.0	13.5	ns

Note 10: Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements for ACT

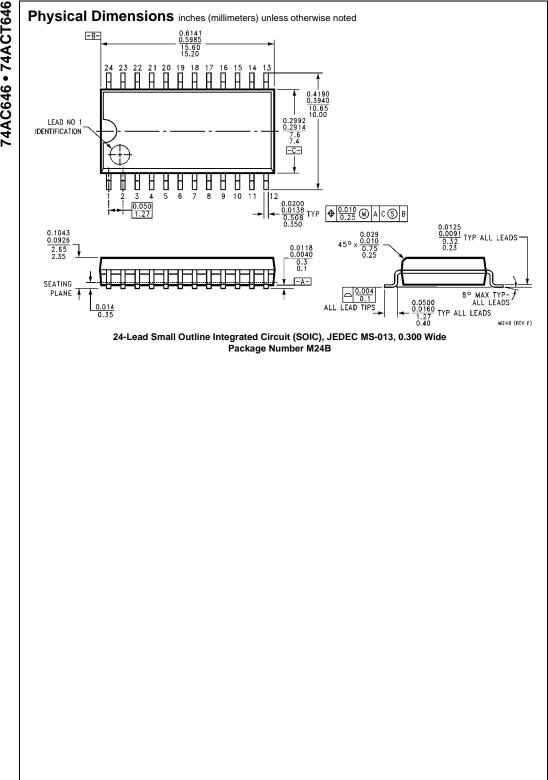
Symbol	Parameter	V _{CC} (V)	$T_A = +25^{\circ}C$ $C_L = 50 \text{ pF}$		$T_A = -40$ °C to +85°C $C_L = 50$ pF	Units
		(Note 11)	Тур	Gua	ranteed Minimum	
t _S	Setup Time, HIGH or LOW BUS to Clock	5.0	2.5	7.0	8.0	ns
t _H	Hold Time, HIGH or LOW Bus to Clock	5.0	0	2.5	2.5	ns
t _W	Clock Pulse Width HIGH or LOW	5.0	4.5	7.0	8.0	ns

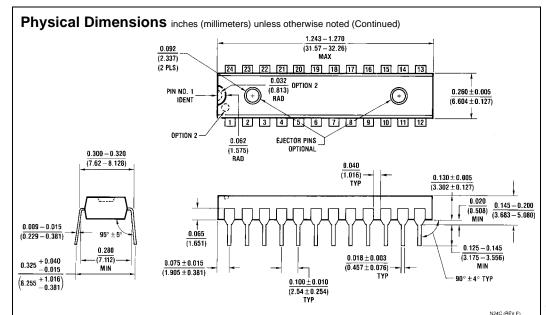
Note 11: Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Тур	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{I/O}	Input/Output Capacitance	15.0	pF	V _{CC} = 5.0V
C _{PD}	Power Dissipation Capacitance	60.0	pF	V _{CC} = 5.0V

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24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N24C

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