DATA SHEET

4G bits DDR2 Mobile RAM™ PoP (12mm × 12mm, 168-ball FBGA)

EDB4432BAPA

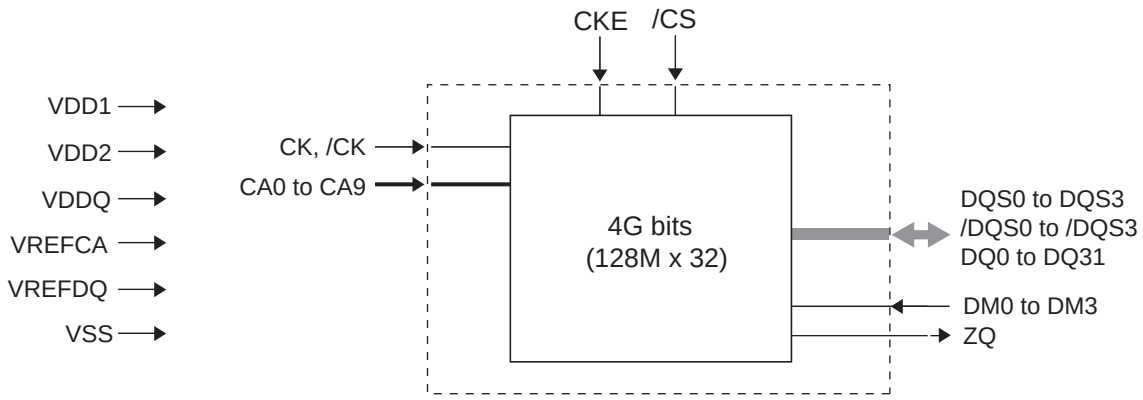
Specifications

- Density: 4G bits
- Organization
  - 16M words × 32 bits × 8 banks
- Data rate: 1066Mbps (max.)
- Package: 168-ball FBGA
  - Package size: 12.0mm × 12.0mm
  - Ball pitch: 0.5mm
  - Lead-free (RoHS compliant) and Halogen-free
- Power supply
  - VDD1 = 1.70V to 1.95V
  - VDD2, VDDQ = 1.14V to 1.30V
- Interface: HSUL_12
- Operating case temperature range
  - TC = -30°C to +85°C

Features

- JEDEC LPDDR2-S4B compliance
- DLL is not implemented
- Low power consumption
- Mobile RAM functions
  - Partial Array Self-Refresh (PASR)
  - Auto Temperature Compensated Self-Refresh (ATCSR) by built-in temperature sensor
  - Deep power-down mode
  - Per Bank Refresh
- This FBGA is suitable for Package on Package (PoP)

Block Diagram



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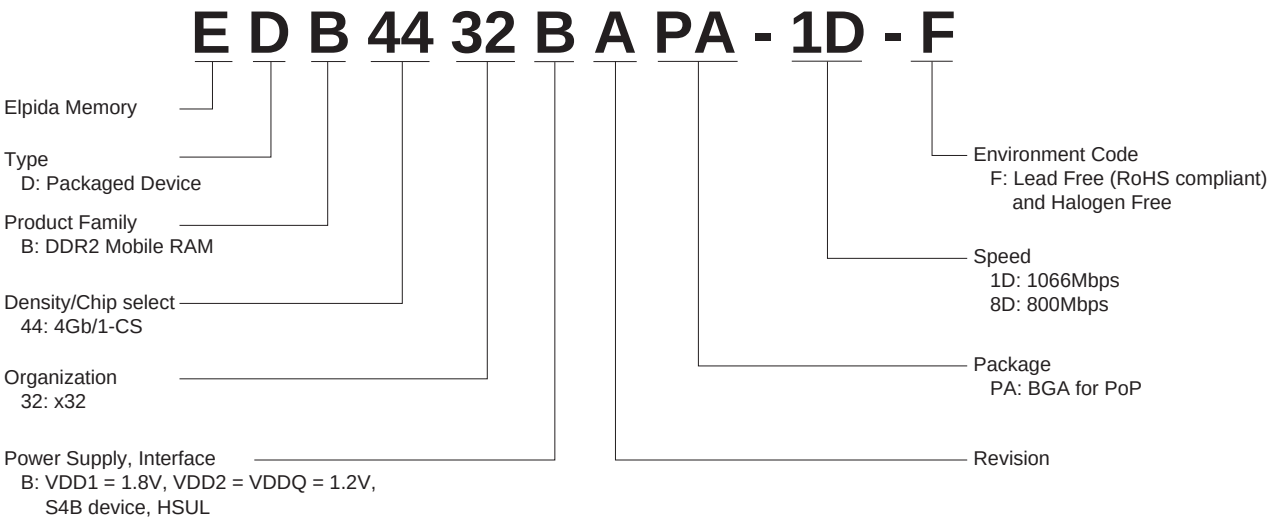
Ordering Information

Part number	Organization (words x bits)	Clock frequency	Data rate	Read latency	Package
EDB4432BAPA-1D-F	128M × 32	533MHz	1066Mbps	8	168-ball FBGA
EDB4432BAPA-8D-F		400MHz	800Mbps	6	

Part Number



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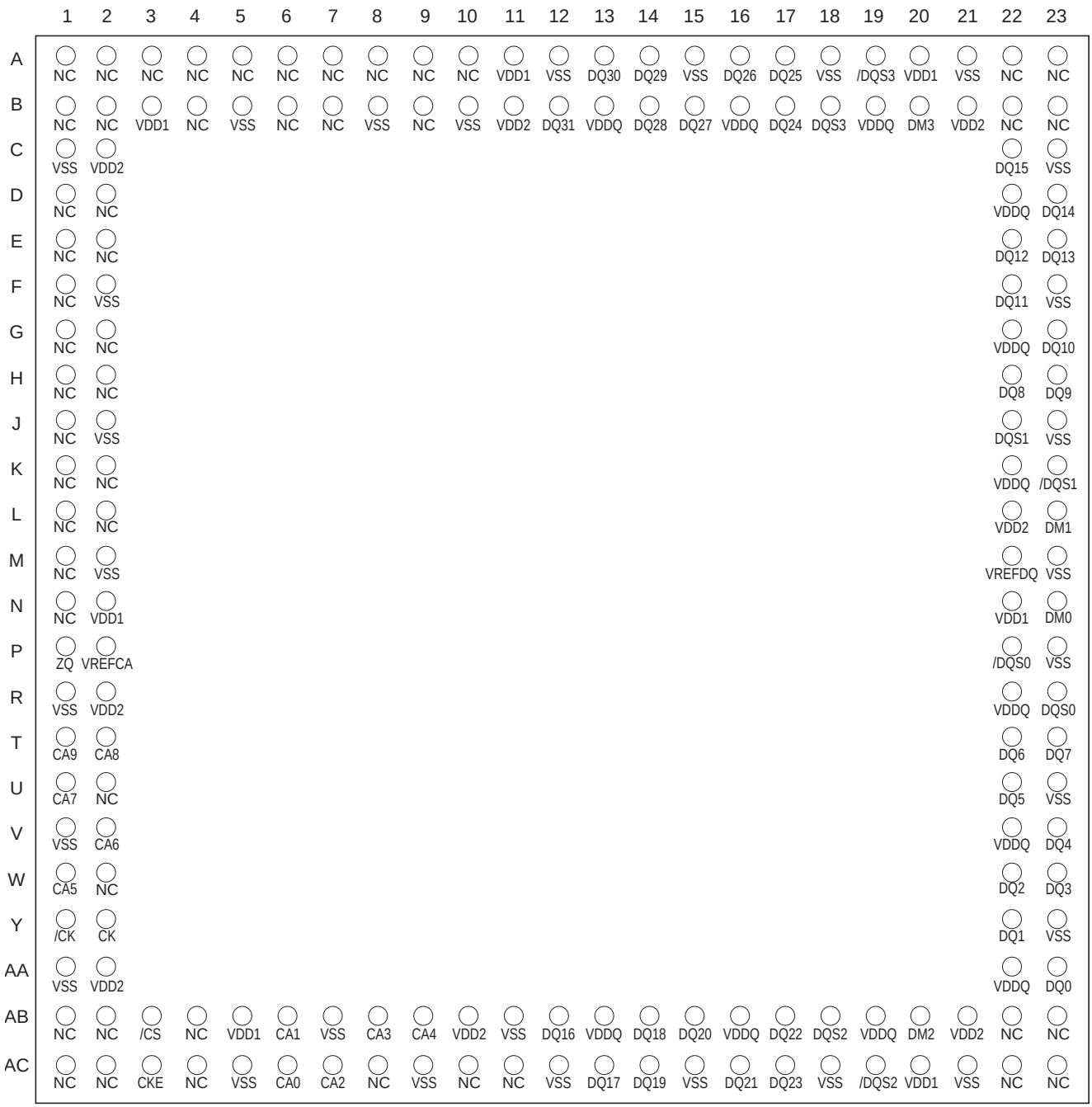
Pin Configurations

/xxx indicate active low signal.

168-ball FBGA



(Top view)

Pin Descriptions

Pin name	Function
CK, /CK	Clock
CKE	Clock enable
/CS	Chip select
CA0 to CA9	DDR command/address inputs (Address configurations: BA0:2, R0:13, C0:9)
DM0 to DM3	Input data mask
DQ0 to DQ31	Data input/output
DQS0 to DQS3, /DQS0 to /DQS3	Data strobe
VDD1	Core power supply 1
VDD2	Core power supply 2 and input receiver power supply
VDDQ	I/O power supply
VREFCA	Reference voltage for CA input receiver
VREFDQ	Reference voltage for DQ input receiver
VSS	Ground
ZQ	Reference pin for output drive strength calibration
NC[*1]	No connection

Note: 1. Not internally connected.

Pin Capacitance

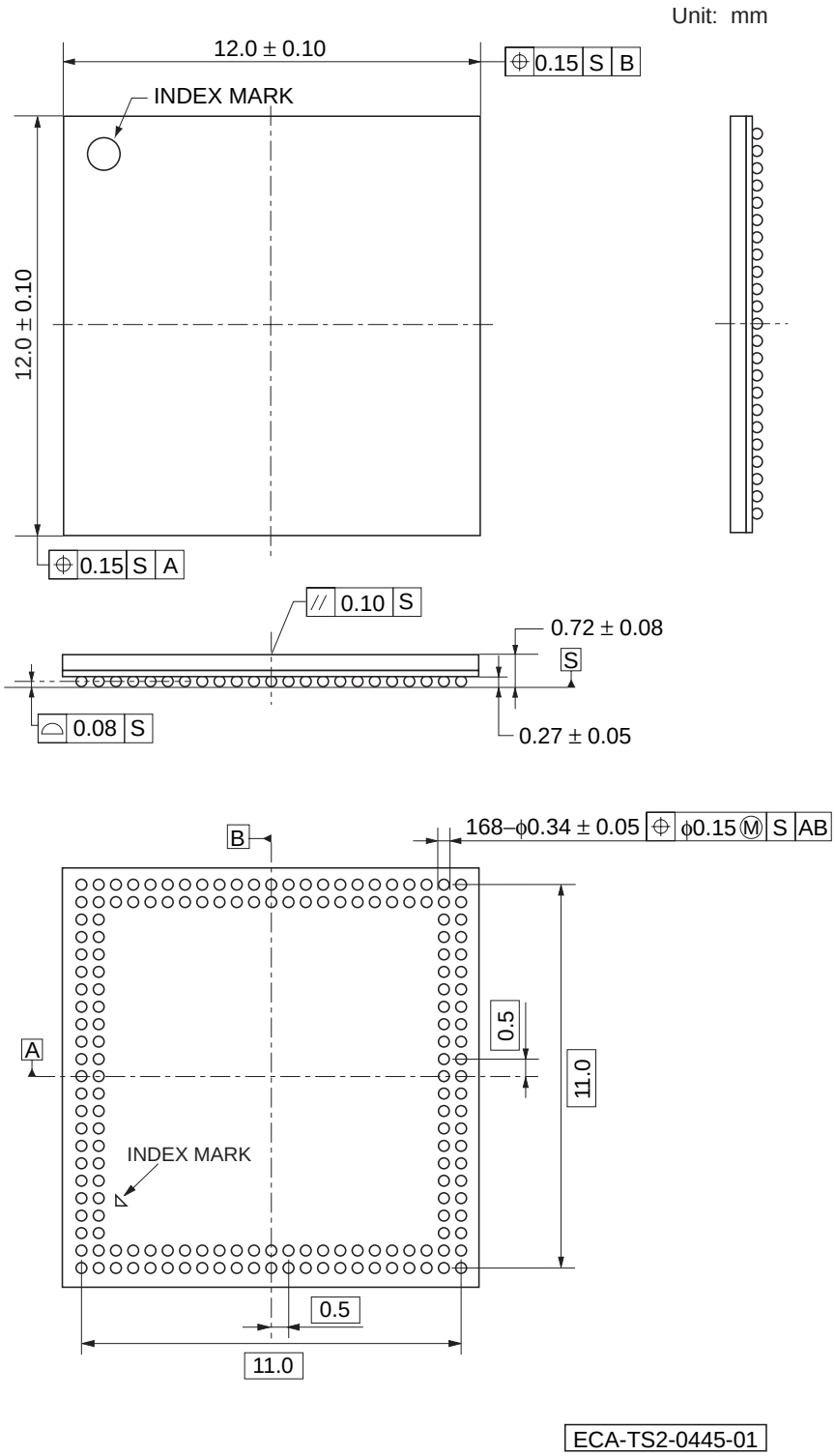
Parameter	Symbol	Pins	min.	max.	Unit	Note
Input capacitance	CI1	CK, /CK	2.0	4.0	pF	1, 2
	CI2	All other DDR2 Mobile RAM input only pins	2.0	4.0	pF	1, 2
Data input/output capacitance	CI/O	DQ, DM, DQS, /DQS	2.0	5.0	pF	1, 2, 3
	CZQ	ZQ	2.0	4.0	pF	1, 2, 3

Notes: 1. This parameter is not subject to production test. It is verified by design and characterization.
2. These parameters are measured on f = 100MHz, VOUT = VDDQ/2, TA = +25°C.
3. DOUT circuits are disabled.

Package Drawing

168-ball FBGA

Solder ball: Lead free



Mode Register Specification

The following table shows the specifications of mode register values (MR5, 6, 7, 8) for the manufacturer ID and the device descriptions such as DRAM type, density, I/O and die revision.

MR#	MA <7:0>	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
5	05h	0	0	0	0	0	0	1	1
		Manufacturer ID : ELPIDA							
6	06h	0	0	0	0	0	0	0	0
		Die Revision : Revision A							
7	07h	0	0	0	0	0	0	0	0
		RFU : Default value							
8	08h	0	0	0	1	1	0	0	0
		I/O : ×32		Density of Die : 4Gbit				Type : S4	

Note: 1. The register values specify monolithic die information in a package.
Therefore, please refer to the block diagram for understanding whole memory configuration of the product containing multiple dice in a package.

1. Electrical Conditions

- All voltages are referenced to VSS (GND)
- Execute power-up and Initialization sequence before proper device operation is achieved.
- Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the DDR2 Mobile RAM Device must be powered down and then restarted through the specialized initialization sequence before normal operation can continue.

1.1 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings

Parameter	Symbol	min.	max.	Unit	Note
VDD1 supply voltage relative to VSS	VDD1	-0.4	2.3	V	2
VDD2 supply voltage relative to VSS	VDD2	-0.4	1.6	V	2
VDDQ supply voltage relative to VSSQ	VDDQ	-0.4	1.6	V	2, 3
Voltage on any ball relative to VSS	VIN, VOUT	-0.4	1.6	V	
Storage Temperature	TSTG	-55	125	°C	

Notes: 1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. See Power-Ramp section “Power-up, initialization and Power-Off” in the individual DDR2 Mobile RAM data sheet for relationship between power supplies.

3. VREF ≤ 0.6 x VDDQ; however, VREF may be ≥ VDDQ provided that VREF ≤ 300mV.

4. Storage Temperature is the case surface temperature on the center/top side of the DDR2 Mobile RAM Device. For the measurement conditions, please refer to JESD51-2 standard.

Caution

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

1.2 Recommended DC Operating Conditions

Table 2 Recommended DC Operating Conditions(TC = -30°C to +85°C)

Parameter	Symbol	min.	typ.	max.	Unit
Core Power1	VDD1	1.70	1.80	1.95	V
Core Power2, Input Buffer Power	VDD2	1.14	1.20	1.30	V
I/O Buffer Power	VDDQ	1.14	1.20	1.30	V

2. Electrical Specifications

2.1 DC Characteristics 1

(TC = -30°C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDQ = 1.14V to 1.30V)

Table 3 IDD Specification Parameters and Operating Conditions

Symbol	Power Supply	1066 max.	800 max.	Unit	Parameter/Condition
IDD0_1	VDD1	11	11	mA	**Operating one bank active-precharge current:** tCK = tCK(avg)min; tRC = tRCmin; CKE is HIGH; /CS is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE
IDD0_2	VDD2	55	52	mA	
IDD0_IN	VDDQ	1.0	1.0	mA	
IDD2P_1	VDD1	0.4	0.4	mA	**Idle power-down standby current:** tCK = tCK(avg)min; CKE is LOW; /CS is HIGH; All banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE
IDD2P_2	VDD2	0.9	0.9	mA	
IDD2P_IN	VDDQ	0.1	0.1	mA	
IDD2PS_1	VDD1	0.4	0.4	mA	**Idle power-down standby current with clock stop:** CK = LOW, /CK = HIGH; CKE is LOW; /CS is HIGH; All banks idle; CA bus inputs are STABLE; Data bus inputs are STABLE
IDD2PS_2	VDD2	0.9	0.9	mA	
IDD2PS_IN	VDDQ	0.1	0.1	mA	
IDD2N_1	VDD1	0.6	0.6	mA	**Idle non power-down standby current:** tCK = tCK(avg)min; CKE is HIGH; /CS is HIGH; All banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE
IDD2N_2	VDD2	15	12	mA	
IDD2N_IN	VDDQ	1.0	1.0	mA	
IDD2NS_1	VDD1	0.6	0.6	mA	**Idle non power-down standby current with clock stop:** CK = LOW, /CK = HIGH; CKE is HIGH; /CS is HIGH; All banks idle; CA bus inputs are STABLE; Data bus inputs are STABLE
IDD2NS_2	VDD2	7.0	7.0	mA	
IDD2NS_IN	VDDQ	1.0	1.0	mA	
IDD3P_1	VDD1	0.7	0.7	mA	**Active power-down standby current:** tCK = tCK(avg)min; CKE is LOW; /CS is HIGH; One bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE
IDD3P_2	VDD2	5.5	5.5	mA	
IDD3P_IN	VDDQ	0.1	0.1	mA	
IDD3PS_1	VDD1	0.7	0.7	mA	**Active power-down standby current with clock stop:** CK = LOW, /CK = HIGH; CKE is LOW; /CS is HIGH; One bank active; CA bus inputs are STABLE; Data bus inputs are STABLE
IDD3PS_2	VDD2	5.5	5.5	mA	
IDD3PS_IN	VDDQ	0.1	0.1	mA	
IDD3N_1	VDD1	1.0	1.0	mA	**Active non power-down standby current:** tCK = tCK(avg)min; CKE is HIGH; /CS is HIGH; One bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE
IDD3N_2	VDD2	22	19	mA	
IDD3N_IN	VDDQ	1.0	1.0	mA	
IDD3NS_1	VDD1	1.0	1.0	mA	**Active non power-down standby current with clock stop:** CK = LOW, /CK = HIGH; CKE is HIGH; /CS is HIGH; One bank active; CA bus inputs are STABLE; Data bus inputs are STABLE
IDD3NS_2	VDD2	15	15	mA	
IDD3NS_IN	VDDQ	1.0	1.0	mA	
IDD4R_1	VDD1	2.0	2.0	mA	**Operating burst read current:** tCK = tCK(avg)min; /CS is HIGH between valid commands; One bank active; BL = 4; RL = RLmin; CA bus inputs are SWITCHING; 50% data change each burst transfer;
IDD4R_2	VDD2	190	150	mA	

Table 3 IDD Specification Parameters and Operating Conditions (cont'd)

Symbol	Power Supply	1066	800	Unit	Parameter/Condition
		max.	max.		
IDD4W_1	VDD1	2.0	2.0	mA	**Operating burst write current:** tCK = tCK(avg)min; /CS is HIGH between valid commands; One bank active; BL = 4; WL = WLmin; CA bus inputs are SWITCHING; 50% data change each burst transfer;
IDD4W_2	VDD2	220	180	mA	
IDD4W_IN	VDDQ	1.0	1.0	mA	

IDD5_1	VDD1	40	40	mA	**All Bank Auto Refresh Burst current:**
					tCK = tCK(avg)min; CKE is HIGH between valid commands;
					tRC = tRFCabmin; Burst refresh;
					CA bus inputs are SWITCHING;
					Data bus inputs are STABLE;

IDD5_2	VDD2	150	150	mA	
IDD5_IN	VDDQ	1.0	1.0	mA	
IDD5AB_1	VDD1	2.0	2.0	mA	**All Bank Auto Refresh Average current:** tCK = tCK(avg)min; CKE is HIGH between valid commands; tRC = tREFI; CA bus inputs are SWITCHING; Data bus inputs are STABLE;
IDD5AB_2	VDD2	16	15	mA	
IDD5AB_IN	VDDQ	1.0	1.0	mA	

IDD5PB_1	VDD1	2.0	2.0	mA	**Per Bank Auto Refresh Average current:**
					tCK = tCK(avg)min; CKE is HIGH between valid commands;
					tRC = tREFI/8;
					CA bus inputs are SWITCHING;
					Data bus inputs are STABLE;

IDD5PB_2	VDD2	16	15	mA	
IDD5PB_IN	VDDQ	1.0	1.0	mA	
IDD8_1	VDD1	16	16	µA	**Deep Power-Down current:** CK = LOW, /CK = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE;
IDD8_2	VDD2	6.0	6.0	µA	
IDD8_IN	VDDQ	12	12	µA	

Notes: 1. IDD values published are the maximum of the distribution of the arithmetic mean.

2. IDD current specifications are tested after the device is properly initialized.

Table 4 IDD6 Full and Partial Array Self-Refresh Current

Parameter		Symbol	Value	Unit	Condition
Self-Refresh Current +45°C	Full Array	IDD6_1	300	µA	CK = LOW, /CK = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE;
		IDD6_2	850	µA	
		IDD6_IN	10	µA	
	1/2 Array	IDD6_1	200	µA	
		IDD6_2	500	µA	
		IDD6_IN	10	µA	
	1/4 Array	IDD6_1	150	µA	
		IDD6_2	300	µA	
		IDD6_IN	10	µA	
	1/8 Array	IDD6_1	120	µA	
		IDD6_2	200	µA	
		IDD6_IN	10	µA	
Self-Refresh Current +85°C	Full Array	IDD6_1	900	µA	
		IDD6_2	3200	µA	
		IDD6_IN	12	µA	
	1/2 Array	IDD6_1	550	µA	
		IDD6_2	2400	µA	
		IDD6_IN	12	µA	
	1/4 Array	IDD6_1	400	µA	
		IDD6_2	2000	µA	
		IDD6_IN	12	µA	
	1/8 Array	IDD6_1	320	µA	
		IDD6_2	1800	µA	
		IDD6_IN	12	µA	

Note: 1. IDD6 85°C is the maximum and IDD6 45°C is typical of the distribution of the arithmetic mean.

2.2 DC Characteristics 2

(TC = -30°C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDQ = 1.14V to 1.30V)

Table 5 Electrical Characteristics and Operating Conditions

Symbol	min.	max.	Unit	Parameter/Condition	Note
IL	-2	+2	µA	**Input leakage current:** For CA, CKE, /CS, CK, /CK Any input 0V ≤ VIN ≤ VDD2 (All other pins not under test = 0V)	2
IVREF	-1	+1	µA	**VREF supply leakage current:** VREFDQ = VDDQ/2 or VREFCA = VDD2/2 (All other pins not under test = 0V)	1

Notes: 1. The minimum limit requirement is for testing purposes. The leakage current on VREFCA and VREFDQ pins should be minimal.

2. Although DM is for input only, the DM leakage shall match the DQ and DQS, /DQS output leakage specification.

2.3 AC Characteristics

(TC = -30°C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDQ = 1.14V to 1.30V)

Table 6 AC Characteristics Table*6

Parameter	Symbol	min. max.	min. tCK*9	1066	800	Unit
Max. Frequency*4			—	533	400	MHz
Clock Timing						
Average Clock Period	tCK(avg)	min.	—	1.875	2.5	ns
		max.	—	100		ns
Average high pulse width	tCH(avg)	min.	—	0.45		tCK(avg)
		max.	—	0.55		
Average low pulse width	tCL(avg)	min.	—	0.45		tCK(avg)
		max.	—	0.55		
Absolute Clock Period	tCK(abs)	min.	—	tCK(avg)(min.) + tJIT(per)(min.)		ps
Absolute clock HIGH pulse width (with allowed jitter)	tCH(abs), allowed	min.	—	0.43		tCK(avg)
		max.	—	0.57		
Absolute clock LOW pulse width (with allowed jitter)	tCL(abs), allowed	min.	—	0.43		tCK(avg)
		max.	—	0.57		
Clock Period Jitter (with allowed jitter)	tJIT(per), allowed	min.	—	-90	-100	ps
		max.	—	90	100	
Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter)	tJIT(cc), allowed	max.	—	180	200	ps
Duty cycle Jitter (with allowed jitter)	tJIT(duty), allowed	min.	—	min((tCH(abs),min - tCH(avg),min), (tCL(abs),min - tCL(avg),min)) × tCK(avg)		ps
		max.	—	max((tCH(abs),max - tCH(avg),max), (tCL(abs),max - tCL(avg),max)) × tCK(avg)		
Cumulative error across 2 cycles	tERR(2per), allowed	min.	—	-132	-147	ps
		max.	—	132	147	
Cumulative error across 3 cycles	tERR(3per), allowed	min.	—	-157	-175	ps
		max.	—	157	175	
Cumulative error across 4 cycles	tERR(4per), allowed	min.	—	-175	-194	ps
		max.	—	175	194	
Cumulative error across 5 cycles	tERR(5per), allowed	min.	—	-188	-209	ps
		max.	—	188	209	
Cumulative error across 6 cycles	tERR(6per), allowed	min.	—	-200	-222	ps
		max.	—	200	222	
Cumulative error across 7 cycles	tERR(7per), allowed	min.	—	-209	-232	ps
		max.	—	209	232	

Table 6 AC Characteristics Table[*6] (cont'd)

Parameter	Symbol	min. max.	min. tCK[*9]	1066	800	Unit
Cumulative error across 8 cycles	tERR(8per), allowed	min.	—	-217	-241	ps
		max.	—	217	241	
Cumulative error across 9 cycles	tERR(9per), allowed	min.	—	-224	-249	ps
		max.	—	224	249	
Cumulative error across 10 cycles	tERR(10per), allowed	min.	—	-231	-257	ps
		max.	—	231	257	
Cumulative error across 11 cycles	tERR(11per), allowed	min.	—	-237	-263	ps
		max.	—	237	263	
Cumulative error across 12 cycles	tERR(12per), allowed	min.	—	-242	-269	ps
		max.	—	242	269	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper), allowed	min.	—	tERR(nper),allowed,min. = (1 + 0.68ln(n)) × tJIT(per),allowed,min.		ps
		max.	—	tERR(nper),allowed,max. = (1 + 0.68ln(n)) × tJIT(per),allowed,max.		
Read Parameters						
DQS output access time from CK, /CK	tDQSCK	min.	—	2500		ps
		max.	—	5500		
DQSCK Delta Short[*15]	tDQSCKDS	max.	—	330	450	ps
DQSCK Delta Medium[*16]	tDQSCKDM	max.	—	680	900	ps
DQSCK Delta Long[*17]	tDQSCKDL	max.	—	920	1200	ps
DQS – DQ skew	tDQSQ	max.	—	200	240	ps
Data hold skew factor	tQHS	max.	—	230	280	ps
DQS Output High Pulse Width	tQSH	min.	—	tCH(abs) - 0.05		tCK(avg)
DQS Output Low Pulse Width	tQSL	min.	—	tCL(abs) - 0.05		tCK(avg)
Data Half Period	tQHP	min.	—	min(tQSH, tQSL)		tCK(avg)
DQ / DQS output hold time from DQS	tQH	min.	—	tQHP - tQHS		ps
Read preamble[*12,*13]	tRPRE	min.	—	0.9		tCK(avg)
Read postamble[*12,*14]	tRPST	min.	—	tCL(abs) - 0.05		tCK(avg)
DQS low-Z from clock[*12]	tLZ(DQS)	min.	—	tDQSCK(min.) - 300		ps
DQ low-Z from clock[*12]	tLZ(DQ)	min.	—	tDQSCK(min.) - (1.4 × tQHS(max.))		ps
DQS high-Z from clock[*12]	tHZ(DQS)	max.	—	tDQSCK(max.) - 100		ps
DQ high-Z from clock[*12]	tHZ(DQ)	max.	—	tDQSCK(max.) + (1.4 × tDQSQ(max.))		ps

Table 6 AC Characteristics Table[*6] (cont'd)

Parameter	Symbol	min. max.	min. tCK[*9]	1066	800	Unit
Write Parameters[*11]						
DQ and DM input hold time (VREF based)	tDH	min.	—	210	270	ps
DQ and DM input setup time (VREF based)	tDS	min.	—	210	270	ps
DQ and DM input pulse width	tDIPW	min.	—	0.35		tCK(avg)
Write command to 1st DQS latching transition	tDQSS	min.	—	0.75		tCK(avg)
		max.	—	1.25		
DQS input high-level width	tDQSH	min.	—	0.4		tCK(avg)
DQS input low-level width	tDQSL	min.	—	0.4		tCK(avg)
DQS falling edge to CK setup time	tDSS	min.	—	0.2		tCK(avg)
DQS falling edge hold time from CK	tDSH	min.	—	0.2		tCK(avg)
Write postamble	tWPST	min.	—	0.4		tCK(avg)
Write preamble	tWPRE	min.	—	0.35		tCK(avg)
CKE Input Parameters						
CKE min. pulse width (high and low pulse width)	tCKE	min.	3	3		tCK(avg)
CKE input setup time	tISCKE[*2]	min.	—	0.25		tCK(avg)
CKE input hold time	tIHCKE[*3]	min.	—	0.25		tCK(avg)
Command Address Input Parameters[*11]						
Address and control input setup time	tIS[*1]	min.	—	220	290	ps
Address and control input hold time	tIH[*1]	min.	—	220	290	ps
Address and control input pulse width	tIPW	min.	—	0.40		tCK(avg)
Boot Parameters (10 MHz – 55 MHz)[*5,*7,*8]						
Clock Cycle Time	tCKb	max.	—	100		ns
		min.	—	18		
CKE Input Setup Time	tISCKEb	min.	—	2.5		ns
CKE Input Hold Time	tIHCKEb	min.	—	2.5		ns
Address & Control Input Setup Time	tISb	min.	—	1150		ps
Address & Control Input Hold Time	tIHb	min.	—	1150		ps
DQS Output Data Access Time from CK, /CK	tDQSCKb	min.	—	2.0		ns
		max.	—	10.0		
Data Strobe Edge to Ouput Data Edge tDQSQb - 1.2	tDQSQb	max.	—	1.2		ns
Data Hold Skew Factor	tQHSb	max.	—	1.2		ns
Mode Register Parameters						
Mode Register Write command period	tMRW	min.	5	5		tCK(avg)
Mode Register Read command period	tMRR	min.	2	2		tCK(avg)

Table 6 AC Characteristics Table[*6] (cont'd)

Parameter	Symbol	min. max.	min. tCK[*9]	1066	800	Unit
DDR2 Mobile RAM Core Parameters[*9]						
Read Latency	RL	min.	3	8	6	tCK(avg)
Write Latency	WL	min.	1	4	3	tCK(avg)
ACTIVE to ACTIVE command period	tRC	min.	—	tRAS + tRPab (with all-bank Precharge) tRAS + tRPpb (with per-bank Precharge)		ns
CKE min. pulse width during Self-Refresh (low pulse width during Self-Refresh)	tCKESR	min.	3	15		ns
Self-refresh exit to next valid command delay	tXSR	min.	2	tRFCab + 10		ns
Exit power down to next valid command delay	tXP	min.	2	7.5		ns
CAS to CAS delay	tCCD	min.	2	2		tCK(avg)
Internal Read to Precharge command delay	tRTP	min.	2	7.5		ns
RAS to CAS Delay	tRCD	min.	3	18		ns
Row Precharge Time (single bank)	tRPpb	min.	3	18		ns
Row Precharge Time (all banks)	tRPab	min.	3	21		ns
Row Active Time	tRAS	min.	3	42		ns
		max.	—	70		µs
Write Recovery Time	tWR	min.	3	15		ns
Internal Write to Read Command Delay	tWTR	min.	2	7.5		ns
Active bank A to Active bank B	tRRD	min.	2	10		ns
Four Bank Activate Window	tFAW	min.	8	50		ns
Minimum Deep Power Down Time	tDPD	min.	—	500		µs
DDR2 Mobile RAM Refresh Requirement Parameters						
Refresh Window	tREFW	max.	—	32		ms
Required number of REFRESH commands	R	min.	—	8192		
Average time between REFRESH commands (for reference only)	tREFI	max.	—	3.9		µs
	tREFIpb	max.	—	0.4875		µs
Refresh Cycle time	tRFCab	min.	—	130		ns
Per Bank Refresh Cycle time	tRFCpb	min.	—	60		ns
Burst Refresh Window = 4 × 8 × tRFCab	tREFBW	min.	—	4.16		µs
ZQ Calibration Parameters[*9]						
Initialization Calibration Time	tZQINIT	min.	—	1		µs
Long Calibration Time	tZQCL	min.	6	360		ns
Short Calibration Time	tZQCS	min.	6	90		ns
Calibration Reset Time	tZQRESET	min.	3	50		ns

Notes: 1. Input set-up/hold time for signal(CA0 – CA9, /CS).

2. CKE input setup time is measured from CKE reaching high/low voltage level to CK, /CK crossing.

3. CKE input hold time is measured from CK, /CK crossing to CKE reaching high/low voltage level.

4. Frequency values are for reference only. Clock cycle time (tCK) shall be used to determine device capabilities.

5. To guarantee device operation before the DDR2 Mobile RAM Device is configured a number of AC boot timing parameters are defined in the Table 6 on page 13. Boot parameter symbols have the letter b appended, e.g. tCK during boot is tCKb.

6. Frequency values are for reference only. Clock cycle time (tCK or tCKb) shall be used to determine device capabilities.

7. The DDR2 Mobile RAM will set some Mode register default values upon receiving a RESET (MRW) command as specified in "Mode Register Definition" in the individual DDR2 Mobile RAM data sheet.

8. The output skew parameters are measured with Ron default settings into the reference load.

9. These parameters should be satisfied with both specification, analog (ns) value and min. tCK.

10. All AC timings assume an input slew rate of 1V/ns.

11. Read, Write, and Input Setup and Hold values are referenced to VREF.

12. For low-to-high and high-to-low transitions the timing reference will be at the point when the signal crosses VTT. tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ)). Figure 1 shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

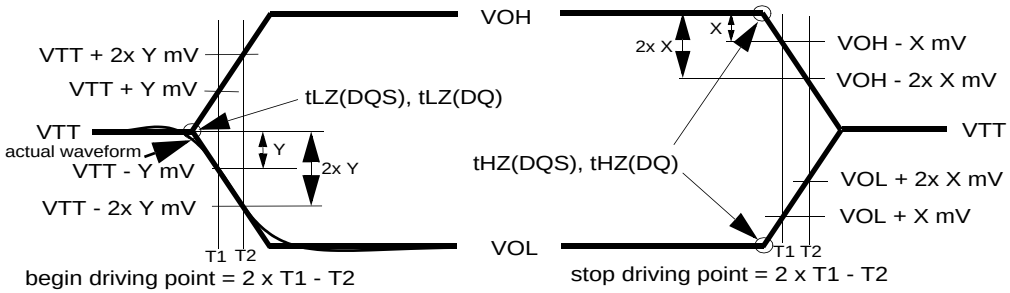


Figure 1 — tLZ and tHZ Method for Calculating Transition and Endpoints

The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS-/DQS.

13. Measured from the start driving of DQS – /DQS to the start driving the first rising strobe edge.

14. Measured from the from start driving the last falling strobe edge to the stop driving DQS – /DQS.

15. tDQSCKDS is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a contiguous sequence of bursts within a 160ns rolling window. tDQSCKDS is not tested and is guaranteed by design. Temperature drift in the system is < 10°C/s. Values do not include clock jitter.

16. tDQSCKDM is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a 1.6μs rolling window. tDQSCKDM is not tested and is guaranteed by design. Temperature drift in the system is < 10°C/s. Values do not include clock jitter.

17. tDQSCKDL is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a 32ms rolling window. tDQSCKDL is not tested and is guaranteed by design. Temperature drift in the system is < 10°C/s. Values do not include clock jitter.

2.3.1 HSUL_12 Driver Output Timing Reference Load

These 'Timing Reference Loads' are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

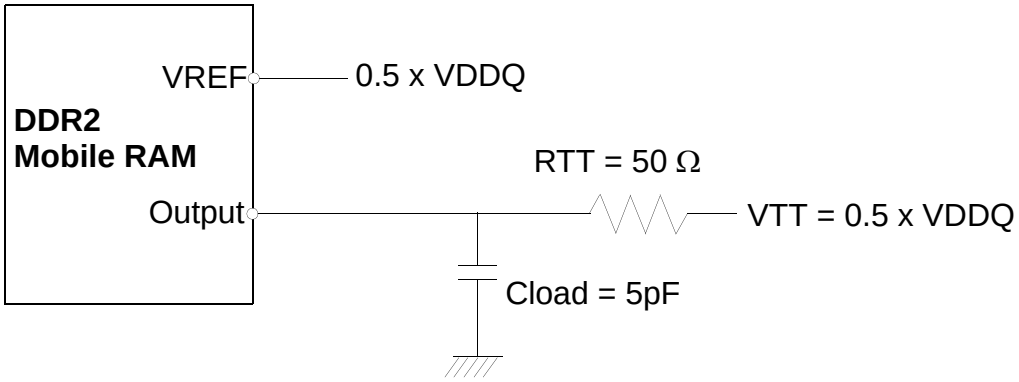


Figure 2 — HSUL_12 Driver Output Reference Load for Timing and Slew Rate

Note: 1. All output timing parameter values (like tDQSCK, tDQSQ, tQHS, tHZ, tRPRE etc) are reported with respect to this reference load. This reference load is also used to report slew rate.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

CME0107

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