5V ECL Coaxial Cable Driver

The MC10EL89 is a differential fanout gate specifically designed to drive coaxial cables. The device is especially useful in Digital Video Broadcasting applications; for this application, since the system is polarity free, each output can be used as an independent driver. The driver boasts a gain of approximately 40 and produces output swings twice as large as a standard ECL output. When driving a coaxial cable, proper termination is required at both ends of the line to minimize signal loss. The 1.6 V output swings allow for termination at both ends of the cable, while maintaining the required 800 mV swing at the receiving end of the cable. Because of the larger output swings, the device cannot be terminated into the standard -2.0 V. All of the DC parameters are tested with a 50 Ω to -3.0 V load. The driver accepts a standard differential ECL input and can run off of the Digital Video Broadcast standard -5.0 V supply.

Features

- 375 ps Propagation Delay
- 1.6 V Output Swings
- PECL Mode Operating Range: $V_{CC} = 4.2 \text{ V}$ to 5.7 V with $V_{EE} = 0 \text{ V}$
- NECL Mode Operating Range: $V_{CC} = 0 V$ with V_{EE} = -4.2 V to -5.7 V
- Internal Input Pulldown Resistors
- Pb-Free Packages are Available

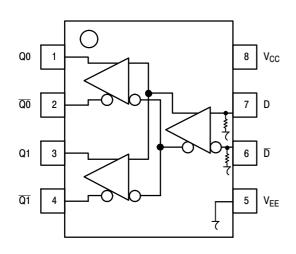


Figure 1. Logic Diagram and Pinout Assignment

ON Semiconductor®										
h	ttp://onsemi.co	m								
		MARKING DIAGRAMS*								
8 (1)	SOIC-8 D SUFFIX CASE 751	8 <u>H H H H</u> HEL89 ALYW 1 U U U U								
8 आ	TSSOP-8 DT SUFFIX CASE 948R	8 <u>A A A A</u> HL89 ALYW- o - 1 <u>H H H H</u>								
	DFN8 MN SUFFIX CASE 506AA									
A L W M	= Assembly Lo = Wafer Lot = Year = Work Week = Date Code = Pb-Free Pao									
*For addition	odot may be in eith al marking informa Note AND8002/D.	ation, refer to								
0000										

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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Table 1. PIN DESCRIPTION

PIN	Function
D, D	ECL Data Inputs
Q0, <u>Q0;</u> Q1, <u>Q1</u>	ECL Data Outputs (1.6 V _{pp})
V _{CC}	Positive Supply
V _{EE}	Negative Supply
EP	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

Table 2. ATTRIBUTES

Characterist	Value				
Internal Input Pulldown Resistor	50 KΩ				
Internal Input Pullup Resistor		N/A			
ESD Protection	Human Body Model Machine Model	> 2 kV > 100 V			
Moisture Sensitivity, Indefinite Time	Out of Drypack (Note 1)	Level 1			
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in			
Transistor Count		31			
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test					

1. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	$V_{CC} = 0 V$		-8	V
VI	PECL Mode Input Voltage NECL Mode Input Voltage	V _{EE} = 0 V V _{CC} = 0 V	$\substack{V_{I} \leq V_{CC} \\ V_{I} \geq V_{EE}}$	6 -6	V V
l _{out}	Output Current	Continuous Surge		50 100	mA mA
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SO-8 SO-8	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board SO-8		41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP-8 TSSOP-8	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44 \pm 5%	°C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	DFN8 DFN8	129 84	°C/W °C/W
T _{sol}	Wave Solder Pb Pb-Free	<2 to 3 sec @ 248°C <2 to 3 sec @ 260°C		265 265	°C
θJC	Thermal Resistance (Junction-to-Case)	(Note 2)	DFN8	35 to 40	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. JEDEC standard multilayer board - 2S2P (2 signal, 2 power)

		-40°C 25°C			85°C						
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
I _{EE}	Power Supply Current		23	28		23	28		23	28	mA
V _{OH}	Output HIGH Voltage (Note 4)	3.77	3.90	4.02	3.87	3.98	4.10	3.94	4.04	4.19	V
V _{OL}	Output LOW Voltage (Note 4)	2.10	2.28	2.42	2.00	2.30	2.44	1.95	2.33	2.49	V
V _{IH}	Input HIGH Voltage (Single-Ended)	3770		4110	3870		4190	3940		4280	mV
V _{IL}	Input LOW Voltage (Single-Ended)	3050		3500	3050		3520	3050		3555	mV
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 5)	2.5		4.6	2.5		4.6	2.5		4.6	V
I _{IH}	Input HIGH Current		70	150		50	150		40	150	μA
IIL	Input LOW Current	0.5	50		0.5	30		0.3	25		μA

Table 4. 10EL SERIES PECL DC CHARACTERISTICS V_{CC} = 5.0 V; V_{EE} = 0.0 V (Note 3)

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.25 V / -0.5 V.

4. Outputs are terminated through a 50 Ω resistor to V_{CC} – 3.0 V.

V_{IHCMR} min varies 1:1 with V_{EE}. V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

			-40°C		25°C			85°C			
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
I _{EE}	Power Supply Current		23	28		23	28		23	28	mA
V _{OH}	Output HIGH Voltage (Note 7)	-1.23	-1.10	-0.98	-1.13	-1.02	-0.90	-1.06	-0.96	-0.81	V
V _{OL}	Output LOW Voltage (Note 7)	-2.90	-2.72	-2.58	-3.00	-2.70	-2.56	-3.05	-2.67	-2.51	V
V _{IH}	Input HIGH Voltage (Single-Ended)	-123 0		-890	-1130		-810	-106 0		-720	mV
V _{IL}	Input LOW Voltage (Single-Ended)	-195 0		-150 0	-195 0		-148 0	-195 0		-144 5	mV
VIHCMR	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 8)	-2.5		-0.4	-2.5		-0.4	-2.5		-0.4	V
I _{IH}	Input HIGH Current		70	150		50	150		20	150	μA
IIL	Input LOW Current	0.5	50		0.5	30		0.3	25		μA

Table 5. 10EL SERIES NECL DC CHARACTERISTICS $V_{CC} = 0.0 V$; $V_{EE} = -5.0 V$ (Note 6)

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.25 V / –0.5 V.

7. Outputs are terminated through a 50 Ω resistor to V_{CC} – 3.0 V.

V_{IHCMR} min varies 1:1 with V_{EE}. V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

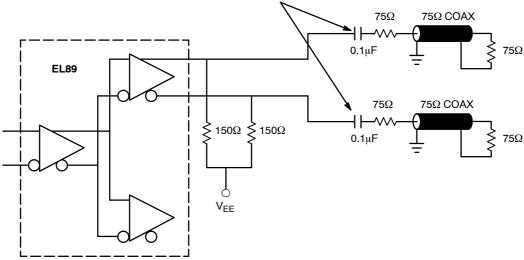
Table 6. AC CHARACTERISTICS V _C	$_{c}$ = 5.0 V; V _{EE} = 0.0 V or V _{CC} = 0.0 V; V _{EE} = -5.0 V	√ (Note 9)
--------------------------------------------	----------------------------------------------------------------------------------------------	------------

		−40°C		25°C		85°C					
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
f _{max}	Maximum Toggle Frequency					1.5					Gb/s
t _{PLH} t _{PHL}	Propagation Delay to Output	200	340	480	260	350	440	310	400	490	ps
t _{SKEW}	Within-Device Skew		5	20		5	20		5	20	ps
t _{JITTER}	Random Clock Jitter (RMS)		5			5			5		ps
V _{PP}	Input Swing (Note 10)	150			150	400		150			mV
t _r t _f	Output Rise/Fall Times Q (20% – 80%)	205	330	455	205	330	455	205	330	455	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

9. V_{EE} can vary +0.25 V / -0.5 V.

 $10.V_{PP(min)}^{-}$ is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈ 40 .



DC BLOCKING CAPACITORS

Figure 2. EL89 CATV Termination Configuration

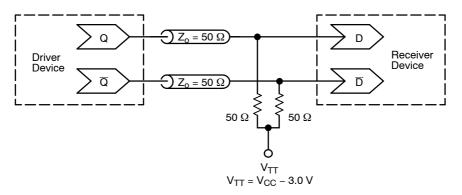


Figure 3. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

ORDERING INFORMATION

Device	Package	Shipping [†]
MC10EL89D	SOIC-8	98 Units / Rail
MC10EL89DG	SOIC-8 (Pb-Free)	98 Units / Rail
MC10EL89DR2	SOIC-8	2500 / Tape & Reel
MC10EL89DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC10EL89DT	TSSOP-8	100 Units / Rail
MC10EL89DTG	TSSOP-8 (Pb-Free)	100 Units / Rail
MC10EL89DTR2	TSSOP-8	2500 / Tape & Reel
MC10EL89DTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel
MC10EL89MNR4	DFN8	1000 / Tape & Reel
MC10EL89MNR4G	DFN8 (Pb-Free)	1000 / Tape & Reel

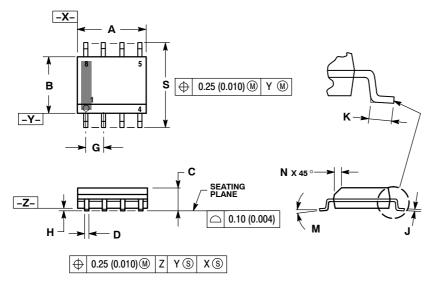
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D	-	ECL Clock Distribution Techniques
AN1406/D	-	Designing with PECL (ECL at +5.0 V)
AN1503/D	_	ECLinPS [™] I/O SPiCE Modeling Kit
AN1504/D	-	Metastability and the ECLinPS Family
AN1568/D	-	Interfacing Between LVDS and ECL
AN1672/D	-	The ECL Translator Guide
AND8001/D	-	Odd Number Counters Design
AND8002/D	-	Marking and Date Codes
AND8020/D	-	Termination of ECL Logic Devices
AND8066/D	-	Interfacing with ECLinPS
AND8090/D	-	AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

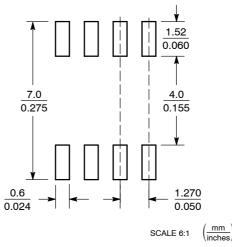
SOIC-8 NB CASE 751-07 **ISSUE AH**

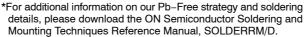


- NOTES:
 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: MILLIMETER.
 DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

	MILLIN	IETERS	INCHES			
DIM	MIN	MAX	MIN	MAX		
Α	4.80	5.00	0.189	0.197		
В	3.80	4.00	0.150	0.157		
С	1.35	1.75	0.053	0.069		
D	0.33	0.51	0.013	0.020		
G	1.27	7 BSC	0.050 BSC			
н	0.10	0.25	0.004	0.010		
J	0.19	0.25	0.007	0.010		
к	0.40	1.27	0.016	0.050		
м	0 °	8 °	0 °	8 °		
Ν	0.25	0.50	0.010	0.020		
S	5.80	6.20	0.228	0.244		

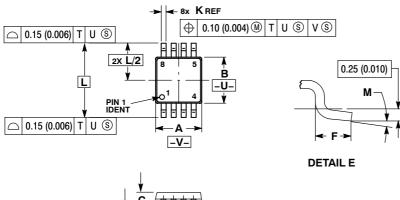
SOLDERING FOOTPRINT*

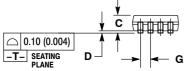


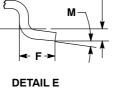


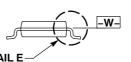
PACKAGE DIMENSIONS

TSSOP-8 DT SUFFIX PLASTIC TSSOP PACKAGE CASE 948R-02 **ISSUE A**





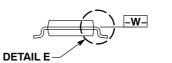




	(0.006) PER SID	DE.								
4.	DIME	SION B	DOES NO	T INCLUE	DE INTERI	EAD					
	FLASH	SH OR PROTRUSION. INTERLEAD FLASH OR									
	PROT	RUSION S	SHALL NO	DT EXCEE	ED 0.25 (0	.010)					
	PER S					,					
5.	TERM	INAL NUM	IBERS AI	RE SHOW	/N FOR						
	REFE	RENCE O	NLY.								
6.	DIME	VSION A	AND B AR	E TO BE	DETERMI	NED					
	AT DA	TUM PLA	NE -W								
						1					
		MILLIMETERS		INC	HES						
	DIM	MIN	MAX	MIN	MAX						
	Α	2.90	3.10	0.114	0.122						
	В	2.90	3.10	0.114	0.122						
	<u>ر</u>	0.80	1 10	0.031	0.043						

NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: MILLIMETER. 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE. 4. DIMENSION R DOES NOT INCLUDE INTERLEAD.

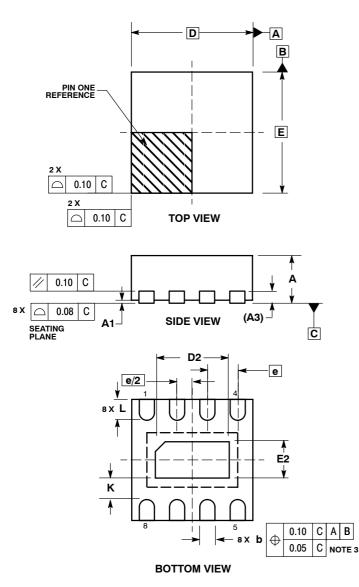
NOTES:



DIM	MIN	MAX	MIN	MAX
Α	2.90	3.10	0.114	0.122
В	2.90	3.10	0.114	0.122
С	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
М	0°	6 °	0°	6 °

PACKAGE DIMENSIONS

DFN8 CASE 506AA-01 ISSUE D



NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLING DIMENSION: MILLIMETERS.
 DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN
- 0.25 AND 0.30 MM FROM TERMINAL.4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	MAX	
Α	0.80	1.00	
A1	0.00	0.05	
A3	0.20 REF		
b	0.20	0.30	
D	2.00 BSC		
D2	1.10	1.30	
E	2.00 BSC		
E2	0.70	0.90	
е	0.50 BSC		
к	0.20		
L	0.25	0.35	

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