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DATA SHEET
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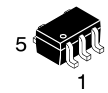
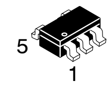
Precision Operational Amplifier, 10 μV, Zero-Drift, 1.6 V to 5.5 V Supply, 1.5 MHz

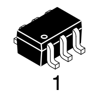
NCS21801, NCS21802, NCS21803, NCS21804



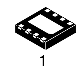
SC−88A / SC70−5
CASE 419A−02



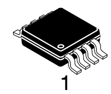
TSOP−5 / SOT23−5
CASE 483



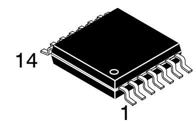
SC−88 / SC70−6
CASE 419B−02



UDFN8
CASE 517AW



Micro8
CASE 846A−02



TSSOP−14 WB
CASE 948G

The NCS21801, NCS21802, NCS21803, and NCS21804 are precision op amps featuring low input offset voltage and low offset drift over time and temperature. The common mode voltage range extends 100 mV beyond the supply rails, which makes it suitable for both high−side and low−side current sensing applications.

The NCS2180x is available in single, dual, and quad channel configurations. All versions are specified for operation from −40°C to +125°C. NCV prefix parts are automotive grade 1 qualified and offer performance over the extended temperature range from −40°C to +150°C.

Features

- Input Offset Voltage: ±10 μV max
- Offset Voltage Drift Over Temperature: ±5 nV/°C Typical
- Common Mode Input Voltage Range: V_{SS} – 0.1 V to V_{DD} + 0.1 V
- Supply Voltage Range: 1.8 V to 5.5 V
- Extended Supply Voltage Range: 1.6 V to 5.5 V for T_A = 0°C to 85°C
- Unity Gain Bandwidth: 1.5 MHz
- Quiescent Consumption: 100 μA Max per Channel
- Enable Function Available on NCS21803
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- High−Side Current Sensing
- Low−Side Current Sensing
- Difference Amplifier
- Instrumentation Amplifier
- Power Management
- Automotive

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 2 of this data sheet.

PIN CONNECTIONS

See pin connections on page 3 of this data sheet.

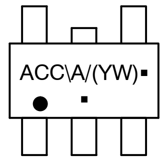
ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

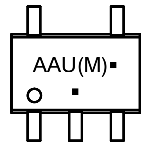
March, 2022 − Rev. 7

Publication Order Number:
NCS21801/D

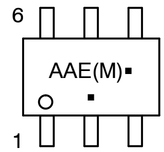
DEVICE MARKING INFORMATION



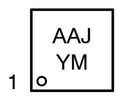
TSOP−5 / SOT23−5
CASE 483



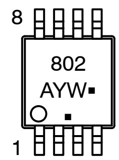
SC−88A / SC70−5
CASE 419A−02



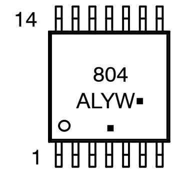
SC−88 / SC70−6 / SOT−363
CASE 419B−02



UDFN8, 2x2, 0.5P
CASE 517AW



Micro8
CASE 846A−02



TSSOP−14 WB
CASE 948G

XX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
M = Date Code
G or ▪ = Pb−Free Package
(Note: Microdot may be in either location)

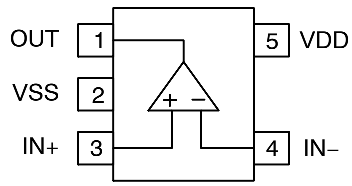
ORDERING INFORMATION

Channels	Enable	Package	Part Number	Marking	Shipping
INDUSTRIAL AND CONSUMER					
Single	No	SOT23−5 / TSOP−5	NCS21801SN2T1G	ACC	3000 / Tape & Reel
		SC70−5 / SC−88−5 / SOT−353−5	NCS21801SQ3T2G	AAU	
	Yes	SC−88 / SC70−6 / SOT−363	NCS21803SQT2G	AAE	
Dual	No	UDFN−8	NCS21802MUTBG	AAJ	3000 / Tape & Reel
		Micro8	NCS21802DMR2G	802	4000 / Tape & Reel
Quad	No	TSSOP−14	NCS21804DTBR2G	804	2500 / Tape & Reel
AUTOMOTIVE QUALIFIED					
Single	No	SOT23−5 / TSOP−5	NCV21801SN2T1G	ACC	3000 / Tape & Reel
		SC70−5 / SC−88−5 / SOT−353−5	NCV21801SQ3T2G	AAU	
Dual	No	Micro8	NCV21802DMR2G	802	4000 / Tape & Reel
Quad	No	TSSOP−14	NCV21804DTBR2G	804	2500 / Tape & Reel

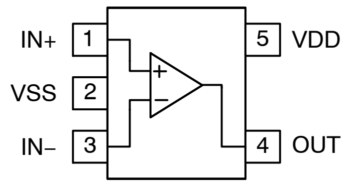
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PIN CONNECTIONS

Single Channel Configuration
NCS21801

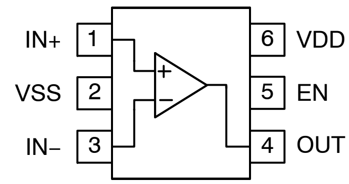


SOT23−5 / TSOP−5



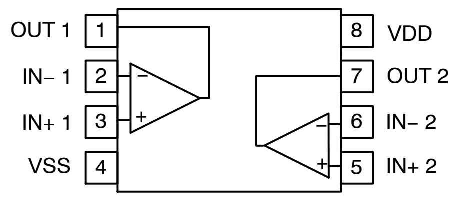
SC70−5 / SC−88−5 / SOT−353−5

Single Channel with Enable Configuration
NCS21803



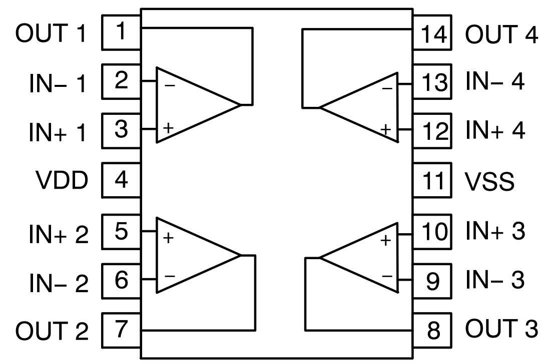
SC88 / SC70−6 / SOT−363

Dual Channel Configuration
NCS21802



UDFN8 / Micro8

Quad Channel Configuration
NCS21804



TSSOP−14

MAXIMUM RATINGS (Note 1)

Parameter		Symbol	Rating	Unit
Supply Voltage (V_{DD} – V_{SS}) (Note 1)		V_S	−0.3 to 6	V
Input Voltage (Note 2)		V_{IN+}, V_{IN-}, V_{EN}	(V_{SS} – 0.3) to (V_{DD} + 0.3)	V
Differential Input Voltage		V_{IN+}, V_{IN-}	± (V_{DD} – V_{SS} + 0.3)	V
Output Voltage (Note 2)		V_{OUT}	(V_{SS} – 0.3) to (V_{DD} + 0.3)	V
Output Short Circuit Current (Note 3)		I_{OUT}	Continuous	
Input Current into Any Pin (Note 2)		I_{IN}	±10	mA
Maximum Junction Temperature		$T_{J(max)}$	+150	°C
Storage Temperature Range		T_{STG}	−65 to +150	°C
ESD	Human Body Model (Note 4)	HBM	±2000	V
	Charged Device Model (Note 4)	CDM	±1000	V
Latch−up Current (Note 5)			100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for safe operating parameters
2. Terminals are diode−clamped to the power−supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to ±10 mA or less. Output terminals should not be driven by external sources.
3. Short circuits to either rail can cause an increase in the junction temperature. The total power dissipation must be limited to prevent the junction temperature from exceeding the 150°C limit.
4. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per JEDEC standard JS−001−2017 (AEC−Q100−002)
   ESD Charged Device Model tested per JEDEC standard JS−002−2014 (AEC−Q100−011)
5. Latch−up Current tested per JEDEC standard: JESD78E.

THERMAL CHARACTERISTICS (Notes 6, 7)

Package	θ_{JA} Junction−to−Ambient Thermal Resistance	Ψ_{JT} Junction−to−Case Top Thermal Characteristic	Ψ_{JB} Junction−to−Board Thermal Characteristic	Unit
TSOP−5 / SOT23−5	188	26	38	°C/W
SC70−5 / SC−88−5 / SOT−353−5	241	46	64	
SC−88 / SC70−6 / SOT−363	230	45	60	
UDFN8	105	10	51	
Micro8 / MSOP−8	105	24	96	
TSSOP−14	86	9	53	

6. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for safe operating parameters
7. Mounted on a JESD51−7 thermal board, 2S2P, 1 in^2 copper spreader area, 1 oz signal plane thickness

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Conditions	Min	Max	Unit
Ambient Temperature	T_A	NCS prefix	−40	125	°C
		NCV prefix	−40	150 (Note 8)	
Common Mode Input Voltage	V_{CM}	Full temperature range	V_{SS} – 0.1	V_{DD} + 0.1	V
Supply Voltage (V_{DD} – V_{SS})	V_S	T_A = 0 to 85°C	1.6	5.5	V
		Full temperature range	1.8	5.5	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

8. Operation up to T_A = 150°C is permitted, provided the total power dissipation is limited to prevent the junction temperature from exceeding the 150°C absolute maximum limit.

ELECTRICAL CHARACTERISTICS At T_A = +25°C, Vs = 1.8 V to 5.5 V, and V_{CM} = V_{OUT} = mid−supply, unless otherwise noted.
Boldface limits apply over the specified temperature range, unless otherwise noted, guaranteed by characterization and/or design.

Parameter	Symbol	Conditions	Temp (°C)	Min	Typ	Max	Unit
INPUT							
Input Offset Voltage	V_{OS}	V_S = 3.3 V	25		±2	±10	μV
Input Offset Voltage Drift vs. Temperature	dV_{OS}/dT	V_S = 1.8 V to 5.5 V	–40 to 125		±5	**±75**	nV/°C
			–40 to 150		±5	**±75**	
Common Mode Rejection Ratio	CMRR	V_S = 1.8 V, V_{CM} = V_{SS} − 0.1 V to V_{DD} + 0.1 V	25	106	131		dB
			–40 to 125	**100**			
			–40 to 150	**100**			
		V_S = 3.3 V, V_{CM} = V_{SS} − 0.1 V to V_{DD} + 0.1 V	25	113	134		
			–40 to 125	**110**			
			–40 to 150	**110**			
		V_S = 5.5 V, V_{CM} = V_{SS} − 0.1 V to V_{DD} + 0.1 V	25	111	137		
			–40 to 125	**108**			
			–40 to 150	**108**			
Input Bias Current (Note 9)	I_{IB}		25		±60	±200	pA
			–40 to 125			**±600**	
			–40 to 150			**±5000**	
Input Offset Current (Note 9)	I_{OS}		25		±60	±300	pA
			–40 to 125			**±400**	
			–40 to 150			**±2500**	
Input Capacitance	C_{IN}	Differential	25		5		pF
		Common mode	25		5		
ENABLE (Note 10)							
Input Voltage Low Threshold	V_{EN-L}	Shutdown	–40 to 125			**V_{SS} + 0.5**	V
Input Voltage High Threshold	V_{EN-H}	Enabled	–40 to 125	**V_{SS} + 1.3**			V
Input Leakage Current	I_{EN}		25		1	100	nA
OUTPUT CHARACTERISTICS							
Open Loop Voltage Gain	A_{VOL}	V_S = 1.8 V	25	108	133		dB
			–40 to 125	**106**			
			–40 to 150	**106**			
		V_S = 3.3 V, 5.5 V	25	120	143		
			–40 to 125	**110**			
			–40 to 150	**110**			

9. Guaranteed by characterization and/or design.
10. The enable function is available on NCS21803 only. The EN pin must be connected to a logic low or logic high voltage.
11. Shutdown Time (t_{OFF}) and Enable Time (t_{ON}) are defined as the time between the 50% point of the signal applied to the EN pin and the point at which the output voltage reaches within 10% of its final value.

ELECTRICAL CHARACTERISTICS At T_A = +25°C, Vs = 1.8 V to 5.5 V, and V_{CM} = V_{OUT} = mid−supply, unless otherwise noted. **Boldface** limits apply over the specified temperature range, unless otherwise noted, guaranteed by characterization and/or design.

Parameter	Symbol	Conditions	Temp (°C)	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS							
Output Voltage High, Referenced from VDD Supply Rail	V_{DD} − V_{OH}	I_{OUT} = 30 μA	25		1	5	mV
			−40 to 125			**10**	
			−40 to 150			**10**	
		V_S = 3.3 V, I_{OUT} = 3 mA	25		55	100	
			−40 to 125			**125**	
			−40 to 150			**125**	
Output Voltage Low, Referenced to VSS Supply Rail	V_{OL} − V_{SS}	I_{OUT} = 30 μA	25		1	5	mV
			−40 to 125			**10**	
			−40 to 150			**10**	
		V_S = 3.3 V, I_{OUT} = 3 mA	25		55	100	
			−40 to 125			**125**	
			−40 to 150			**125**	
Output Current Sourcing Capability	I_O	V_S = 1.8 V	25		24		mA
		V_S = 3.3 V	25		29		
		V_S = 5.5 V	25		32		
Output Current Sinking Capability	I_O	V_S = 1.8 V	25		28		
		V_S = 3.3 V	25		32		
		V_S = 5.5 V	25		38		
Capacitive Load Capability	C_L	A_V = −1, V_{IN} = 100 mVpp step A_V = 1, V_{IN} = 100 mVpp step	25		400 125		pF
DYNAMIC RESPONSE							
Unity Gain Bandwidth	BW	C_L = 20 pF	25		1.5		MHz
Gain Margin	A_M	C_L = 20 pF	25		6		dB
Phase Margin	Φ_M	C_L = 20 pF	25		50		°
Slew Rate	SR		25		0.7		V/μs
Settling Time	t_s	0.1%, A_V = 1	25		20		μs
Overload Recovery Time	t_{OR}	V_{IN} * GAIN > V_S	25		200		μs
Channel Separation		NCS21802, NCS21804, f = 10 kHz	25		90		dB
EMI Rejection Ratio	EMIRR		25		See Fig. 26		dB
NOISE							
Voltage Noise Density	e_N	V_S = 3.3, f_{in} = 1 kHz	25		42		nV/√Hz
Voltage Noise, Peak−to−Peak	e_{P-P}	f_{in} = 0.1 Hz to 10 Hz	25		400		nV_{PP}
Current Noise Density	i_N	f_{in} = 1 kHZ	25		445		fA/√Hz

9. Guaranteed by characterization and/or design.
10. The enable function is available on NCS21803 only. The EN pin must be connected to a logic low or logic high voltage.
11. Shutdown Time (t_{OFF}) and Enable Time (t_{ON}) are defined as the time between the 50% point of the signal applied to the EN pin and the point at which the output voltage reaches within 10% of its final value.

ELECTRICAL CHARACTERISTICS At T_A = +25°C, Vs = 1.8 V to 5.5 V, and V_{CM} = V_{OUT} = mid−supply, unless otherwise noted. **Boldface** limits apply over the specified temperature range, unless otherwise noted, guaranteed by characterization and/or design.

Parameter	Symbol	Conditions	Temp (°C)	Min	Typ	Max	Unit
POWER SUPPLY							
Quiescent Current	I_Q	NCS21801, NCS2803, no load	25		75	105	μA
			–40 to 125			**130**	
			–40 to 150			**200**	
		NCS21802, NCS21804, per channel, no load	25		75	100	μA
			–40 to 125			**125**	
			–40 to 150			**150**	
Quiescent Current in Shutdown (Notes 9, 10)	I_{QSD}	Per channel	25		5	50	nA
			–40 to 85			**75**	
			–40 to 125			**200**	
Power Supply Rejection Ratio	PSRR	V_S = 1.8 V to 5.5 V	25	115	140		dB
			–40 to 125	**110**			
			–40 to 150	**110**			
Power Up Time		NCS21801, NCS21803	25		50		μs
		NCS21802, NCS21804	25		40		
Enable Time (Note 10, 11)	t_{ON}		25		50		μs
Shutdown Time (Note 10, 11)	t_{OFF}		25		3		μs

9. Guaranteed by characterization and/or design.
10. The enable function is available on NCS21803 only. The EN pin must be connected to a logic low or logic high voltage.
11. Shutdown Time (t_{OFF}) and Enable Time (t_{ON}) are defined as the time between the 50% point of the signal applied to the EN pin and the point at which the output voltage reaches within 10% of its final value.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ELECTRICAL CHARACTERISTICS At T_A = +25°C, V_S = 1.6 V, and V_{CM} = V_{OUT} = mid−supply, unless otherwise noted. **Boldface** limits apply over the specified temperature range, T_A = 0°C to 85°C, guaranteed by characterization and/or design.

Parameter	Symbol	Conditions	Temp (°C)	Min	Typ	Max	Unit
INPUT							
Input Offset Voltage	V_{OS}		25		±3	±13	μV
Input Offset Voltage Drift vs. Temperature	dV_{OS}/dT		0 to 85		±5	**±75**	nV/°C
Common Mode Rejection Ratio	CMRR	V_{CM} = V_{SS} − 0.1 V to V_{DD} + 0.1 V	25	96	123		dB
			0 to 85	**94**			
Input Bias Current (Note 12)	I_{IB}		25		±30	±160	pA
			0 to 85			**±250**	
Input Offset Current (Note 12)	I_{OS}		25		±36	±200	pA
			0 to 85			**±250**	
Input Capacitance	C_{IN}	Differential	25		5		pF
		Common mode	25		5		
ENABLE (Note 14)							
Input Voltage Low Threshold	V_{EN-L}	Shutdown	0 to 85			**V_{SS} + 0.5**	V
Input Voltage High Threshold	V_{EN-H}	Enabled	0 to 85	**V_{SS} + 1.3**			V
Input Leakage Current	I_{EN}		25		1	100	nA
OUTPUT CHARACTERISTICS							
Open Loop Voltage Gain	A_{VOL}		25	106	128		dB
			0 to 85	**104**			
Output Voltage High, Referenced from V_{DD} Supply Rail	V_{DD} − V_{OH}	I_{OUT} = 30 μA	25		1	5	mV
			0 to 85			**10**	
		I_{OUT} = 3 mA	25		85	130	
			0 to 85			**150**	
Output Voltage Low, Referenced to V_{SS} Supply Rail	V_{OL} − V_{SS}	I_{OUT} = 30 μA	25		1	5	mV
			0 to 85			**10**	
		I_{OUT} = 3 mA	25		75	130	
			0 to 85			**150**	
Output Current Sourcing Capability	I_o		25		15		mA
Output Current Sinking Capability	I_o		25		21		
Capacitive Load Capability	C_L	A_V = −1, V_{IN} = 100 mVpp step A_V = 1, V_{IN} = 100 mVpp step	25		400 125		pF
DYNAMIC RESPONSE							
Unity Gain Bandwidth	BW	C_L = 20 pF	25		1.4		MHz
Gain Margin	A_M	C_L = 20 pF	25		6		dB
Phase Margin	Φ_M	C_L = 20 pF	25		50		°
Slew Rate	SR		25		0.7		V/μs

12. Guaranteed by design and/or characterization.
13. The enable function is available on NCS21803 only. The EN pin must be connected to a logic low or logic high voltage.
14. Shutdown Time (t_{OFF}) and Enable Time (t_{ON}) are defined as the time between the 50% point of the signal applied to the EN pin and the point at which the output voltage reaches within 10% of its final value.

ELECTRICAL CHARACTERISTICS At T_A = +25°C, V_S = 1.6 V, and V_{CM} = V_{OUT} = mid−supply, unless otherwise noted. **Boldface** limits apply over the specified temperature range, T_A = 0°C to 85°C, guaranteed by characterization and/or design.

Parameter	Symbol	Conditions	Temp (°C)	Min	Typ	Max	Unit
DYNAMIC RESPONSE							
Settling Time	t_S	0.1%, A_V = 1	25		20		µs
Overload Recovery Time	t_{OR}	V_{IN} * GAIN > V_S	25		200		µs
Channel Separation		NCS21802, NCS21804, f = 10 kHz	25		90		dB
EMI Rejection Ratio	EMIRR		25		See Fig. 26		dB
NOISE							
Voltage Noise Density	e_N	f_{in} = 1 kHz	25		53		nV/√Hz
Voltage Noise, Peak−to−Peak	e_{P-P}	f_{in} = 0.1 Hz to 10 Hz	25		400		nV_{PP}
Current Noise Density	i_N	f_{in} = 1 kHz	25		450		fA/√Hz
POWER SUPPLY							
Quiescent Current	I_Q	NCS21801, NCS21803, no load	25		70	95	µA
			0 to 85			**110**	
		NCS21802, NCS21804, per channel, no load	25		65	90	
			0 to 85			**105**	
Quiescent Current in Shutdown (Notes 12, 13)	I_{QSD}	Per channel	25		5	50	nA
			0 to 85			**75**	
Power Supply Rejection Ratio	PSRR	V_S = 1.6 V to 5.5 V	25	115	135		dB
			0 to 85	**110**			
Power Up Time		NCS21801, NCS21803	25		75		µs
		NCS21802, NCS21804	25		40		
Enable Time (Notes 13, 14)	t_{ON}		25		75		µs
Shutdown Time (Notes 13, 14)	t_{OFF}		25		5		µs

12. Guaranteed by design and/or characterization.
13. The enable function is available on NCS21803 only. The EN pin must be connected to a logic low or logic high voltage.
14. Shutdown Time (t_{OFF}) and Enable Time (t_{ON}) are defined as the time between the 50% point of the signal applied to the EN pin and the point at which the output voltage reaches within 10% of its final value.

TYPICAL CHARACTERISTICS

Typical Performance at T_A = 25°C, V_{CM} = mid−supply, C_L = 20 pF, R_L = 10 kΩ to mid−supply, unless otherwise noted

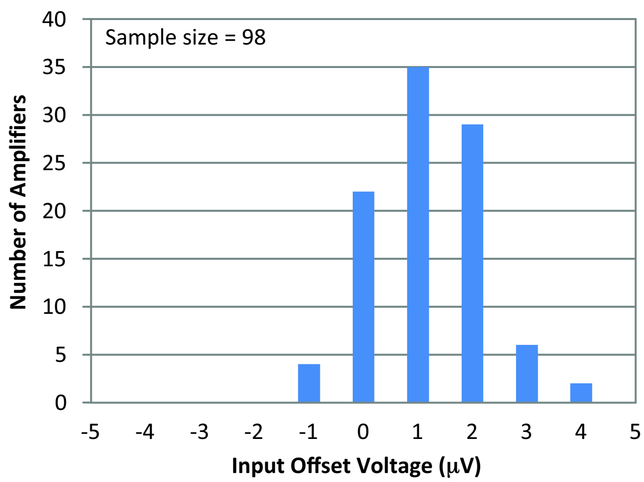


Figure 1. Input Offset Voltage Distribution with 3.3 V Supply

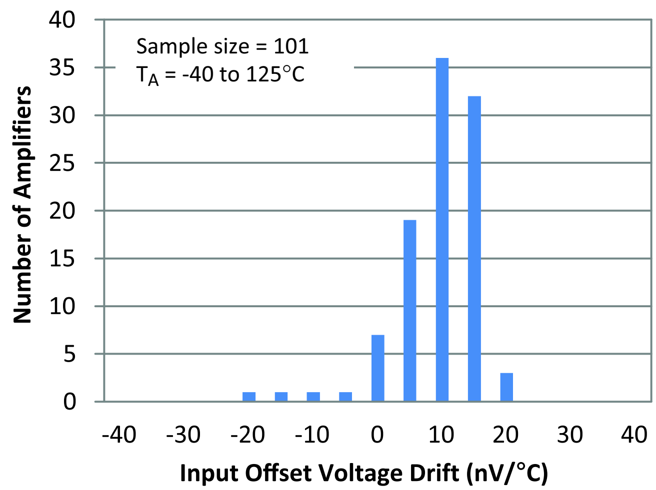


Figure 2. Input Offset Voltage Drift Distribution with 3.3 V Supply

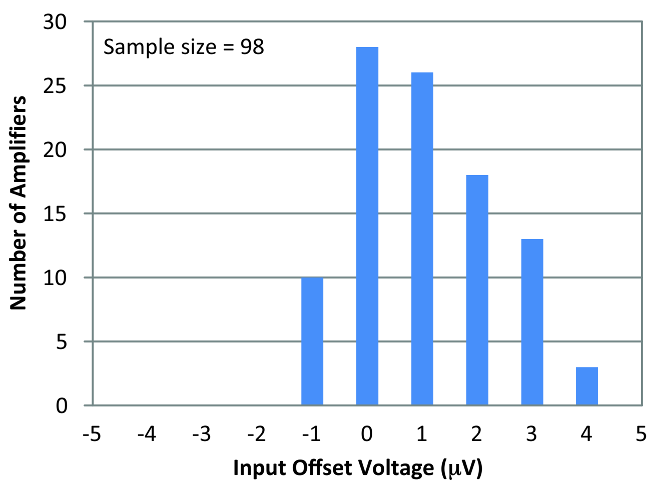


Figure 3. Input Offset Voltage Distribution with 1.6 V Supply

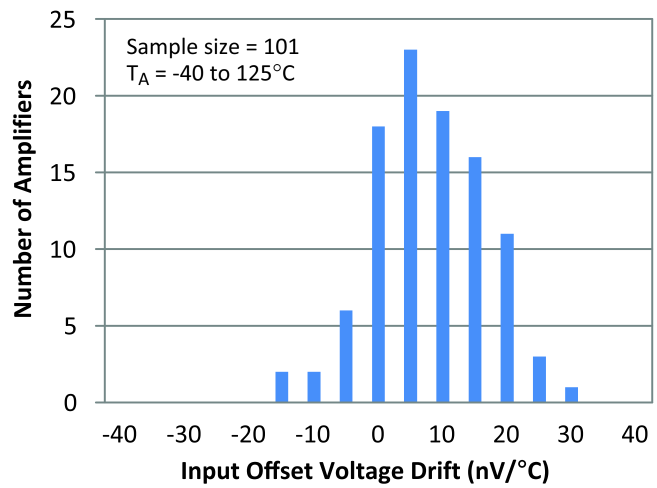


Figure 4. Input Offset Voltage Drift Distribution with 1.6 V Supply

TYPICAL CHARACTERISTICS

Typical Performance at T_A = 25°C, V_{CM} = mid−supply, C_L = 20 pF, R_L = 10 kΩ to mid−supply, unless otherwise noted

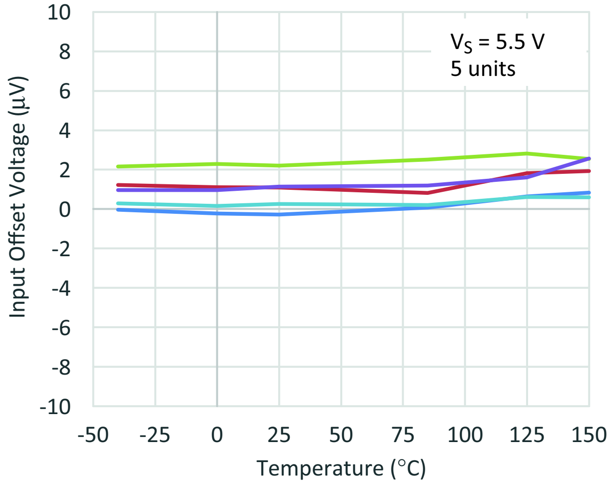


Figure 5. Input Offset Voltage vs. Temperature at 5.5 V Supply

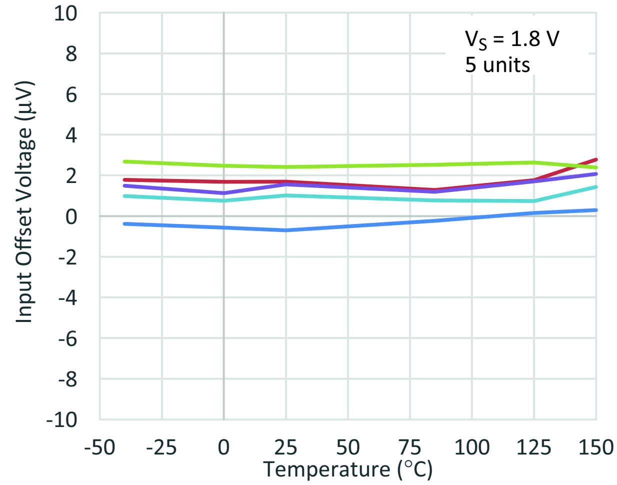


Figure 6. Input Offset Voltage vs. Temperature at 1.8 V Supply

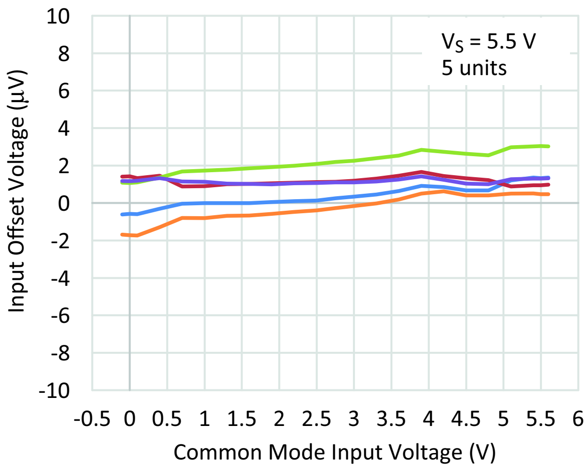


Figure 7. Input Offset Voltage vs. Common Mode Voltage at 5.5 V Supply

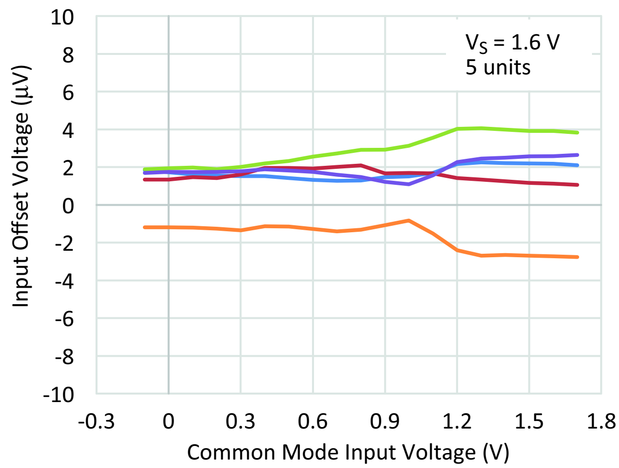


Figure 8. Input Offset Voltage vs. Common Mode Voltage at 1.6 V Supply

TYPICAL CHARACTERISTICS

Typical Performance at T_A = 25°C, V_{CM} = mid−supply, C_L = 20 pF, R_L = 10 kΩ to mid−supply, unless otherwise noted

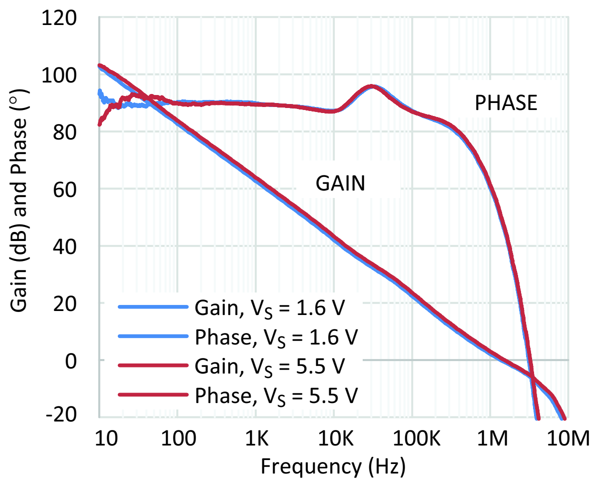


Figure 9. Open Loop Gain and Phase vs. Frequency

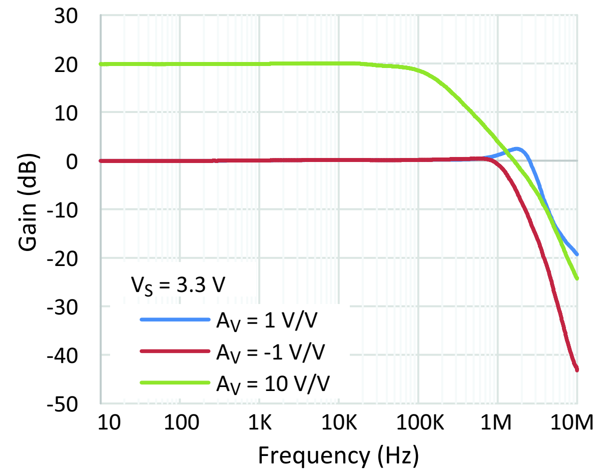


Figure 10. Closed Loop Gain vs. Frequency

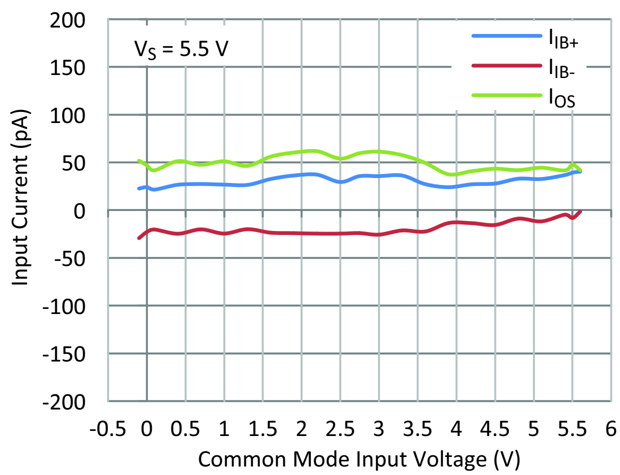


Figure 11. Input Bias Current and Input Offset Current vs. Common Mode Input Voltage

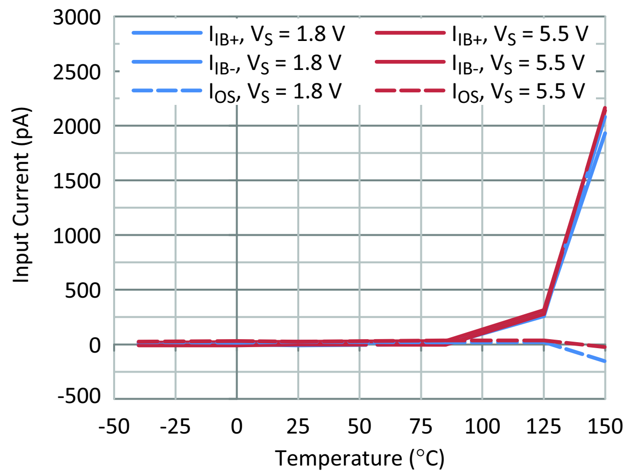


Figure 12. Input Bias Current and Input Offset Current vs. Temperature

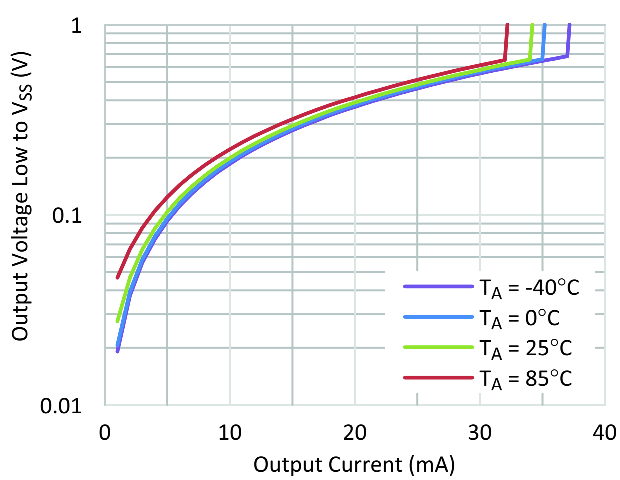


Figure 13. Output Voltage Low vs. Output Current at 5.5 V Supply

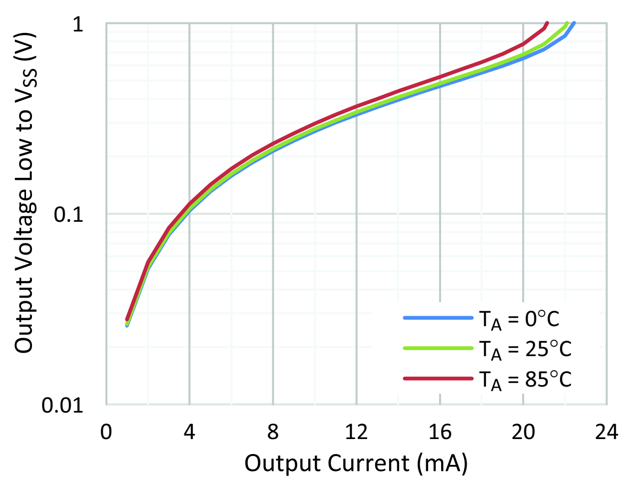


Figure 14. Output Voltage Low vs. Output Current at 1.6 V Supply

TYPICAL CHARACTERISTICS

Typical Performance at T_A = 25°C, V_{CM} = mid−supply, C_L = 20 pF, R_L = 10 kΩ to mid−supply, unless otherwise noted

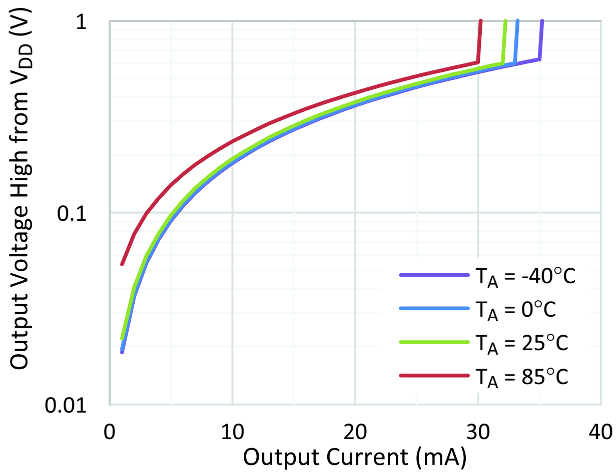


Figure 15. Output Voltage High vs. Output Current at 5.5 V Supply

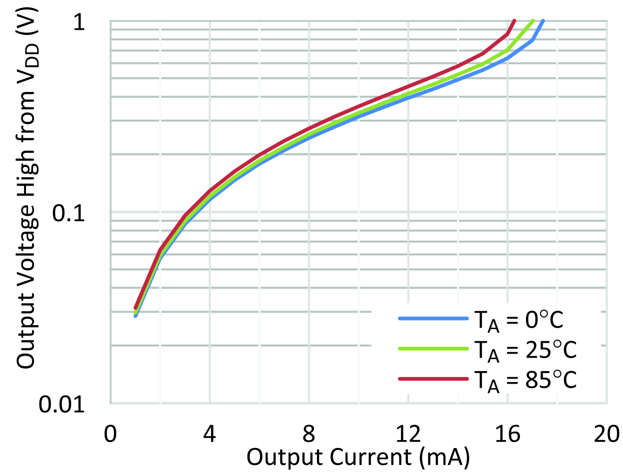


Figure 16. Output Voltage High vs. Output Current at 1.6 V Supply

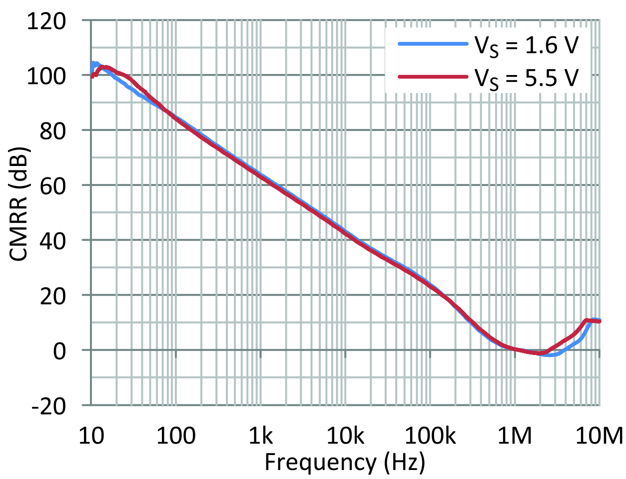


Figure 17. CMRR vs. Frequency

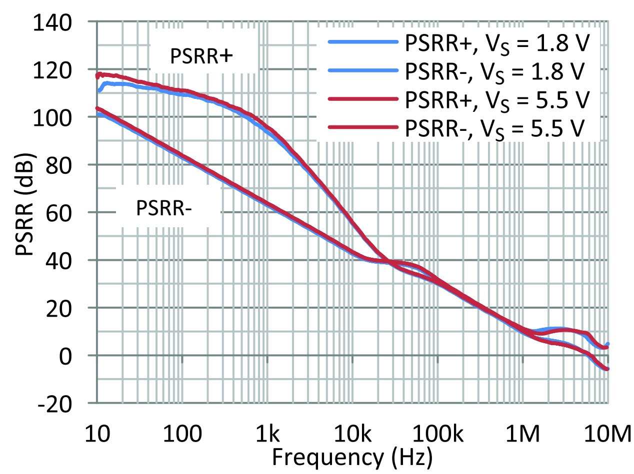


Figure 18. PSRR vs. Frequency

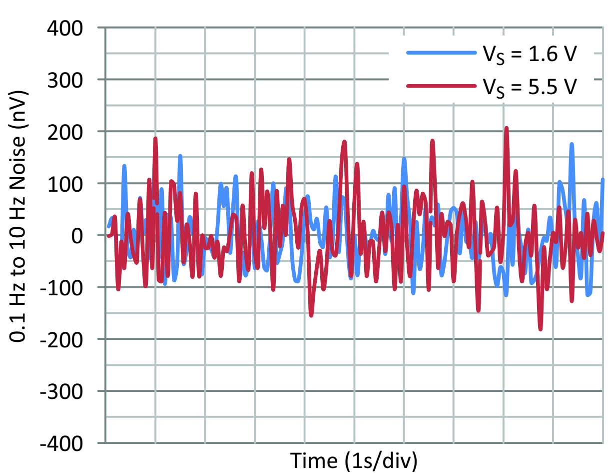


Figure 19. 0.1 Hz to 10 Hz Noise

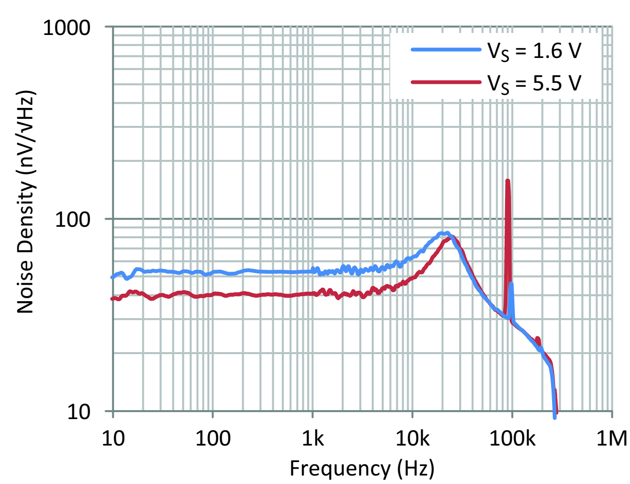


Figure 20. Voltage Noise Density vs. Frequency

TYPICAL CHARACTERISTICS

Typical Performance at T_A = 25°C, V_{CM} = mid−supply, C_L = 20 pF, R_L = 10 kΩ to mid−supply, unless otherwise noted

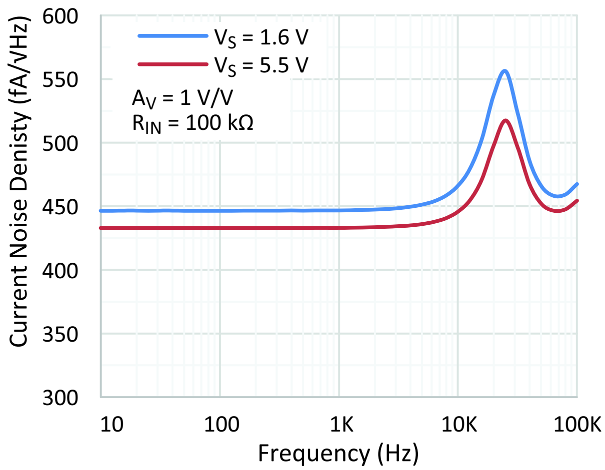


Figure 21. Current Noise Density vs. Frequency

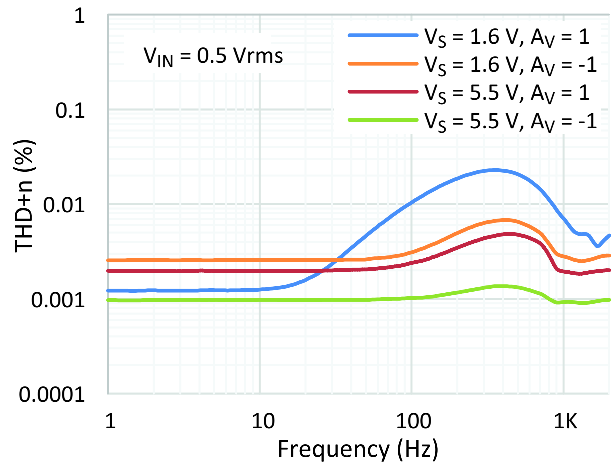


Figure 22. THD+n vs. Frequency

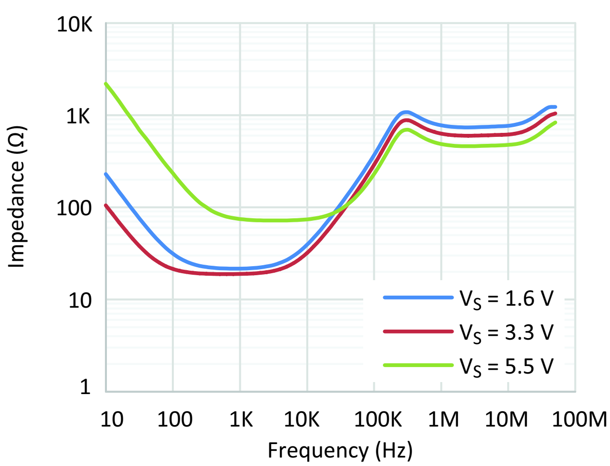


Figure 23. Open Loop Output Impedance vs. Frequency

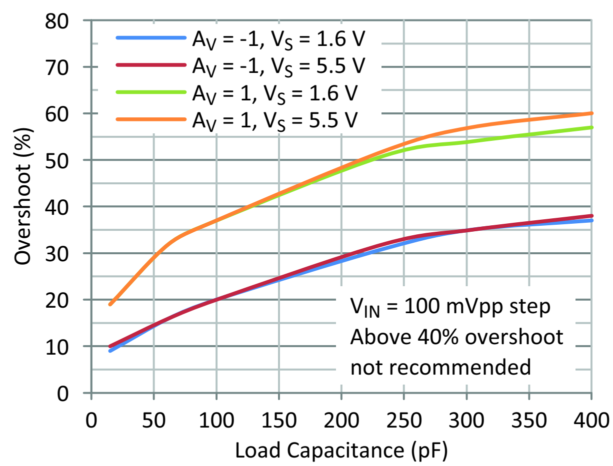


Figure 24. Small Signal Overshoot vs. Load Capacitance

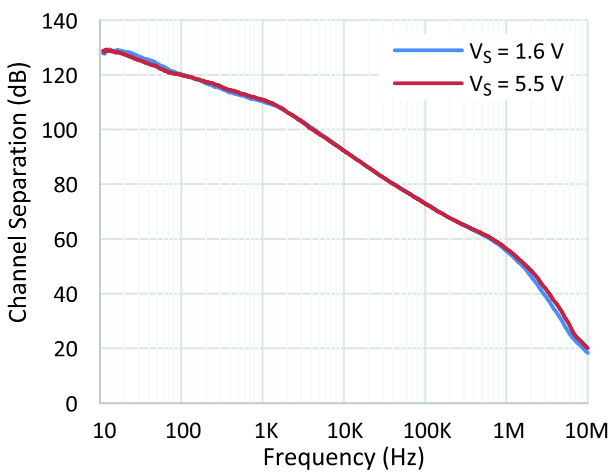


Figure 25. Channel Separation vs. Frequency

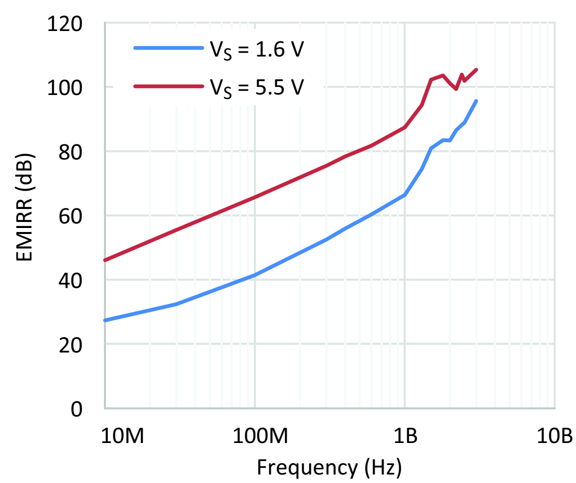


Figure 26. EMIRR vs. Frequency

TYPICAL CHARACTERISTICS

Typical Performance at T_A = 25°C, V_{CM} = mid−supply, C_L = 20 pF, R_L = 10 kΩ to mid−supply, unless otherwise noted

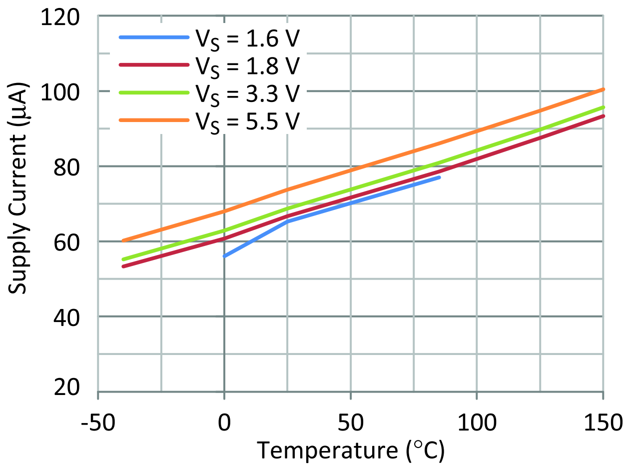


Figure 27. Quiescent Current Per Channel vs. Temperature

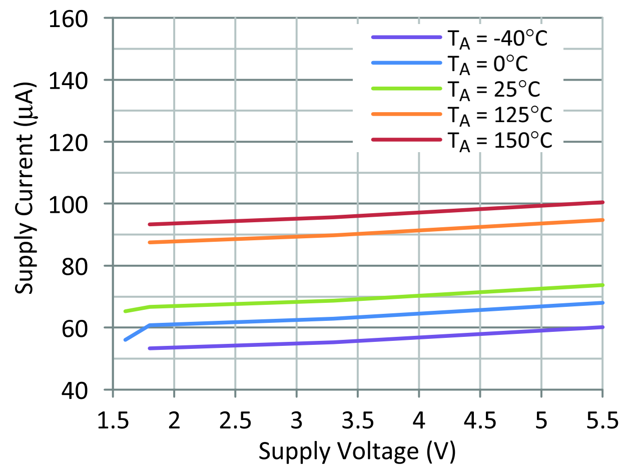


Figure 28. Quiescent Current Per Channel vs. Supply Voltage

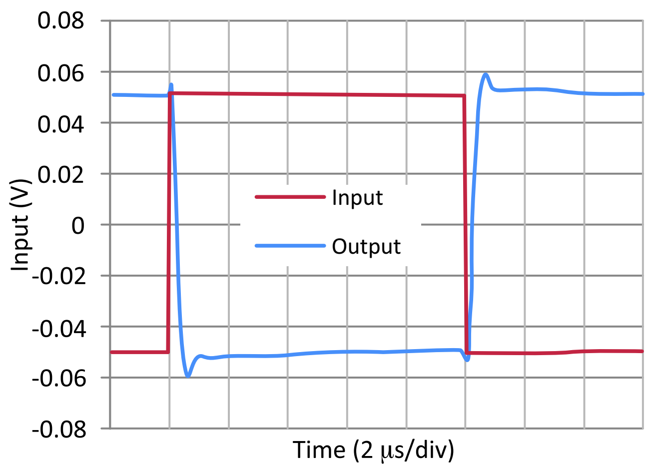


Figure 29. Inverting Small Signal Step Response with V_S = 3.3 V (Split Supplies)

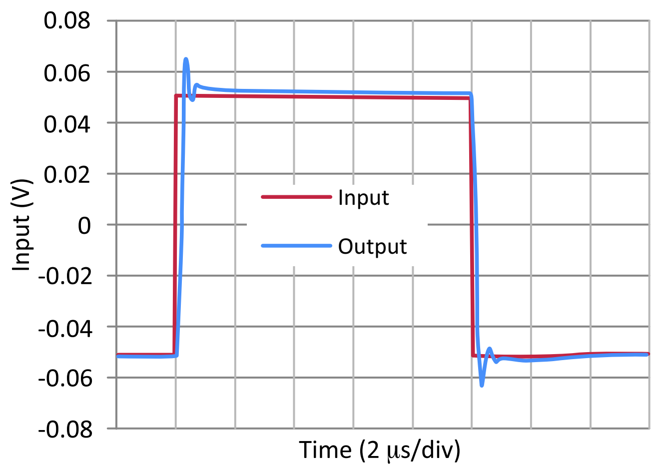


Figure 30. Non−Inverting Small Signal Step Response with V_S = 3.3 V (Split Supplies)

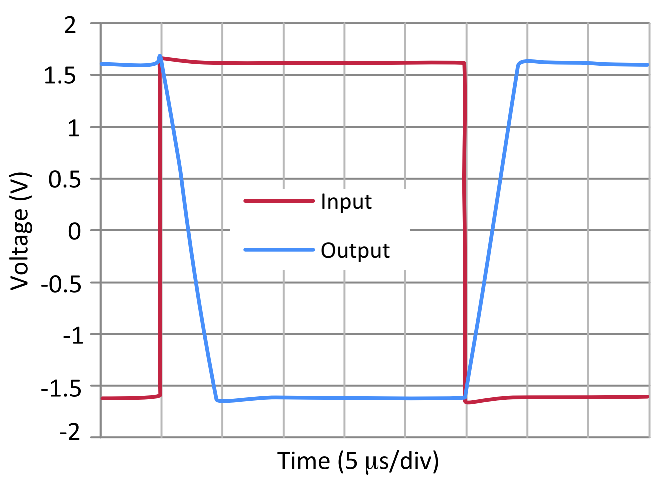


Figure 31. Inverting Large Signal Step Response with V_S = 3.3 V (Split Supply)

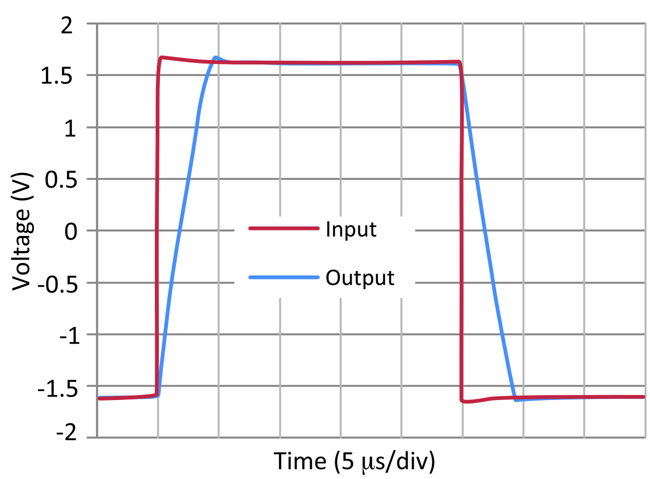


Figure 32. Non−Inverting Large Signal Step Response with V_S =3.3 V (Split Supply)

TYPICAL CHARACTERISTICS

Typical Performance at T_A = 25°C, V_{CM} = mid−supply, C_L = 20 pF, R_L = 10 kΩ to mid−supply, unless otherwise noted

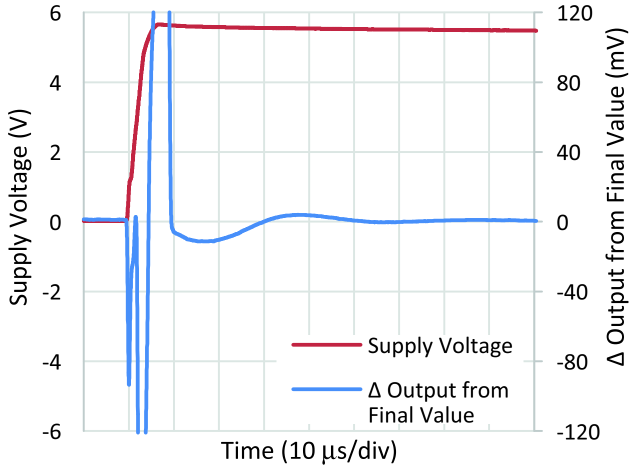


Figure 33. Power Up Time with 5.5 V Supply

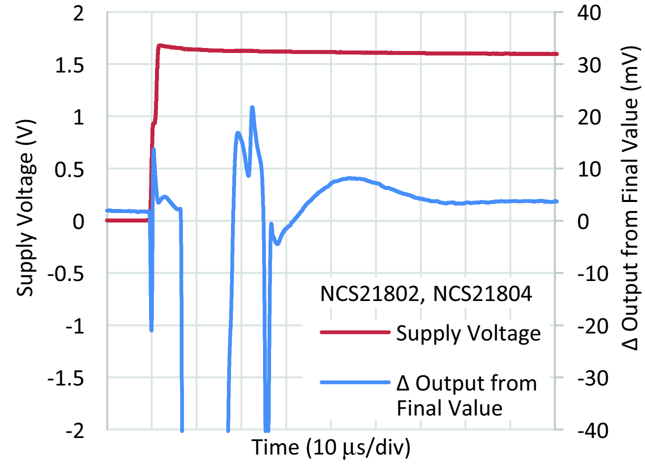


Figure 34. Power Up Time with 1.6 V Supply

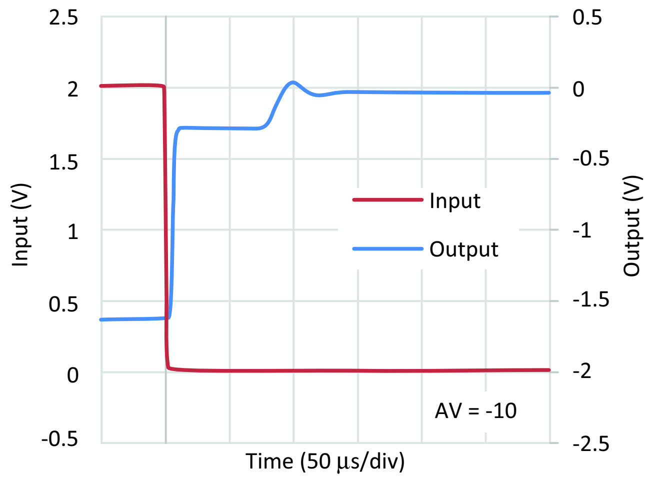


Figure 35. Output Overload Recovery with V_S = 3.3 V (Split Supply)

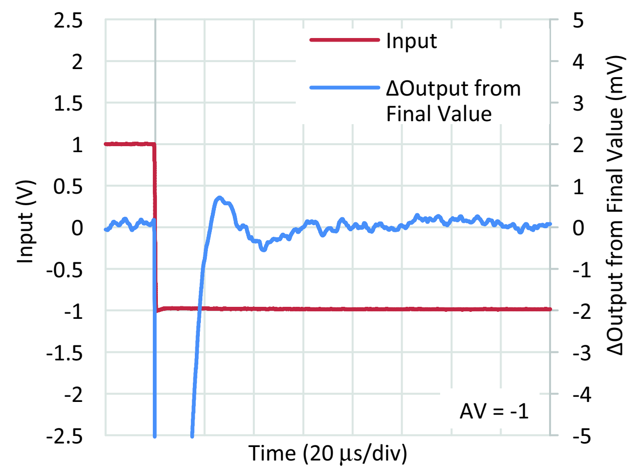


Figure 36. Settling Time with V_S = 3.3 V (Split Supply)

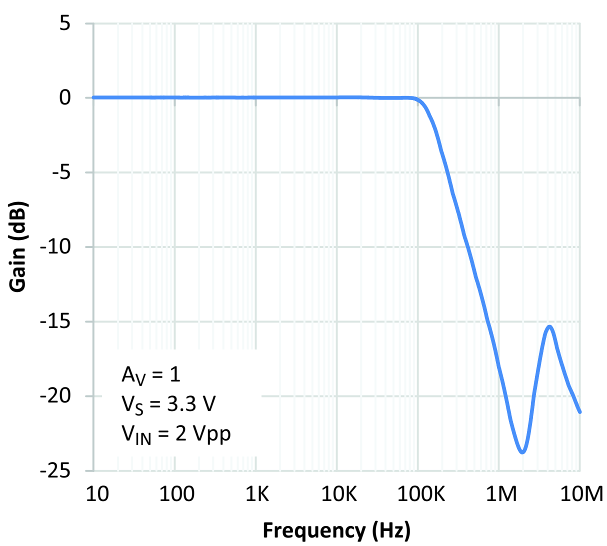


Figure 37. Large Signal Gain vs. Frequency

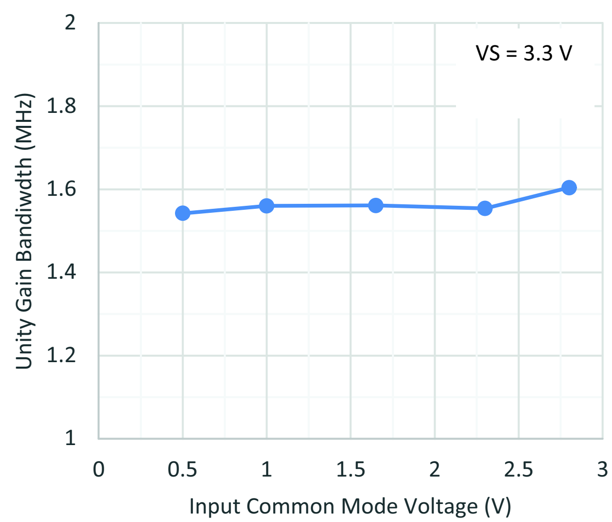


Figure 38. Unity Gain Bandwidth vs. Input Common Mode Voltage

TYPICAL CHARACTERISTICS

Typical Performance at T_A = 25°C, V_{CM} = mid−supply, C_L = 20 pF, R_L = 10 kΩ to mid−supply, unless otherwise noted

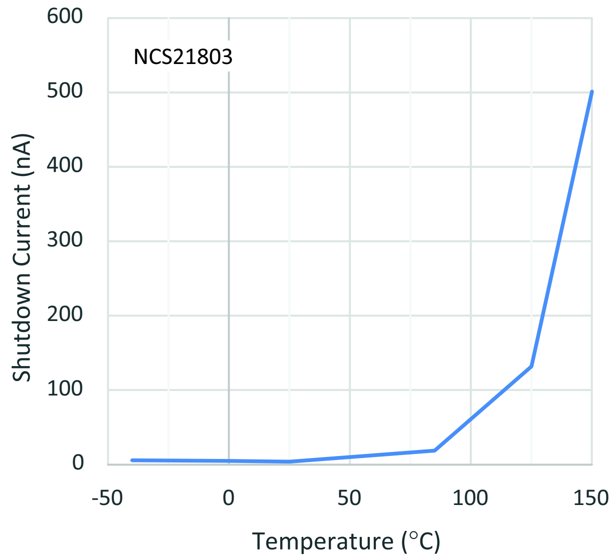


Figure 39. Shutdown Current vs. Temperature

TYPICAL CHARACTERISTICS

Typical Performance at T_A = 25°C, V_{CM} = mid−supply, C_L = 20 pF, R_L = 10 kΩ to mid−supply, unless otherwise noted

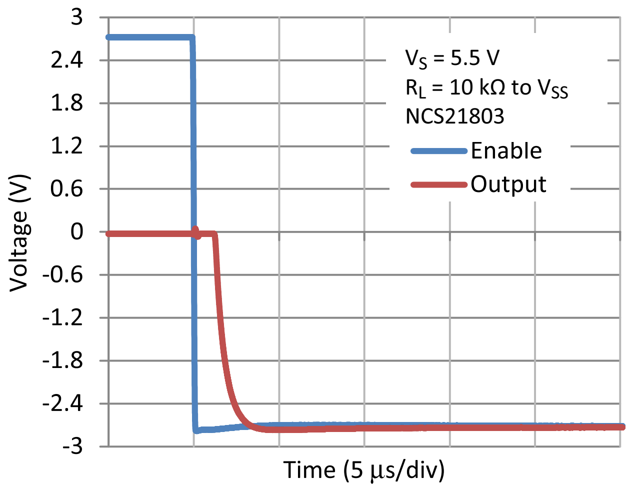


Figure 40. Shutdown Time with V_S = 5.5 V (Split Supply)

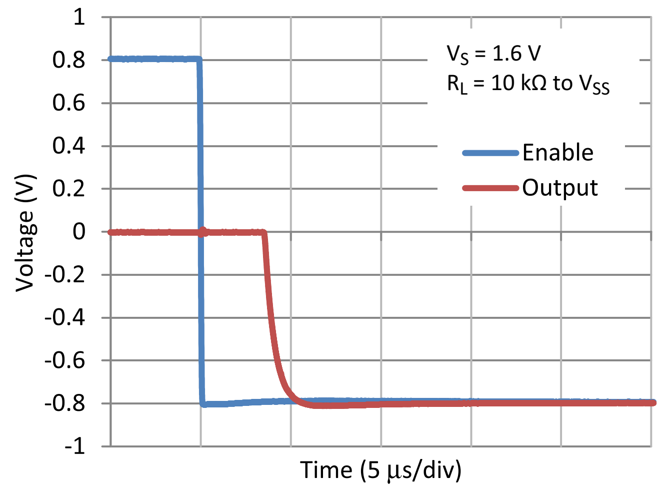


Figure 41. Shutdown Time with V_S = 1.6 V (Split Supply)

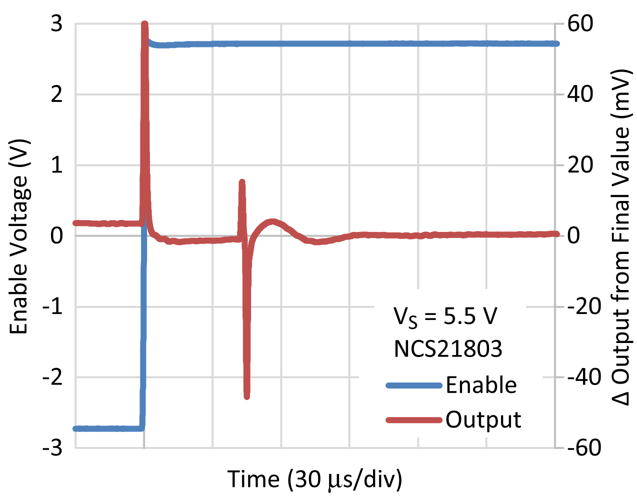


Figure 42. Enable Time with V_S = 5.5 V (Split Supply)

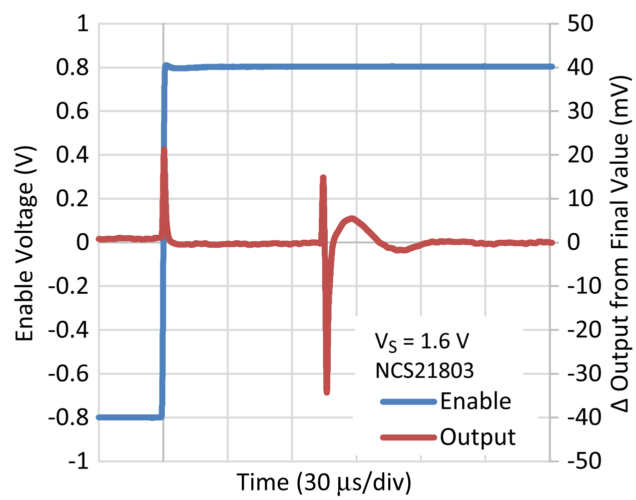


Figure 43. Enable Time with V_S = 1.6 V (Split Supply)

APPLICATIONS INFORMATION

The NCS21801, NCS21802, NCS21803, and NCS21804 precision amplifiers feature low input offset voltage and zero−drift over temperature. The input common mode voltage range extends 100 mV beyond the rails, allowing for measurements at ground or the supply voltage. These characteristics make the NCS21801 series well−suited for applications such as current sensing and sensor interface. The NCS21803 additionally features an enable pin that allows the amplifier to enter shutdown mode to reduce current consumption in low power applications.

Architecture

The low input offset voltage and zero−drift characteristics of amplifiers in the NCS21801 series is achieved through the chopper−stabilized architecture. Unlike the classical chopper architecture, the chopper−stabilized architecture has two signal paths to take advantage of both precision and speed.

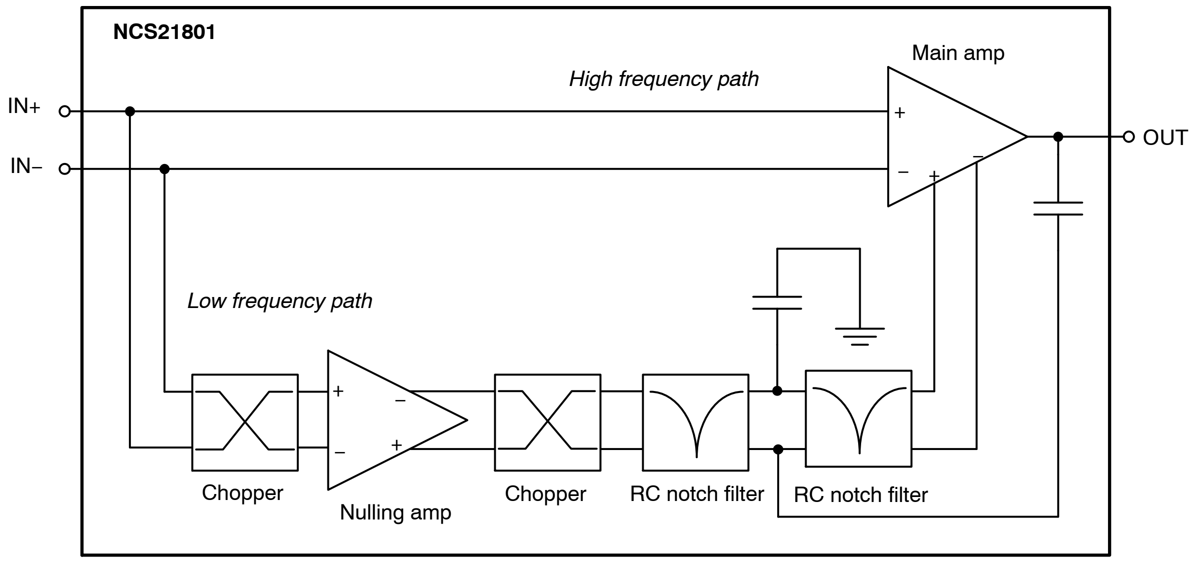


Figure 44. Simplified Schematic of the Chopper−stabilized Amplifier Architecture

In Figure 44, the lower signal path is where the chopper samples the input offset voltage, which is then used to correct the offset at the output. The offset correction occurs at a frequency of 100 kHz. Due to this periodic sampling, the chopper−stabilized architecture is optimized for best performance at frequencies up to the related Nyquist frequency (1/2 of the offset correction frequency). As the signal frequency exceeds the Nyquist frequency, 50 kHz, aliasing may occur at the output. This is an inherent limitation of all chopper and chopper−stabilized architectures. Nevertheless, the NCS2180x is designed to minimize aliasing beyond the Nyquist frequency. ON Semiconductor's patented approach utilizes two cascaded, symmetrical, RC notch filters tuned to the chopper frequency and its fifth harmonic to reduce aliasing effects.

The feed−forward path, which is shown as the upper signal path of the block diagram in Figure 44, is the high speed signal path that extends the gain bandwidth to 1.5 MHz. Not only does this help retain high frequency components of the input signal, but it also improves the loop gain at low frequencies. This is especially useful for low−side current sensing and sensor interface applications where the signal is low frequency and the differential voltage is relatively small.

Both internal amplifiers have specialized circuitry to maintain nearly constant bandwidth, noise, and slew rate over the entire common mode voltage range. This also improves the overall input offset voltage, PSRR, and CMRR performance, while significantly reducing the THD+noise level. These characteristics are very useful in signal processing.

Input Offset Voltage

Input offset voltage is an intrinsic op amp characteristic that arises from mismatches in the IN+ and IN− paths. Since the NCS2180x series amplifiers have such low input offset voltage to begin with, external factors can have a non−trivial contribution to the effective input offset voltage. Conditions created by the physical environment can create package stress, thereby influencing the input offset voltage. These factors include air flow and PCB construction. Taking these factors into consideration, the input offset voltage performance should be validated in the application environment.

EMIRR

The NCS21801 series has built−in input filters to reduce high frequency EMI frequency signals before they enter the amplifier. Under normal circumstances, P−N junctions within the silicon can rectify these high frequency signals, and the effect can be seen as a DC offset at the output. Since this added offset can have a noticeable effect on high precision measurements, EMI rejection ratio (EMIRR) can be used to quantify the robustness of an amplifier to these signals.

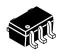
Enable Function

The enable pin on NCS21803 allows the user to put the amplifier into shutdown mode when it is not is use. Setting EN to the logic low level reduces the current consumption down to less than 300 nA, which is useful for portable and battery−powered applications. The output becomes high impedance. Setting the EN pin to logic high enables the output again, with the output reaching the final value (±1%) according the specified enable time. A floating EN pin results in an indeterminate output state.

Layout Recommendations

Bypass capacitors of 0.1 μF to ground should be placed as close as possible to the supply pins.

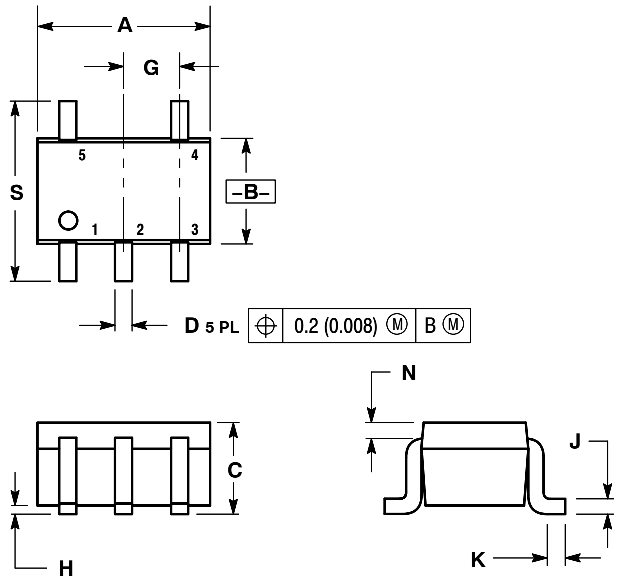
The UDFN8 package has an exposed leadframe die pad on the underside of the package. This pad should be soldered to the PCB, as shown in the recommended soldering footprint in the Package Dimensions section of this datasheet. The center pad can be electrically connected to VSS or it may be left floating. When connected to VSS, the center pad acts as a heat sink, improving the thermal resistance of the part.



SCALE 2:1

SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE L

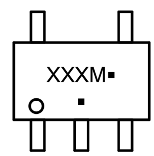
DATE 17 JAN 2013



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

GENERIC MARKING DIAGRAM*

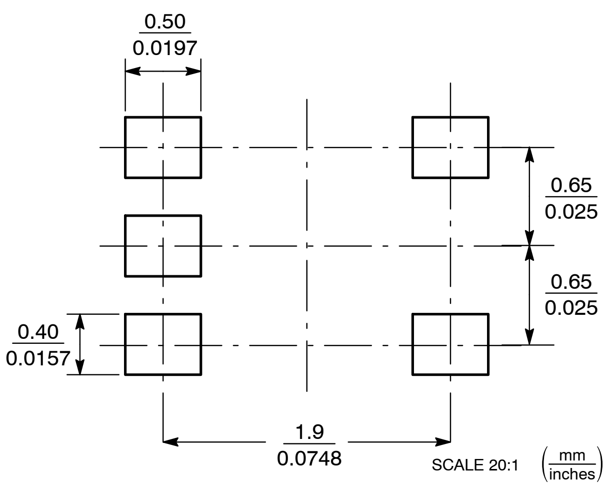


XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

SOLDER FOOTPRINT



STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

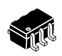
DOCUMENT NUMBER:	98ASB42984B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SC−88A (SC−70−5/SOT−353)	PAGE 1 OF 1

ON Semiconductor®

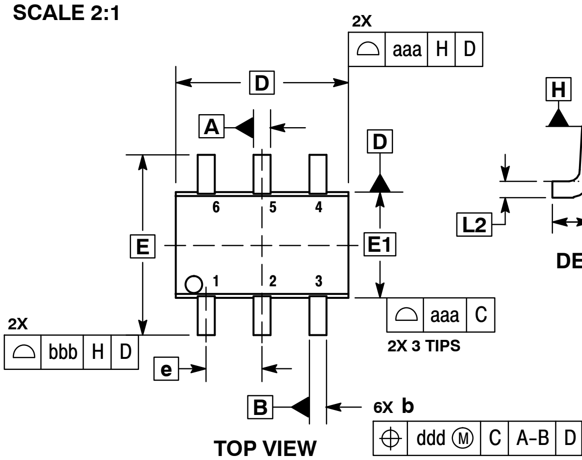
SC−88/SC70−6/SOT−363

CASE 419B−02
ISSUE Y

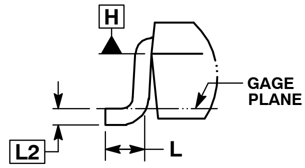
DATE 11 DEC 2012



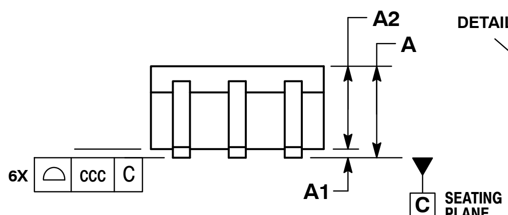
1
SCALE 2:1



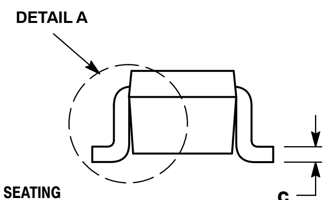
TOP VIEW



DETAIL A



SIDE VIEW

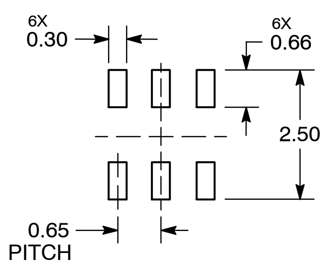


END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e		0.65 BSC			0.026 BSC	
L	0.26	0.36	0.46	0.010	0.014	0.018
L2		0.15 BSC			0.006 BSC	
aaa		0.15			0.006	
bbb		0.30			0.012	
ccc		0.10			0.004	
ddd		0.10			0.004	

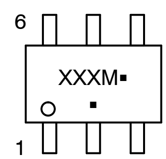
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42985B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SC−88/SC70−6/SOT−363	PAGE 1 OF 2

SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE Y

DATE 11 DEC 2012

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. COLLECTOR
4. EMITTER
5. BASE
6. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. EMITTER 2
2. EMITTER 1
3. COLLECTOR 1
4. BASE 1
5. BASE 2
6. COLLECTOR 2

STYLE 10:
PIN 1. SOURCE 2
2. SOURCE 1
3. GATE 1
4. DRAIN 1
5. DRAIN 2
6. GATE 2

STYLE 11:
PIN 1. CATHODE 2
2. CATHODE 2
3. ANODE 1
4. CATHODE 1
5. CATHODE 1
6. ANODE 2

STYLE 12:
PIN 1. ANODE 2
2. ANODE 2
3. CATHODE 1
4. ANODE 1
5. ANODE 1
6. CATHODE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 15:
PIN 1. ANODE 1
2. ANODE 2
3. ANODE 3
4. CATHODE 3
5. CATHODE 2
6. CATHODE 1

STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

STYLE 18:
PIN 1. VIN1
2. VCC
3. VOUT2
4. VIN2
5. GND
6. VOUT1

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

STYLE 20:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 21:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. N/C
6. CATHODE 1

STYLE 22:
PIN 1. D1 (i)
2. GND
3. D2 (i)
4. D2 (c)
5. VBUS
6. D1 (c)

STYLE 23:
PIN 1. Vn
2. CH1
3. Vp
4. N/C
5. CH2
6. N/C

STYLE 24:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 25:
PIN 1. BASE 1
2. CATHODE
3. COLLECTOR 2
4. BASE 2
5. EMITTER
6. COLLECTOR 1

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 27:
PIN 1. BASE 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. EMITTER 2
6. COLLECTOR 2

STYLE 28:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

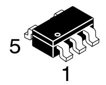
STYLE 29:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE/ANODE
6. CATHODE

STYLE 30:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1

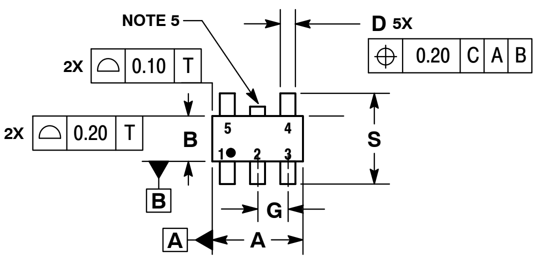
Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

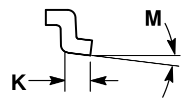
TSOP−5
CASE 483
ISSUE N

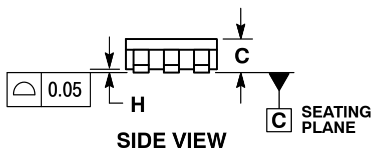
DATE 12 AUG 2020

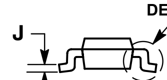


SCALE 2:1





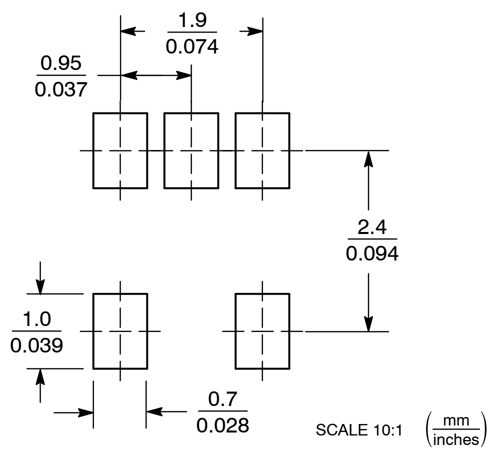




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

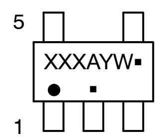
	MILLIMETERS	
DIM	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0 °	10 °
S	2.50	3.00

SOLDERING FOOTPRINT*

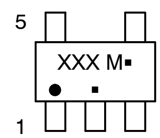


*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



Analog



Discrete/Logic

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

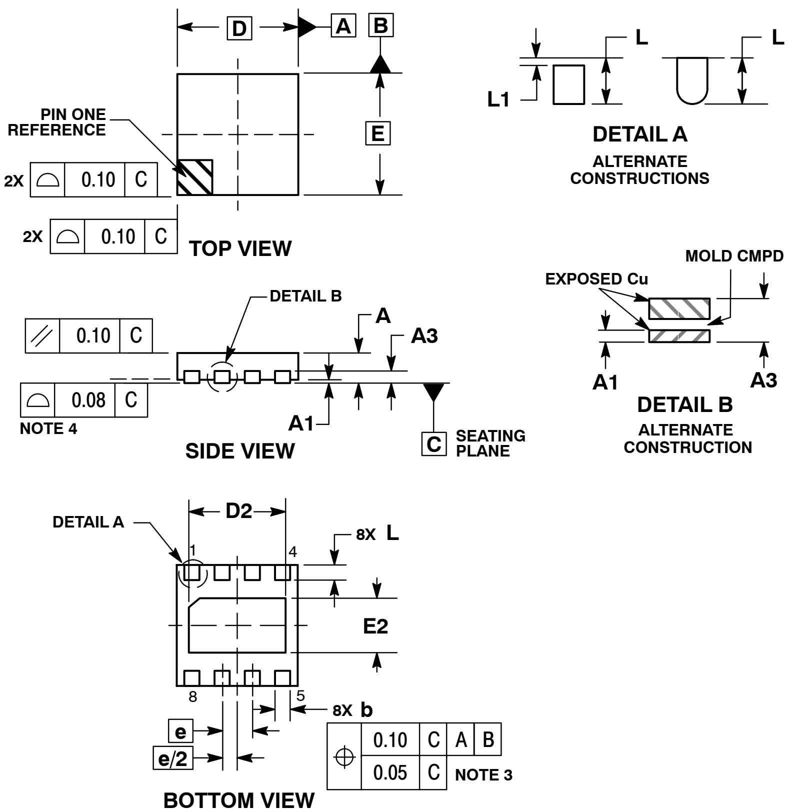
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	98ARB18753C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	TSOP−5	PAGE 1 OF 1

SCALE 2:1

UDFN8, 2x2
CASE 517AW
ISSUE A

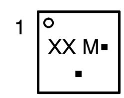
DATE 13 NOV 2015



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. FOR DEVICE OPN CONTAINING W OPTION, DETAIL B ALTERNATE CONSTRUCTION IS NOT APPLICABLE.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.18	0.30
D	2.00 BSC	
D2	1.50	1.70
E	2.00 BSC	
E2	0.80	1.00
e	0.50 BSC	
L	0.20	0.45
L1	---	0.15

GENERIC MARKING DIAGRAM*

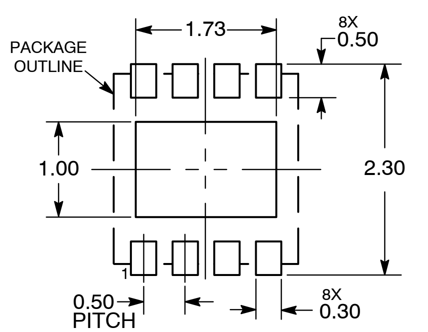


XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

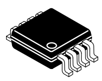
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

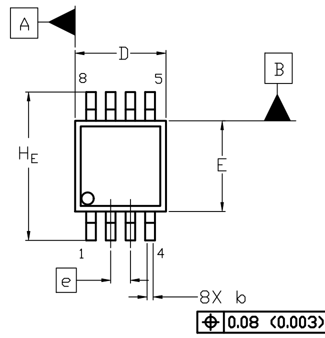
DOCUMENT NUMBER:	98AON34462E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	UDFN8, 2X2	PAGE 1 OF 1



SCALE 2:1

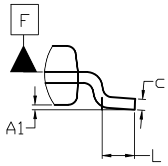
Micro8
CASE 846A−02
ISSUE K

DATE 16 JUL 2020



TOP VIEW

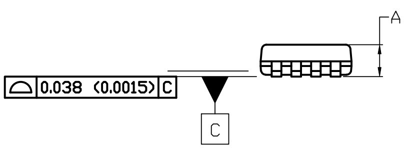
NOTE 3



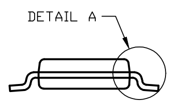
DETAIL A

NOTES:

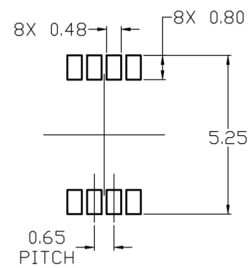
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



SIDE VIEW



END VIEW

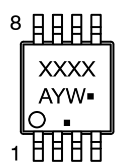


RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
b	0.25	0.33	0.40
c	0.13	0.18	0.23
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.65 BSC		
H_E	4.75	4.90	5.05
L	0.40	0.55	0.70

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

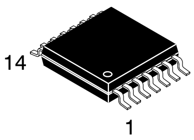
STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:
PIN 1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

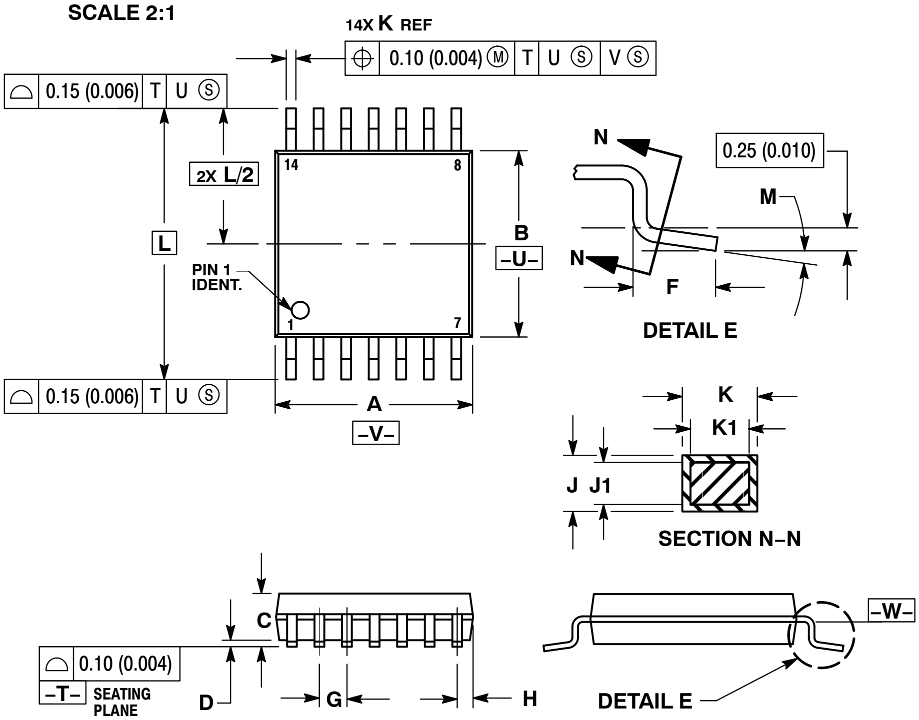
DOCUMENT NUMBER:	98ASB14087C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	MICRO8	PAGE 1 OF 1

TSSOP−14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016



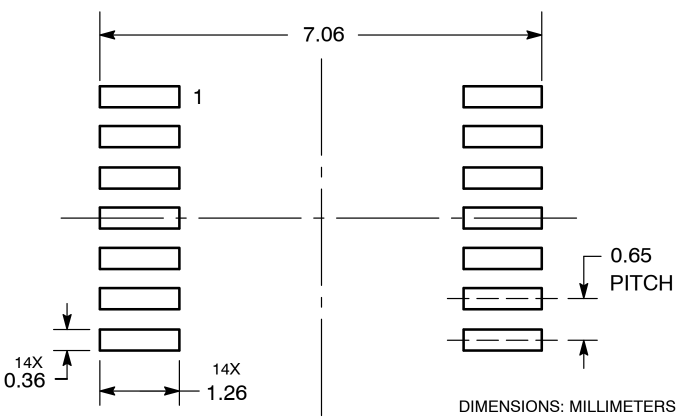
SCALE 2:1



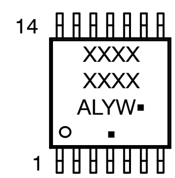
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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