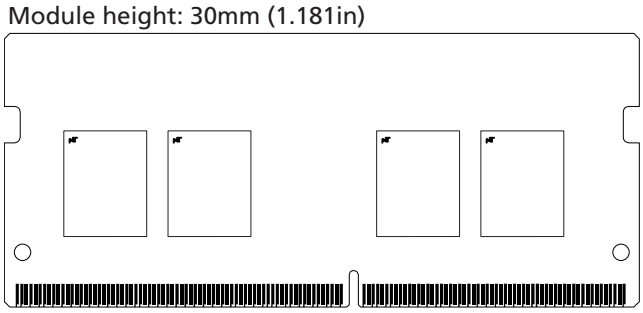
DDR4 SDRAM SODIMM

MTA8ATF51264HZ – 4GB

Features

- DDR4 functionality and operations supported as defined in the component data sheet
- 260-pin, small-outline dual in-line memory module (SODIMM)
- Fast data transfer rates: PC4-2400, PC4-2133, or PC4-1866
- 4GB (512 Meg x 72)
- V_{DD} = 1.20V (TYP)
- V_{PP} = 2.5V (TYP)
- V_{DDSPD} = 2.2–3.6V
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Low-power auto self refresh (LPASR)
- Data bus inversion (DBI) for data bus
- On-die V_{REFDQ} generation and calibration
- Single-rank
- Onboard I^2C serial presence-detect (SPD) EEPROM
- 16 internal banks; 4 groups of 4 banks each
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control command and address bus

Figure 1: 260-Pin SODIMM (MO-310 R/C A)



Options	Marking
• Operating temperature	
– Commercial (0°C ≤ T_{OPER} ≤ 95°C)	None
• Package	
– 256-pin DIMM (halogen-free)	Z
• Frequency/CAS latency	
– 0.83ns @ CL = 16 (DDR4-2400)	-2G4
– 0.93ns @ CL = 15 (DDR4-2133)	-2G1
– 1.07ns @ CL = 13 (DDR4-1866)	-1G9

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)								^tRCD (ns)	^tRP (ns)	^tRC (ns)
		CL = 18	CL = 16	CL = 15	CL = 14	CL = 13	CL = 12	CL = 11	CL = 9			
-2G4	PC4-2400	2400	2400	2133	1866	1866	1600	1600	1333	13.32	13.32	45.32
-2G1	PC4-2133	–	2133	2133	1866	1866	1600	1600	1333	13.5	13.5	46.5
-1G9	PC4-1866	–	–	–	1866	1866	1600	1600	1333	13.5	13.5	47.5

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Table 2: Addressing

Parameter	4GB
Row address	32K A[14:0]
Column address	1K A[9:0]
Device bank group address	4 BG[1:0]
Device bank address per group	4 BA[1:0]
Device configuration	4Gb (512 Meg x 8), 16 banks
Module rank address	CS0_n

Table 3: Part Numbers and Timing Parameters – 4GB Modules

Base device: MT40A512M8,[1] 4Gb DDR4 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MTA8ATF51264HZ-2G4__	4GB	512 Meg x 72	19.2 GB/s	0.83ns/2400 MT/s	16-16-16
MTA8ATF51264HZ-2G1__	4GB	512 Meg x 72	17.0 GB/s	0.93ns/2133 MT/s	15-15-15
MTA8ATF51264HZ-1G9__	4GB	512 Meg x 72	14.9 GB/s	1.07ns/1866 MT/s	13-13-13

Notes:
1. The data sheet for the base device can be found on micron.com
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MTA8ATF51264HZ-2G1A1.

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Pin Assignments

Table 4: Pin Assignments

260-Pin DDR4 SODIMM Front								260-Pin DDR4 SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	67	DQ29	133	A1	199	DM5_n/ DBI5_n	2	V_{SS}	68	V_{SS}	134	EVENT_n, NF	200	DQS5_t
3	DQ5	69	V_{SS}	135	V_{DD}	201	V_{SS}	4	DQ4	70	DQ24	136	V_{DD}	202	V_{SS}
5	V_{SS}	71	DQ25	137	CK0_t	203	DQ46	6	V_{SS}	72	V_{SS}	138	CK1_t/NF	204	DQ47
7	DQ1	73	V_{SS}	139	CK0_c	205	V_{SS}	8	DQ0	74	DQS3_c	140	CK1_c/NF	206	V_{SS}
9	V_{SS}	75	DM3_n/ DBI3_n	141	V_{DD}	207	DQ42	10	V_{SS}	76	DQS3_t	142	V_{DD}	208	DQ43
11	DQS0_c	77	V_{SS}	143	PARITY	209	V_{SS}	12	DM0_n/ DBI0_n	78	V_{SS}	144	A0	210	V_{SS}
13	DQS0_t	79	DQ30	145	BA1	211	DQ52	14	V_{SS}	80	DQ31	146	A10/AP	212	DQ53
15	V_{SS}	81	V_{SS}	147	V_{DD}	213	V_{SS}	16	DQ6	82	V_{SS}	148	V_{DD}	214	V_{SS}
17	DQ7	83	DQ26	149	CS0_n	215	DQ49	18	V_{SS}	84	DQ27	150	BA0	216	DQ48
19	V_{SS}	85	V_{SS}	151	WE_n/ A14	217	V_{SS}	20	DQ2	86	V_{SS}	152	RAS_n/ A16	218	V_{SS}
21	DQ3	87	CB5/NC	153	V_{DD}	219	DQS6_c	22	V_{SS}	88	CB4/NC	154	V_{DD}	220	DM6_n/ DBI6_n
23	V_{SS}	89	V_{SS}	155	ODT0	221	DQS6_t	24	DQ12	90	V_{SS}	156	CAS_n/ A15	222	V_{SS}
25	DQ13	91	CB1/NC	157	CS1_n	223	V_{SS}	26	V_{SS}	92	CB0/NC	158	A13	224	DQ54
27	V_{SS}	93	V_{SS}	159	V_{DD}	225	DQ55	28	DQ8	94	V_{SS}	160	V_{DD}	226	V_{SS}
29	DQ9	95	DQS8_c	161	ODT1	227	V_{SS}	30	V_{SS}	96	DM8_n/ DBI_n/NC	162	C0/ CS2_n/NC	228	DQ50
31	V_{SS}	97	DQS8_t	163	V_{DD}	229	DQ51	32	DQS1_c	98	V_{SS}	164	V_{REFCA}	230	V_{SS}
33	DM1_n/ DBI_n	99	V_{SS}	165	C1, CS3_n, NC	231	V_{SS}	34	DQS1_t	100	CB6/NC	166	SA2	232	DQ60
35	V_{SS}	101	CB2/NC	167	V_{SS}	233	DQ61	36	V_{SS}	102	V_{SS}	168	V_{SS}	234	V_{SS}
37	DQ15	103	V_{SS}	169	DQ37	235	V_{SS}	38	DQ14	104	CB7/NC	170	DQ36	236	DQ57
39	V_{SS}	105	CB3/NC	171	V_{SS}	237	DQ56	40	V_{SS}	106	V_{SS}	172	V_{SS}	238	V_{SS}
41	DQ10	107	V_{SS}	173	DQ33	239	V_{SS}	42	DQ11	108	RESET_n	174	DQ32	240	DQS7_c
43	V_{SS}	109	CKE0	175	V_{SS}	241	DM7_n/ DBI7_n	44	V_{SS}	110	CKE1	176	V_{SS}	242	DQS7_t
45	DQ21	111	V_{DD}	177	DQS4_c	243	V_{SS}	46	DQ20	112	V_{DD}	178	DM4_n/ DBI4_n	244	V_{SS}
47	V_{SS}	113	BG1	179	DQS4_t	245	DQ62	48	V_{SS}	114	ACT_n	180	V_{SS}	246	DQ63
49	DQ17	115	BG0	181	V_{SS}	247	V_{SS}	50	DQ16	116	ALERT_n	182	DQ39	248	V_{SS}
51	V_{SS}	117	V_{DD}	183	DQ38	249	DQ58	52	V_{SS}	118	V_{DD}	184	V_{SS}	250	DQ59
53	DQS2_c	119	A12	185	V_{SS}	251	V_{SS}	54	DM2_n/ DBI2_n	120	A11	186	DQ35	252	V_{SS}
55	DQS2_t	121	A9	187	DQ34	253	SCL	56	V_{SS}	122	A7	188	V_{SS}	254	SDA
57	V_{SS}	123	V_{DD}	189	V_{SS}	255	V_{DDSPD}	58	DQ22	124	V_{DD}	190	DQ45	256	SA0
59	DQ23	125	A8	191	DQ44	257	V_{PP}	60	V_{SS}	126	A5	192	V_{SS}	258	V_{TT}
61	V_{SS}	127	A6	193	V_{SS}	259	V_{PP}	62	DQ18	128	A4	194	DQ41	260	SA1
63	DQ19	129	V_{DD}	195	DQ40	–	–	64	V_{SS}	130	V_{DD}	196	V_{SS}	–	–
65	V_{SS}	131	A3	197	V_{SS}	–	–	66	DQ28	132	A2	198	DQS5_c	–	–

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Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for DDR4 modules. All pins listed may not be supported on this module. See Functional Block Diagram for pins specific to this module.

Table 5: Pin Descriptions

Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands in order to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, and RAS_n/A16 have additional functions; see individual entries in this table.) The address inputs also provide the op-code during the MODE REGISTER SET command. A17 is only defined for x4 SDRAM.
A10/AP	Input	**Auto precharge:** A10 is sampled during READ and WRITE commands to determine whether an auto precharge should be performed on the accessed bank after a READ or WRITE operation. (HIGH = auto precharge; LOW = no auto precharge.) A10 is sampled during a PRECHARGE command to determine whether the precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses.
A12/BC_n	Input	**Burst chop:** A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. (HIGH = no burst chop; LOW = burst- chopped.) See Command Truth Table in the DDR4 component data sheet.
ACT_n	Input	**Command input:** ACT_n defines the ACTIVATE command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 are considered as row address A16, A15, and A14. See Command Truth Table.
BAx	Input	**Bank address inputs:** Define the bank (with a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command.
BGx	Input	**Bank group address inputs:** Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations. x16-based SDRAM only has BG0.
C0, C1, C2 (RDIMM/LRDIMM only)	Input	**Chip ID:** These inputs are used only when devices are stacked; that is, 2H, 4H, and 8H stacks for x4 and x8 configurations using through-silicon vias (TSVs). These pins are not used in the x16 configuration. Some DDR4 modules support a traditional DDP package, which uses CS1_n, CKE1, and ODT1 to control the second die. All other stack configurations, such as a 4H or 8H, are assumed to be single-load (master/slave) type configurations where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT. Chip ID is considered part of the command code.
CKx_t CKx_c	Input	**Clock:** Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.

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Table 5: Pin Descriptions (Continued)

Symbol	Type	Description
CKEx	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit. After V_{REFCA} has become stable during the power-on and initialization sequence, it must be maintained during all operations (including SELF REFRESH). CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK_t, CK_c, ODT, RESET_n, and CKE) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during self refresh.
CSx_n	Input	**Chip select:** All commands are masked when CS_n is registered HIGH. CS_n provides external rank selection on systems with multiple ranks. CS_n is considered part of the command code. (CS2_n and CS3_n are not used on UDIMMs.)
ODTx	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT (R_{TT}) is applied only to each DQ, DQS_t, DQS_c, DM_n/DBI_n/TDQS_t, and TDQS_c signal for x4 and x8 configurations (when the TDQS function is enabled via the mode register). For the x16 configuration, R_{TT} is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, UDM_n, and LDM_n signal. The ODT pin will be ignored if the mode registers are programmed to disable R_{TT}.
PARITY	Input	**Parity for command and address:** This function can be enabled or disabled via the mode register. When enabled in MR5, the DRAM calculates parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG[1:0], BA[1:0], A[16:0]. Input parity should be maintained at the rising edge of the clock and at the same time as command and address with CS_n LOW.
RAS_n/A16 CAS_n/A15 WE_n/A14	Input	**Command inputs:** RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n) define the command and/or address being entered and have multiple functions. For example, for activation with ACT_n LOW, these are addresses like A16, A15, and A14, but for a non-activation command with ACT_n HIGH, these are command pins for READ, WRITE, and other commands defined in Command Truth Table.
RESET_n	CMOS Input	**Active LOW asynchronous reset:** Reset is active when RESET_n is LOW and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
SAx	Input	**Serial address inputs:** Used to configure the temperature sensor/SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I^2C bus.
DQx, CBx	I/O	**Data input/output and check bit input/output:** Bidirectional data bus. DQ represents DQ[3:0], DQ[7:0], and DQ[15:0] for the x4, x8, and x16 configurations, respectively. If cyclic redundancy checksum (CRC) is enabled via the mode register, the CRC code is added at the end of the data burst. Any one or all of DQ0, DQ1, DQ2, or DQ3 may be used for monitoring of internal V_{REF} level during test via mode register setting MR[4] A[4] = HIGH; training times change when enabled.

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Table 5: Pin Descriptions (Continued)

Symbol	Type	Description
DM_n/DBI_n/ TDQS_t (DMU_n, DBIU_n), (DML_n/ DBIl_n)	I/O	**Input data mask and data bus inversion:** DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM is multiplexed with the DBI function by the mode register A10, A11, and A12 settings in MR5. For a x8 device, the function of DM or TDQS is enabled by the mode register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 device and not inverted if DBI_n is HIGH. TDQS is only supported in x8 SDRAM configurations. (TDQS is not valid for UDIMMs.)
SDA	I/O	**Serial Data:** Bidirectional signal used to transfer data in or out of the EEPROM or EEPROM/TS combo device.
DQS_t DQS_c DQSU_t DQSU_c DQSL_t DQSL_c	I/O	**Data strobe:** Output with read data, input with write data. Edge-aligned with read data, centered-aligned with write data. For x16 configurations, DQSL corresponds to the data on DQ[7:0], and DQSU corresponds to the data on DQ[15:8]. For the x4 and x8 configurations, DQS corresponds to the data on DQ[3:0] and DQ[7:0], respectively. DDR4 SDRAM supports a differential data strobe only and does not support a single-ended data strobe.
ALERT_n	Output	**Alert output:** Possesses functions such as CRC error flag and command and address parity error flag as output signal. If a CRC error occurs, ALERT_n goes LOW for the period time interval and returns HIGH. If an error occurs during a command address parity check, ALERT_n goes LOW until the on-going DRAM internal recovery transaction is complete. During connectivity test mode, this pin functions as an input. Use of this signal is system-dependent. If not connected as signal, ALERT_n pin must be connected to V_{DD} on DIMMs.
EVENT_n	Output	**Temperature event:** The EVENT_n pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded. This pin has no function (NF) on modules without temperature sensors.
TDQS_t TDQS_c (x8 DRAM-based RDIMM only)	Output	**Termination data strobe:** When enabled via the mode register, the DRAM device enables the same R_{TT} termination resistance on TDQS_t and TDQS_c that is applied to DQS_t and DQS_c. When the TDQS function is disabled via the mode register, the DM/TDQS_t pin provides the data mask (DM) function, and the TDQS_c pin is not used. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations. The DM function is supported only in x8 and x16 configurations. DM, DBI, and TDQS are a shared pin and are enabled/disabled by mode register settings. For more information about TDQS, see the DDR4 DRAM component data sheet. (TDQS_t and TDQS_c are not valid for UDIMMs.)
V_{DD}	Supply	**Module power supply:** 1.21V (TYP).
V_{PP}	Supply	**DRAM activating power supply:** 2.5V –0.125V / +0.250V.
V_{REFCA}	Supply	Reference voltage for control, command, and address pins.
V_{SS}	Supply	Ground.
V_{TT}	Supply	Power supply for termination of address, command, and control $V_{DD}/2$.
V_{DDSPD}	Supply	Power supply used to power the I^2C bus for SPD.
RFU	–	Reserved for future use.
NC	–	**No connect:** No internal electrical connection is present.

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Table 5: Pin Descriptions (Continued)

Symbol	Type	Description
NF	–	**No function:** May have internal connection present, but has no function.

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DQ Map

Table 6: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	1	7	U2	0	16	50
	1	3	21		1	18	62
	2	0	8		2	17	49
	3	2	20		3	19	63
	4	5	3		4	20	46
	5	7	17		5	22	58
	6	4	4		6	21	45
	7	6	16		7	23	59
U3	0	40	193	U4	0	56	235
	1	43	206		1	59	248
	2	41	192		2	57	234
	3	42	205		3	58	247
	4	44	189		4	61	231
	5	47	202		5	63	244
	6	45	188		6	60	230
	7	46	201		7	62	243
U5	0	52	209	U6	0	36	168
	1	55	223		1	39	180
	2	53	210		2	37	167
	3	54	222		3	38	181
	4	48	214		4	32	172
	5	51	227		5	35	184
	6	49	213		6	33	171
	7	50	226		7	34	185
U8	0	28	66	U9	0	12	24
	1	31	80		1	15	37
	2	29	67		2	13	25
	3	30	79		3	14	38
	4	24	70		4	8	28
	5	27	84		5	11	42
	6	25	71		6	9	29
	7	26	83		7	10	41

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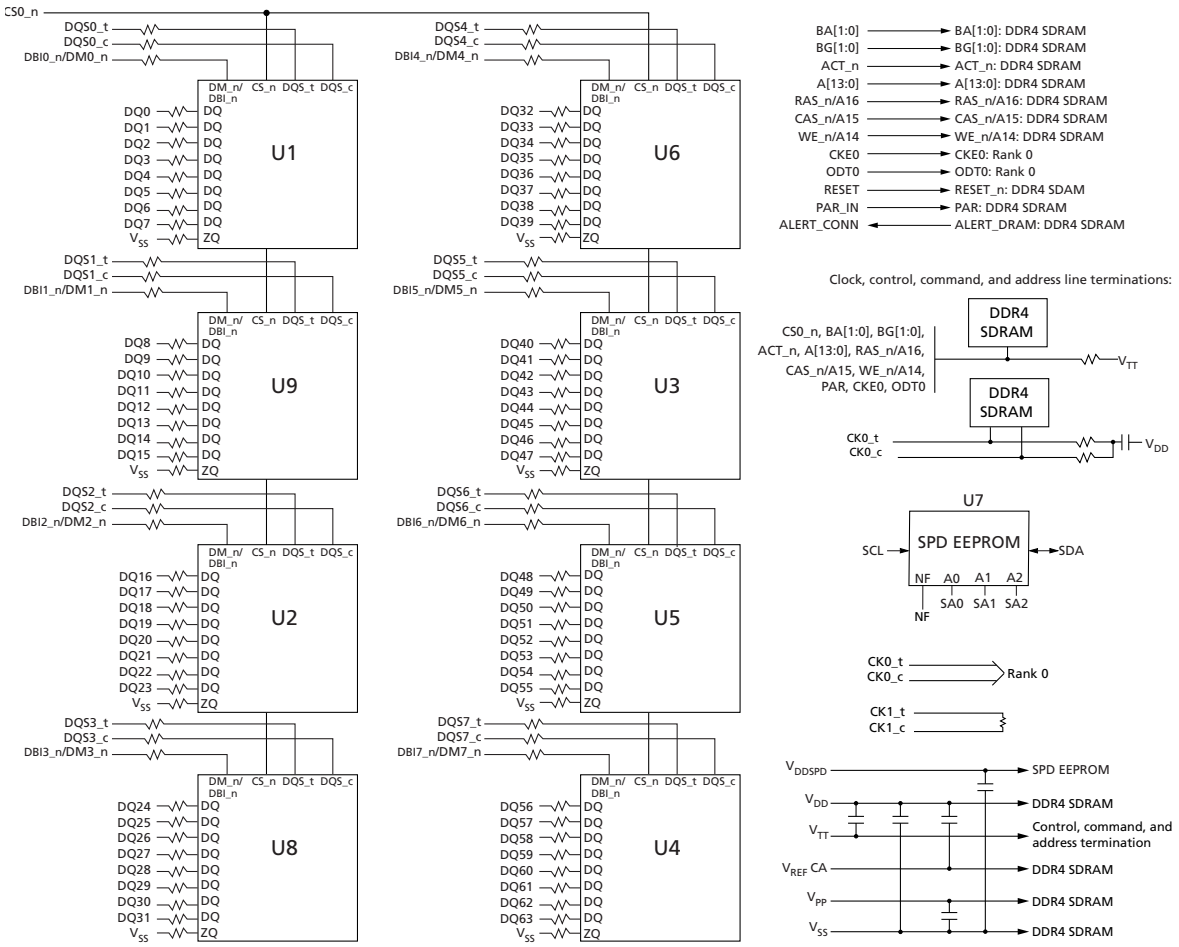
Functional Block Diagram

Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

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General Description

High-speed DDR4 SDRAM modules use DDR4 SDRAM devices with two or four internal memory bank groups. DDR4 SDRAM modules utilizing 4- and 8-bit-wide DDR4 SDRAM devices have four internal bank groups consisting of four memory banks each, providing a total of 16 banks. 16-bit-wide DDR4 SDRAM devices have two internal bank groups consisting of four memory banks each, providing a total of eight banks. DDR4 SDRAM modules benefit from DDR4 SDRAM's use of an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single READ or WRITE operation for the DDR4 SDRAM effectively consists of a single 8*n*-bit-wide, four-clock data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR4 modules use two sets of differential signals: DQS_t and DQS_c to capture data and CK_t and CK_c to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

Fly-By Topology

DDR4 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR4.

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SPD EEPROM Operation

DDR4 SDRAM modules incorporate serial presence detect (SPD). The SPD data is stored in a 512-byte JEDEC JC-42.4-compliant EEPROM that is segregated into four 128-byte, write-protectable blocks. The SPD content is aligned with these blocks as shown in the table below.

Block	Range		Description
0	0–127	000h–07Fh	Configuration and DRAM parameters
1	128–255	080h–0FFh	Module-specific parameters
2	256–319	100h–13Fh	Reserved; all bytes coded as 00h
	320–383	140h–17Fh	Manufacturing information
3	384–511	180h–1FFh	End-user programmable

The first 384 bytes are programmed by Micron to comply with JEDEC standard JC-45, "Appendix X: Serial Presence Detect (SPD) for DDR4 SDRAM Modules." The remaining 128 bytes of storage are available for use by the customer.

The EEPROM resides on a two-wire I^2C serial interface and is not integrated with the memory bus in any way. It operates as a slave device in the I^2C bus protocol, with all operations synchronized by the serial clock. Transfer rates of up to 1 MHz are achievable at 2.2–3.6V.

Micron implements reversible software write protection on DDR4 SDRAM-based modules. This prevents the lower 384 bytes (bytes 0–383) from being inadvertently programmed or corrupted. The upper 128 bytes remain available for customer use and unprotected.

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Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 7: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	V_{DD} supply voltage relative to V_{SS}	–0.4	1.5	V	1
V_{DDQ}	V_{DDQ} supply voltage relative to V_{SS}	–0.4	1.5	V	1
V_{PP}	Voltage on V_{PP} pin relative to V_{SS}	–0.4	3.0	V	2
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.4	1.5	V	

Table 8: Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units	Notes
V_{DD}	V_{DD} supply voltage	1.14	1.2	1.26	V	1
V_{PP}	DRAM activating power supply	2.375	2.5	2.75	V	2
$V_{REFCA(DC)}$	Input reference voltage command/ address bus	0.49 × V_{DD}	0.5 × V_{DD}	0.51 × V_{DD}	V	3
I_{VTT}	Termination reference current from V_{TT}	–750	–	750	mA	
V_{TT}	Termination reference voltage (DC) – command/address bus	0.49 × V_{DD} - 20mV	0.5 × V_{DD}	0.51 × V_{DD} + 20mV	V	4
I_I	Input leakage current; any input excluding ZQ; 0V < V_{IN} < 1.1V	–2.0	–	2.0	µA	5
$I_{I/O}$	DQ leakage; 0V < V_{in} < V_{DD}	–4.0	–	4.0	µA	5
I_I	Input leakage current; ZQ	–3.0	–	3.0	µA	5, 6
I_{OZpd}	Output leakage current; V_{OUT} = V_{DD}; DQ is disabled	–	–	5.0	µA	
I_{OZpu}	Output leakage current; V_{OUT} =V_{SS}; DQ and ODT are disabled; ODT is disabled with ODT input HIGH	–	–	5.0	µA	
I_{VREFCA}	V_{REFCA} leakage; V_{REFCA} = V_{DD}/2 (after DRAM is initialized)	–2.0	–	2.0	µA	5

Notes:
1. V_{DDQ} tracks with V_{DD}; V_{DDQ} and V_{DD} are tied together.
2. V_{PP} must be greater than or equal to V_{DD} at all times.
3. V_{REFCA} must not be greater than 0.6 x V_{DD}. When V_{DD} is less than 500mV, V_{REF} may be less than or equal to 300mV.
4. V_{TT} termination voltages in excess of the specification limit adversely affect the voltage margins of command and address signals and reduce timing margins.
5. Multiply by the number of DRAM die on the module.
6. Tied to ground. Not connected to edge connector.

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Table 9: Thermal Characteristics

Symbol	Parameter/Condition	Value	Units	Notes
T_C	Commercial operating case temperature	0 to 85	°C	1, 2, 3
T_C		>85 to 95	°C	1, 2, 3, 4
T_{OPER}	Normal operating temperature range	0 to 85	°C	5, 6
T_{OPER}	Extended temperature operating range (optional)	>85 to 95	°C	5, 6

Notes:
1. Maximum operating case temperature; T_C is measured in the center of the package.
2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum T_C during operation.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum T_C during operation.
4. If T_C exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 3.9µs interval refresh rate.
5. The refresh rate must double when 85°C < T_{OPER} ≤ 95°C.
6. For additional information, refer to technical note TN-00-08: "Thermal Applications" available on micron.com.

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DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR4 component data sheets. Component specifications are available on micron.com. Module speed grades correlate with component speed grades, as shown below.

Table 10: Module and Component Speed Grades

DDR4 components may exceed the listed module speed grades; module may not be available in all listed speed grades

Module Speed Grade	Component Speed Grade
-2G4	-083E
-2G1	-093E
-1G9	-107E

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the edge connector of the module, not at the DRAM. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

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I_{DD} Specifications

Table 11: DDR4 I_{DD} Specifications and Conditions – 4GB (Die Revision A)

Values are for the MT40A512M8 DDR4 SDRAM only and are computed from values specified in the 4Gb (512 Meg x 8) component data sheet

Parameter	Symbol	2400	2133	1866	Units
One bank ACTIVATE-PRECHARGE current	I_{DD0}	512	480	464	mA
One bank ACTIVATE-PRECHARGE, Word Line Boost, I_{PP} current	I_{PP0}	32	32	32	mA
One bank ACTIVATE-READ-PRECHARGE current	I_{DD1}	544	520	504	mA
Precharge standby current	I_{DD2N}	400	368	352	mA
Precharge standby ODT current	I_{DD2NT}	464	432	400	mA
Precharge power-down current	I_{DD2P}	256	240	240	mA
Precharge quiet standby current	I_{DD2Q}	328	312	312	mA
Active standby current	I_{DD3N}	536	504	488	mA
Active standby I_{PP} current	I_{PP3N}	24	24	24	mA
Active power-down current	I_{DD3P}	352	352	352	mA
Burst read current	I_{DD4R}	1280	1200	1120	mA
Burst read I_{DDQ} current	I_{DDQ4R}	320	288	256	mA
Burst write current	I_{DD4W}	1440	1280	1152	mA
Burst refresh current (1x REF)	I_{DD5B}	1536	1520	1520	mA
Burst refresh I_{PP} current (1x REF)	I_{PP5B}	176	176	176	mA
Self refresh current: Normal temperature range (0°C to 85°C)	I_{DD6N}	160	160	160	mA
Self refresh current: Extended temperature range (0°C to 95°C)	I_{DD6E}	216	216	216	mA
Self refresh current: Reduced temperature range (0°C to 45°C)	I_{DD6R}	80	80	80	mA
Auto self refresh current (25°C)	I_{DD6A}	72	72	72	mA
Auto self refresh current (45°C)	I_{DD6A}	80	80	80	mA
Auto self refresh current (75°C)	I_{DD6A}	128	128	128	mA
Bank interleave read current	I_{DD7}	1680	1480	1280	mA
Bank interleave read I_{PP} current	I_{PP7}	112	96	80	mA
Maximum power-down current	I_{DD8}	144	144	144	mA

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SPD EEPROM Operating Conditions

For the latest SPD data, refer to Micron's SPD page: micron.com/spd.

Table 12: SPD EEPROM DC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	2.2	3.6	V
Input low voltage: logic 0; all inputs	V_{IL}	–0.5	V_{DDSPD} × 0.3	V
Input high voltage: logic 1; all inputs	V_{IH}	V_{DDSPD} × 0.7	V_{DDSPD} + 0.5	V
Output low voltage: 3mA sink current V_{DDSPD} > 2V	V_{OL}	–	0.4	V
Input leakage current: (SCL, SDA) V_{IN} = V_{DDSPD} or V_{SSSPD}	I_{LI}	–	±5	µA
Output leakage current: V_{OUT} = V_{DDSPD} or V_{SSSPD}, SDA in High-Z	I_{LO}	–	±5	µA

Notes:
1. Table is provided as a general reference. Consult JEDEC JC-42.4 EE1004 and TSE2004 device specifications for complete details.
2. All voltages referenced to V_{DDSPD}.

Table 13: SPD EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Clock frequency	^{t}SCL	10	1000	kHz
Clock pulse width HIGH time	^{t}HIGH	260	–	ns
Clock pulse width LOW time	^{t}LOW	500	–	ns
Detect clock LOW timeout	^{t}TIMEOUT	25	35	ms
SDA rise time	^{t}R	–	120	ns
SDA fall time	^{t}F	–	120	ns
Data-in setup time	^{t}SU:DAT	50	–	ns
Data-in hold time	^{t}HD:DI	0	–	ns
Data out hold time	^{t}HD:DAT	0	350	ns
Start condition setup time	^{t}SU:STA	260	–	ns
Start condition hold time	^{t}HD:STA	260	–	ns
Stop condition setup time	^{t}SU:STO	260	–	ns
Time the bus must be free before a new transition can start	^{t}BUF	500	–	ns
Write time	^{t}W	–	5	ms
Warm power cycle time off	^{t}POFF	1	–	ms
Time from power on to first command	^{t}INIT	10	–	ms

Note:
1. Table is provided as a general reference. Consult JEDEC JC-42.4 EE1004 and TSE2004 device specifications for complete details.

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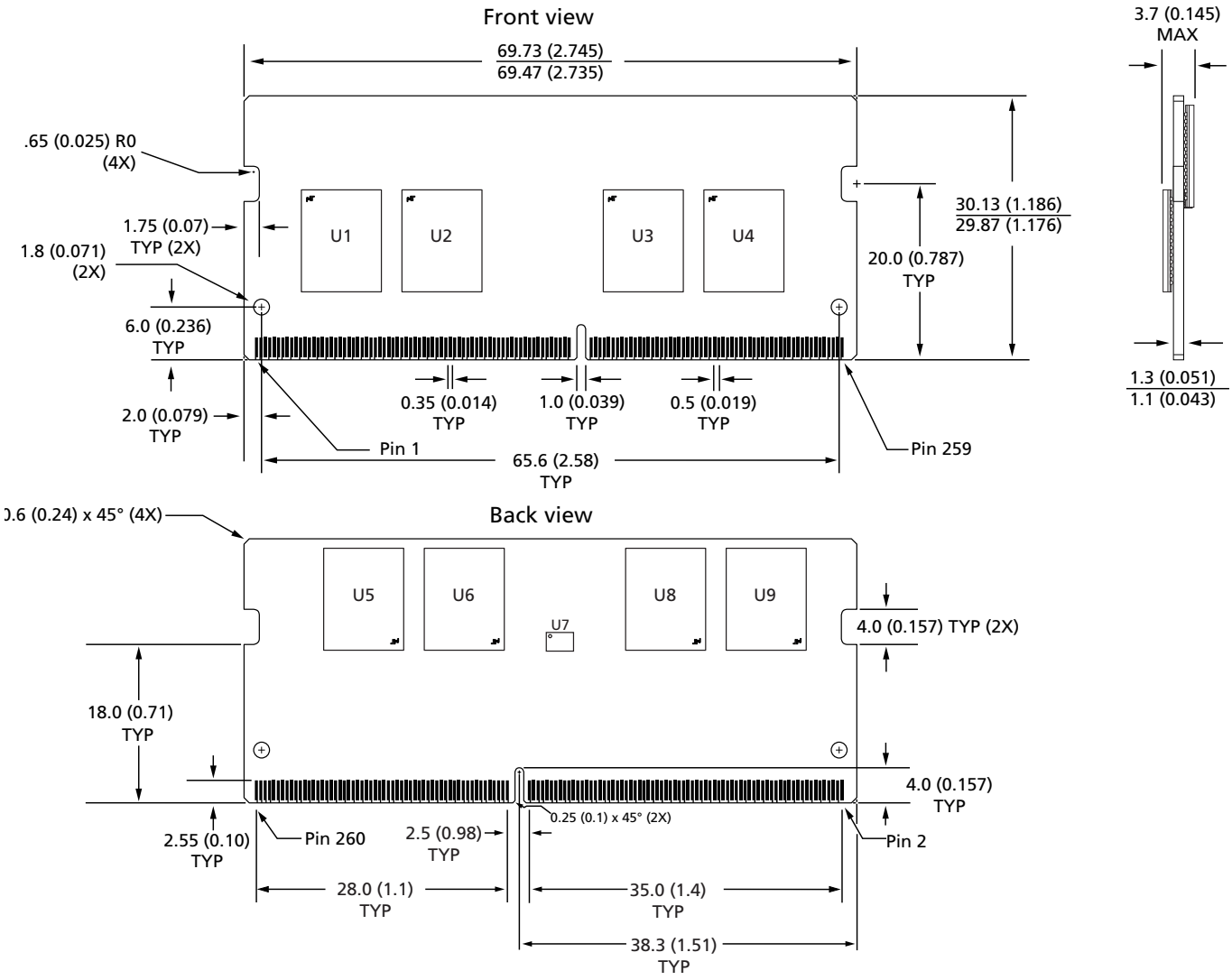
Module Dimensions

Figure 3: 260-Pin DDR4 SODIMM



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.

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