

N-channel TrenchMOS logic level FET Rev. 03 — 31 May 2010

Product data sheet

Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Q101 compliant

- Suitable for logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V and 24 V loads
- Automotive systems

- General purpose power switching
- Motors, lamps and solenoids

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	-	55	V
I _D	drain current	$V_{GS} = 5 \text{ V}; T_{mb} = 25 \text{ °C};$ see <u>Figure 1</u> ; see <u>Figure 3</u>	<u>[1]</u>	-	-	75	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>		-	-	203	W
Static char	acteristics						
0	drain-source on-state	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A};$ $T_j = 25 \text{ °C}$		-	6.2	7	mΩ
	resistance	$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A};$ $T_j = 25 \text{ °C};$ see Figure 11; see Figure 12		-	7.1	8.4	mΩ



Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Avalanche	ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I_D = 75 A; $V_{sup} \le 55$ V; R_{GS} = 50 Ω ; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped	-	-	352	mJ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 5 \text{ V; } I_D = 25 \text{ A;}$ $V_{DS} = 44 \text{ V; } T_j = 25 \text{ °C;}$ see Figure 13	-	16	-	nC

^[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain	mb	D
3	S	source		G (EX)
mb	D			mbb076 S
			1 2 3	
			SOT226 (I2PAK)	

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9E08-55B	I2PAK	plastic single-ended package (I2PAK); TO-262	SOT226

4. Limiting values

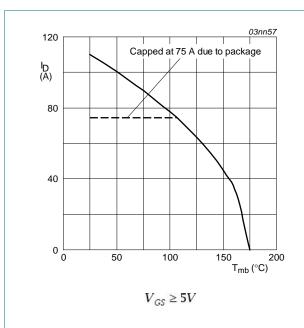
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	-	55	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$		-	-	55	V
V _{GS}	gate-source voltage			-15	-	15	V
I _D	drain current	$T_{mb} = 100 ^{\circ}C; V_{GS} = 5 V; see \underline{Figure 1}$	<u>[1]</u>	-	-	75	Α
		$T_{mb} = 25 ^{\circ}\text{C}; V_{GS} = 5 \text{V}; \text{see} \frac{\text{Figure 1}}{\text{Figure 1}};$	[2]	-	-	110	Α
		see Figure 3	[1]	-	-	75	Α
I _{DM}	peak drain current	T_{mb} = 25 °C; $t_p \le 10 \mu s$; pulsed; see Figure 3		-	-	439	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>		-	-	203	W
T _{stg}	storage temperature			-55	-	175	°C
Tj	junction temperature			-55	-	175	°C
Source-drain	diode						
Is	source current	T _{mb} = 25 °C	[2]	-	-	110	Α
			<u>[1]</u>	-	-	75	Α
I _{SM}	peak source current	$t_p \le 10 \ \mu s$; pulsed; $T_{mb} = 25 \ ^{\circ}C$		-	-	439	Α
Avalanche rug	ggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I_D = 75 A; V_{sup} ≤ 55 V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped		-	-	352	mJ

^[1] Continuous current is limited by package.

^[2] Current is limited by power dissipation chip rating.



120

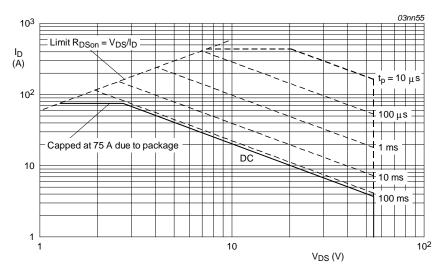
Pder (%)

80

40 $0 = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$

Fig 1. Continuous drain current as a function of mounting base temperature

Fig 2. Normalized total power dissipation as a function of mounting base temperature



 $T_{mb} = 25$ °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	see Figure 4	-	-	0.74	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	vertical in still air	-	60	-	K/W

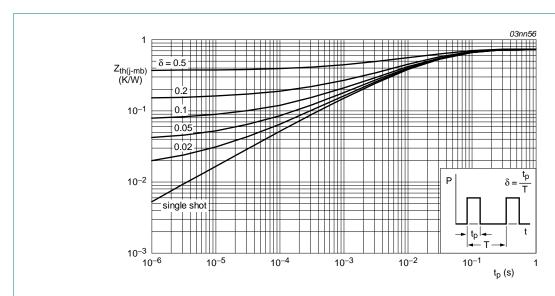


Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Table 6.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	aracteristics					
$V_{(BR)DSS}$	drain-source	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	55	-	-	V
	breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ °C}$	50	-	-	V
V _{GS(th)}	gate-source threshold voltage	$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_j = 25$ °C; see <u>Figure 10</u>	1.1	1.5	2	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_j = -55$ °C; see <u>Figure 10</u>	-	-	2.3	V
		$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 175 \text{ °C}$; see <u>Figure 10</u>	0.5	-	-	V
I _{DSS}	drain leakage current	$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ °C}$	-	-	500	μΑ
		$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.02	1	μΑ
I _{GSS}	gate leakage current	$V_{DS} = 0 \text{ V}; V_{GS} = 15 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nA
		$V_{DS} = 0 \text{ V}; V_{GS} = -15 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nA
R _{DSon}	drain-source on-state	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C}$	-	-	9.3	mΩ
	resistance	$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 175 °C;$ see <u>Figure 11</u> ; see <u>Figure 12</u>	-	-	16.8	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C}$	-	6.2	7	mΩ
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 ^{\circ}\text{C};$ see <u>Figure 11</u> ; see <u>Figure 12</u>	-	7.1	8.4	mΩ
Dynamic	characteristics					
Q _{G(tot)}	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 44 \text{ V}; V_{GS} = 5 \text{ V};$	-	45	-	nC
Q_{GS}	gate-source charge	T _j = 25 °C; see <u>Figure 13</u>	-	9	-	nC
Q_{GD}	gate-drain charge		-	16	-	nC
C _{iss}	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$	-	3960	5280	pF
C _{oss}	output capacitance	T _j = 25 °C; see <u>Figure 14</u>	-	517	620	pF
C _{rss}	reverse transfer capacitance		-	206	282	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \Omega; V_{GS} = 5 \text{ V};$	-	29	-	ns
t _r	rise time	$R_{G(ext)} = 10 \Omega; T_j = 25 °C$	-	123	-	ns
t _{d(off)}	turn-off delay time		-	131	-	ns
t _f	fall time		-	86	-	ns
L _D	internal drain inductance	from drain lead 6 mm from package to center of die; $T_j = 25$ °C	-	4.5	-	nΗ
		from upper edge of drain mounting base to center of die ; $T_j = 25$ °C	-	2.5	-	nΗ
L _S	internal source inductance	from source lead to source bond pad ; $T_j = 25 ^{\circ}\text{C}$	-	7.5	-	nΗ

Table 6. Characteristics ... continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C};$ see <u>Figure 15</u>	-	0.85	1.2	V
t _{rr}	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s};$	-	69	-	ns
Q _r	recovered charge	$V_{GS} = -10 \text{ V}; V_{DS} = 30 \text{ V}; T_j = 25 \text{ °C}$	-	72	-	nC

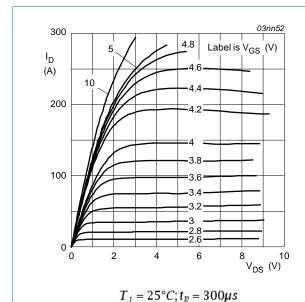


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

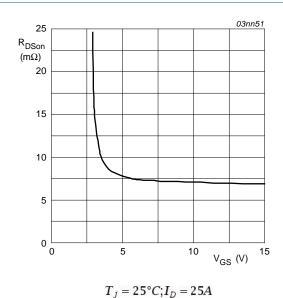


Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

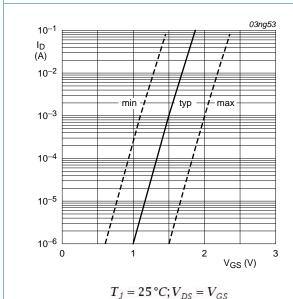
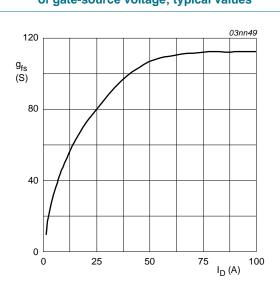


Fig 7. Sub-threshold drain current as a function of gate-source voltage



 $T_j = 25^{\circ}C; V_{DS} = 25V$

Fig 8. Forward transconductance as a function of drain current; typical values

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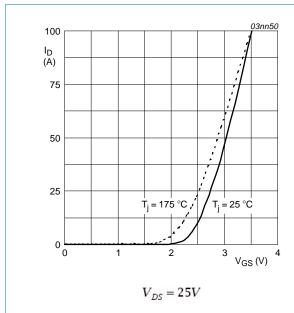


Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

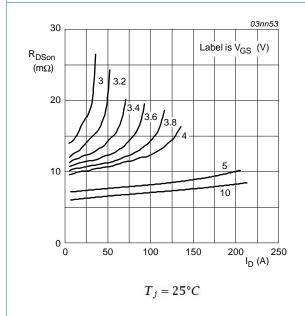
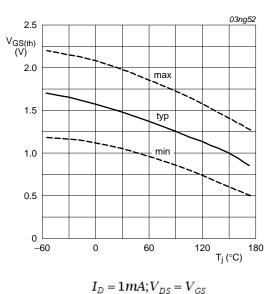


Fig 11. Drain-source on-state resistance as a function of drain current; typical values



2 , 23

Fig 10. Gate-source threshold voltage as a function of junction temperature

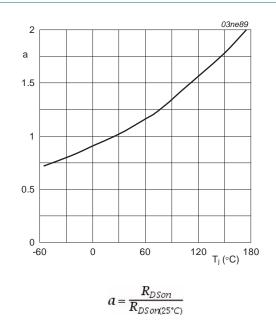


Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

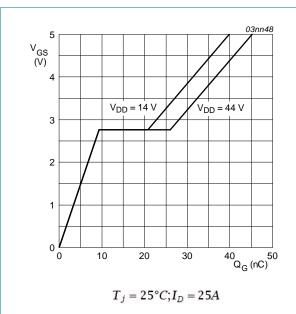
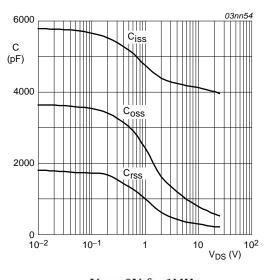
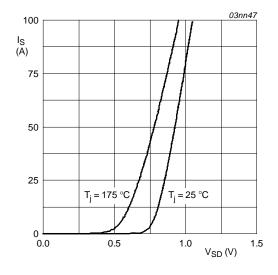


Fig 13. Gate-source voltage as a function of gate charge; typical values



 $V_{GS} = 0V; f = 1MHz$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



 $V_{GS} = 0V$

Fig 15. Source current as a function of source-drain voltage; typical values

7. Package outline

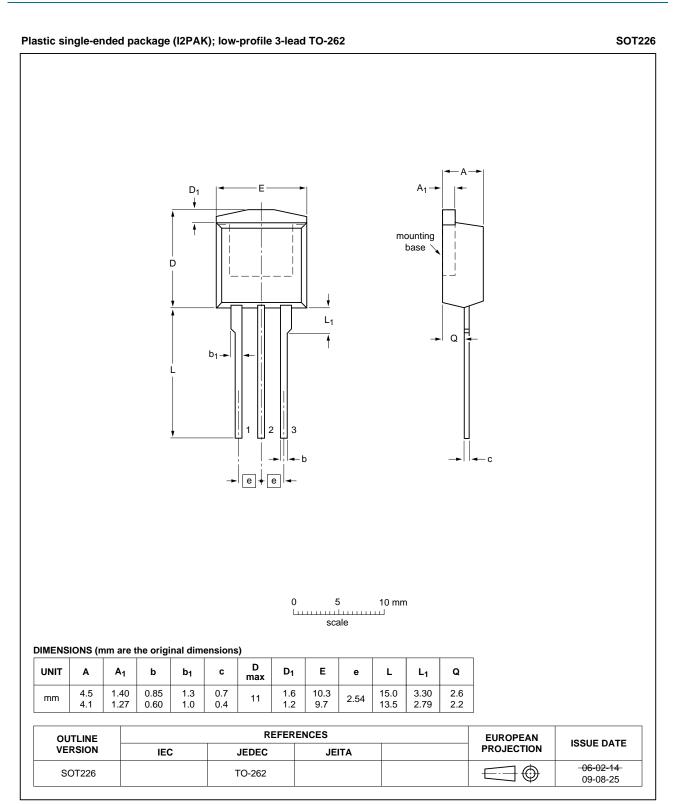


Fig 16. Package outline SOT226 (I2PAK)

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8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
BUK9E08-55B v.3	20100531	Product data sheet	-	BUK95_96_9E08_55B-02	
Modifications:	 The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. 				
	 Type number 	er BUK9E08-55B separated	d from data sheet BUK9	5_96_9E08_55B-02.	
BUK95_96_9E08_55B-02 (9397 750 12052)	20031013	Product data sheet	-	-	

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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