NB7LQ572

2.5V / 3.3V Differential 4:1 Mux w/Input Equalizer to 1:2 LVPECL Clock/Data Fanout / Translator

Multi−Level Inputs w/ Internal Termination

The NB7LQ572 is a high performance differential 4:1 Clock/Data input multiplexer and a 1:2 LVPECL Clock / Data fanout buffer that operates up to 7 GHz / 11 Gbps respectively with a 2.5 V or 3.3 V power supply.

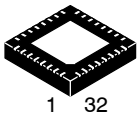
Each INx/$\overline{\text{INx}}$ input pair incorporates a fixed Equalizer Receiver, which when placed in series with a Data path, will enhance the degraded signal transmitted across an FR4 backplane or cable interconnect. For applications that do not require Equalization, consider the NB7L572, which is pin−compatible to the NB7LQ572.

The differential Clock / Data inputs have internal 50 Ω termination resistors and will accept differential LVPECL, CML, or LVDS logic levels. The NB7LQ572 incorporates a pair of Select pins that will choose one of four differential inputs and will produce two identical LVPECL output copies of Clock or Data. As such, the NB7LQ572 is ideal for SONET, GigE, Fiber Channel, Backplane and other Clock/Data distribution applications.

The two differential LVPECL outputs will swing 750 mV when externally loaded and terminated with a 50 Ω resistor to V_{CC} − 2 V and are optimized for low skew and minimal jitter.

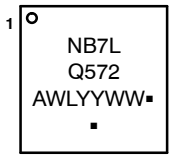
The NB7LQ572 is offered in a low profile 5x5 mm 32−pin QFN Pb−Free package. Application notes, models, and support documentation are available at www.onsemi.com.

The NB7LQ572 is a member of the GigaComm™ family of high performance clock products.



QFN32
MN SUFFIX
CASE 488AM

MARKING DIAGRAM



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

Features

- Input Data Rate > 11 Gb/s Typical
- Data Dependent Jitter < 10 ps
- Maximum Input Clock Frequency > 7 GHz Typical
- Random Clock Jitter < 0.8 ps RMS
- Fixed Input Equalization
- Low Skew 1:2 LVPECL Outputs, < 15 ps max
- 4:1 Multi−Level Mux Inputs, accepts LVPECL, CML LVDS
- 160 ps Typical Propagation Delay
- 50 ps Typical Rise and Fall Times
- Differential LVPECL Outputs, 800 mV peak−to−peak, typical
- Operating Range: 2.5 ±5% or 3.3 V ±10%
- Internal 50 Ω Input Termination Resistors
- V_{REFAC} Reference Output
- QFN−32 Package, 5mm x 5mm
- −40°C to +85°C Ambient Operating Temperature
- These are Pb−Free Devices

April, 2010 − Rev. 0
Publication Order Number:
NB7LQ572/D

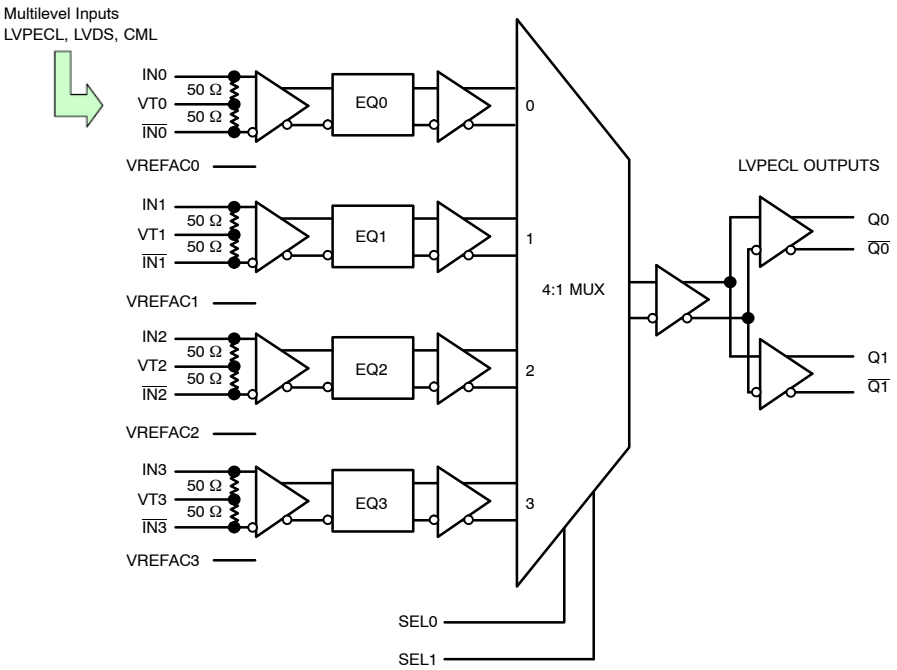


Figure 1. Simplified Block Diagram

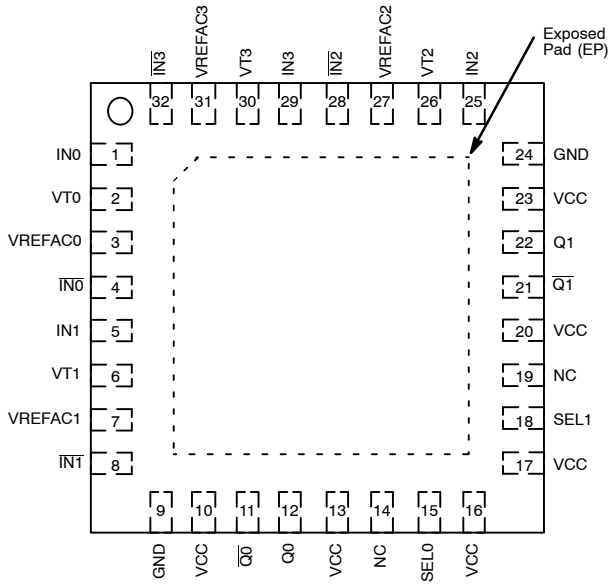


Figure 2. Pinout: QFN−32 (Top View)

Table 1. Input Select Function Table

SEL1*	SEL0*	Clock / Data Input Selected
0	0	IN0 Input Selected
0	1	IN1 Input Selected
1	0	IN2 Input Selected
1	1	IN3 Input Selected

*Defaults HIGH when left open.

Table 2. PIN DESCRIPTION

Pin Number	Pin Name	I/O	Pin Description
1, 4 5, 8 25, 28 29, 32	IN0, $\overline{IN0}$ IN1, $\overline{IN1}$ IN2, $\overline{IN2}$ IN3, $\overline{IN3}$	LVPECL, CML, LVDS Input	Noninverted, Inverted, Differential Clock or Data Inputs
2, 6 26, 30	VT0, VT1 VT2, VT3		Internal 100 Ω Center−tapped Termination Pin for INx / $\overline{INx}$
15 18	SEL0 SEL1	LVTTL/LVCMOS Input	Input Select pins, default HIGH when left open through a 94 kΩ pullup resistor. Input logic threshold is V_{CC} / 2. See Select Function, Table 1.
14, 19	NC	−	No Connect
10, 13, 16 17, 20, 23	V_{CC}	−	Positive Supply Voltage.
11, 12 21, 22	$\overline{Q0}$, Q0 $\overline{Q1}$, Q1	LVPECL Output	Non−inverted, Inverted Differential Outputs.
9, 24	GND		Negative Supply Voltage
3 7 27 31	VREFAC0 VREFAC1 VREFAC2 VREFAC3	−	Output Voltage Reference for Capacitor−Coupled Inputs
−	EP	−	The Exposed Pad (EP) on the QFN−32 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat−sinking conduit. The pad is electrically connected to the die, and must be electrically connected to GND.

1. In the differential configuration when the input termination pins (VT0, VT1, VT2, VT3) are connected to a common termination voltage or left open, and if no signal is applied on INx/$\overline{INx}$ input, then the device will be susceptible to self−oscillation.
2. All V_{CC} and GND pins must be externally connected to a power supply for proper operation.

Table 3. ATTRIBUTES

Characteristics		Value
ESD Protection	Human Body Model Machine Model	> 2 kV > 200 V
R_{PU} – SELx Input Pullup Resistor		56 kΩ
Moisture Sensitivity (Note 3)	QFN−32	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		268
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

3. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	GND = 0 V		−0.5 to +4.0	V
V_{IN}	Positive Input Voltage	GND = 0 V		−0.5 to V_{CC} +0.5	V
V_{INPP}	Differential Input Voltage |IN − $\overline{IN}$|			1.89	V
I_{OUT}	LVPECL Output Current	Continuous Surge		50 100	mA
I_{IN}	Input current Through RT (50 Ω resistor)			±40	mA
I_{VREFAC}	V_{REFAC} Sink or Source Current			±1.5	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 4)	0 lfpm 500 lfpm	QFN−32 QFN−32	31 27	°C/W
θ_{JC}	Thermal Resistance (Junction−to−Case) (Note 4)		QFN−32	12	°C/W
T_{sol}	Wave Solder	≤ 20 sec		265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. JEDEC standard multilayer board − 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 5. DC CHARACTERISTICS POSITIVE LVPECL OUTPUT V_{CC} = 2.375 V to 2.625 V, 3.0 V to 3.6 V, GND = 0 V, T_A = −40°C to +85°C (Note 5)

Symbol	Characteristic	Min	Typ	Max	Unit
POWER SUPPLY					
V_{CC}	Power Supply Voltage V_{CC} = 2.5 V V_{CC} = 3.3 V	2.375 3.0	2.5 3.3	2.625 3.6	V
I_{CC}	Power Supply Current for V_{CC} (Inputs and Outputs Open)		100	125	mA
LVPECL OUTPUTS					
V_{OH}	Output HIGH Voltage (Note 6) V_{CC} = 2.5 V V_{CC} = 3.3 V	V_{CC} − 1145 1355 2155	V_{CC} − 900 1600 2400	V_{CC} − 800 1700 2500	mV
V_{OL}	Output LOW Voltage (Note 6) V_{CC} = 2.5 V V_{CC} = 3.3 V	V_{CC} − 2000 500 1300	V_{CC} − 1700 800 1600	V_{CC} − 1500 1000 1800	mV
DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE−ENDED (Note 7) (Figures 9 and 10)					
V_{IH}	Single−ended Input HIGH Voltage	V_{th} + 100		V_{CC}	mV
V_{IL}	Single−ended Input LOW Voltage	GND		V_{th} − 100	mV
V_{th}	Input Threshold Reference Voltage Range (Note 8)	1100		V_{CC} − 100	mV
V_{ISE}	Single−ended Input Voltage (V_{IH} − V_{IL})	200		V_{CC}	mV
VREFAC					
V_{REFAC}	Output Reference Voltage (100 μA Load)	V_{CC} − 1300	V_{CC} − 1100	V_{CC} − 900	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Note 9) (Figures 11 and 12)					
V_{IHD}	Differential Input HIGH Voltage (IN_x, $\overline{IN}_x$)	1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage (IN_x, $\overline{IN}_x$)	0		V_{IHD} − 100	mV
V_{ID}	Differential Input Voltage (IN_x, $\overline{IN}_x$) (V_{IHD} − V_{ILD})	100		1200	mV
V_{CMR}	Input Common Mode Range (Differential Configuration) (Note 10) (Figure 13)	1150		V_{CC} − 50	mV
I_{IH}	Input HIGH Current $IN_x/\overline{IN}_x$ ($VT_x/\overline{VT}_x$ Open)	−150		150	μA
I_{IL}	Input LOW Current $IN_x/\overline{IN}_x$ ($VT_x/\overline{VT}_x$ Open)	−150		150	μA
CONTROL INPUT (SELx Pin)					
V_{IH}	Input HIGH Voltage for Control Pin	2.0		V_{CC}	V
V_{IL}	Input LOW Voltage for Control Pin	GND		0.8	V
I_{IH}	Input HIGH Current	−150		150	μA
I_{IL}	Input LOW Current	−150		150	μA
TERMINATION RESISTORS					
R_{TIN}	Internal Input Termination Resistor (Measured from INx to VTx)	45	50	55	Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Input and Output parameters vary 1:1 with V_{CC}.
6. LVPECL outputs loaded with 50 Ω to V_{CC} − 2 V for proper operation.
7. Vth, V_{IH}, $V_{IL,}$, and V_{ISE} parameters must be complied with simultaneously.
8. Vth is applied to the complementary input when operating in single−ended mode.
9. V_{IHD}, V_{ILD}, V_{ID} and V_{CMR} parameters must be complied with simultaneously.
10. V_{CMR} min varies 1:1 with GND, V_{CMR} max varies 1:1 with V_{CC}. The V_{CMR} range is referenced to the most positive side of the differential input signal.

Table 6. AC CHARACTERISTICS V_{CC} = 2.375 V to 2.625 V, 3.0 V to 3.6 V, GND = 0 V, T_A = −40°C to +85°C (Note 11)

Symbol	Characteristic		Min	Typ	Max	Unit
f_{MAX}	Maximum Input Clock Frequency	$V_{OUT} \geq$ 400 mV	6	7		GHz
$f_{DATAMAX}$	Maximum Operating Data Rate	NRZ, (PRBS23)	10	11		Gbps
f_{SEL}	Maximum Toggle Frequency, SELx		4	10		MHz
V_{OUTPP}	Output Voltage Amplitude (@ $V_{INPPmin}$) $f_{in} \leq$ 6 GHz (Note 11) (Figures 3 and 14)		400	800		mV
t_{PLH}, t_{PHL}	Propagation Delay to Differential Outputs Measured at Differential Crosspoint	INx/$\overline{INx}$ to Qx/$\overline{Qx}$ @1 GHz @ 50 MHz SELn to Qx	75	160 5	250 10	ps ns
$t_{PD\ Tempco}$	Differential Propagation Delay Temperature Coefficient			100		Δfs/°C
tskew	Output – Output skew (within device) (Note 13) Device – Device skew ($t_{pdmax} - t_{pdmin}$)			0 30	15 100	ps
t_{DC}	Output Clock Duty Cycle (Reference Duty Cycle = 50%)	f_{in} = 1 GHz	45	50	55	%
Φ_N	Phase Noise, f_C = 1 GHz	10 kHz 100 kHz 1 MHz 10 MHz 20 MHz		−135 −136 −148 −148 −148		dBc
$t_{JIT(\Phi)}$	Phase Jitter (RMS) (Figure 7) f_C = 1 GHz, 12 kHz – 20 MHz			40		fs
t_{JITTER}	Random Clock Jitter, RJ(RMS), (Note 14) Deterministic Jitter, DJ (Note 15)	$f_{IN} \leq$ 7 GHz $f_{IN} \leq$ 10 Gbps		0.2	0.8 10	ps
	Crosstalk Induced Jitter (RMS) (Adjacent Channel) (Note 16)				0.7	ps
V_{INPP}	Input Voltage Swing (Differential Configuration) (Note 17)		100		1200	mV
t_r, t_f	Output Rise/Fall Times @ 1 GHz; (20% – 80%), Qx, $\overline{Qx}$		25	50	75	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

11. Measured using a $V_{INPPmin}$ source, 50% duty cycle clock source. All output loading with external 50 Ω to V_{CC} – 2 V. Input edge rates 40 ps (20% – 80%).
12. Output voltage swing is a single−ended measurement operating in differential mode.
13. Skew is measured between outputs under identical transitions and conditions. Duty cycle skew is defined only for differential operation when the delays are measured from cross−point of the inputs to the cross−point of the outputs.
14. Additive RMS jitter with 50% duty cycle clock signal.
15. Additive Peak−to−Peak data dependent jitter with input NRZ data at PRBS23.
16. Crosstalk is measured at the output while applying two similar clock frequencies that are asynchronous with respect to each other at the inputs.
17. Input voltage swing is a single−ended measurement operating in differential mode.

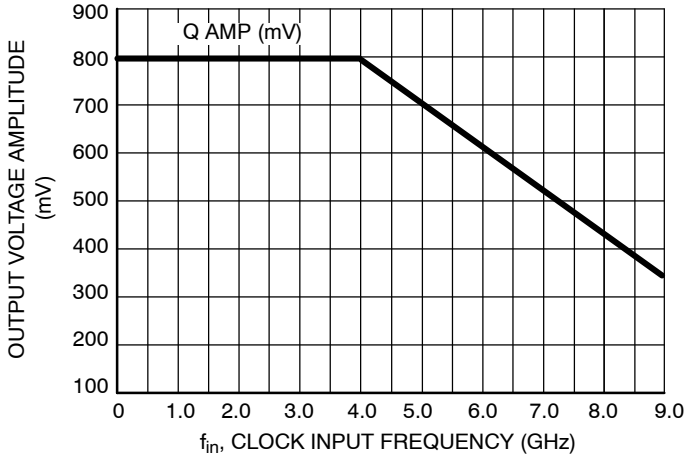


Figure 3. Clock Output Voltage Amplitude (V_{OUTPP}) vs. Input Frequency (f_{in}) at Ambient Temperature (Typical)

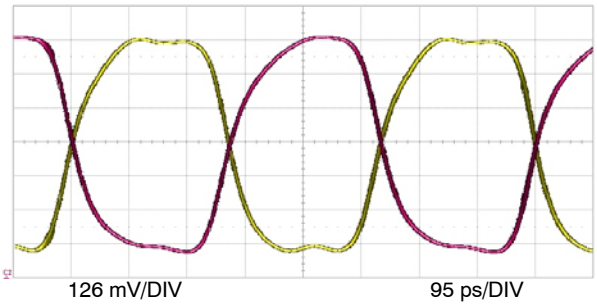


Figure 4. Typical Output Waveform at 2 GHz (V_{INPP} = 175 mV, V_{CC} = 2.38 V)

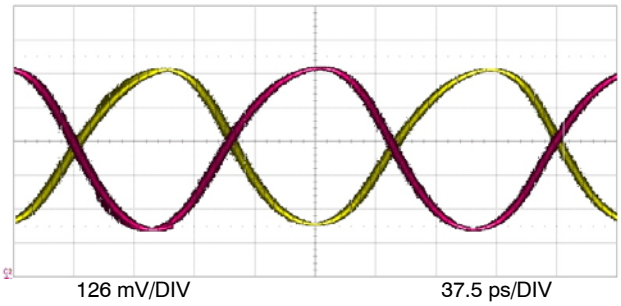


Figure 5. Typical Output Waveform at 5 GHz (V_{INPP}= 175 mV, V_{CC} = 2.38 V)

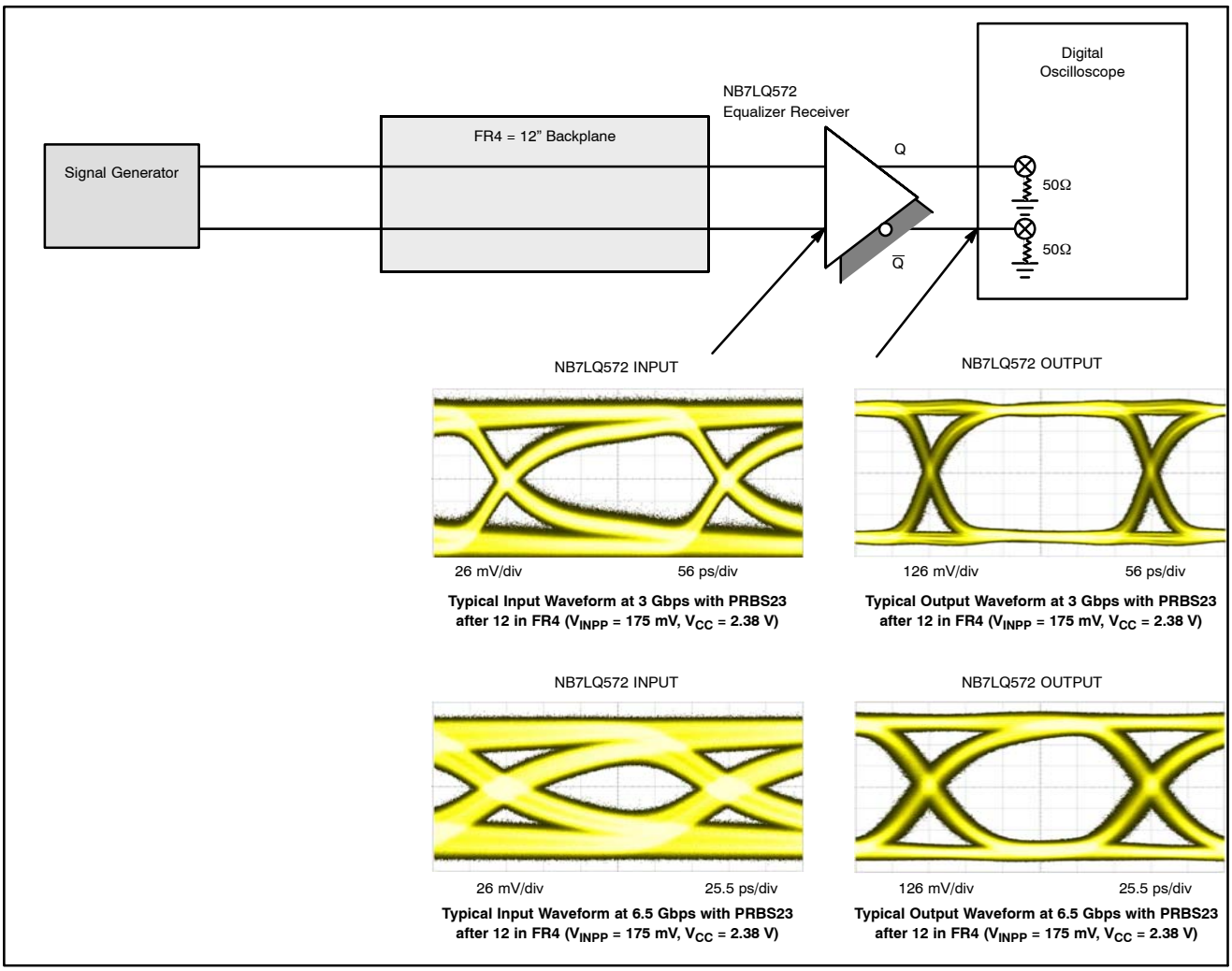


Figure 6. Typical NB7LQ572 Equalizer Application and Interconnect; Eye Diagrams with PRBS23 Pattern at 3 Gbps and 6.5 Gbps after 12 inches of FR4

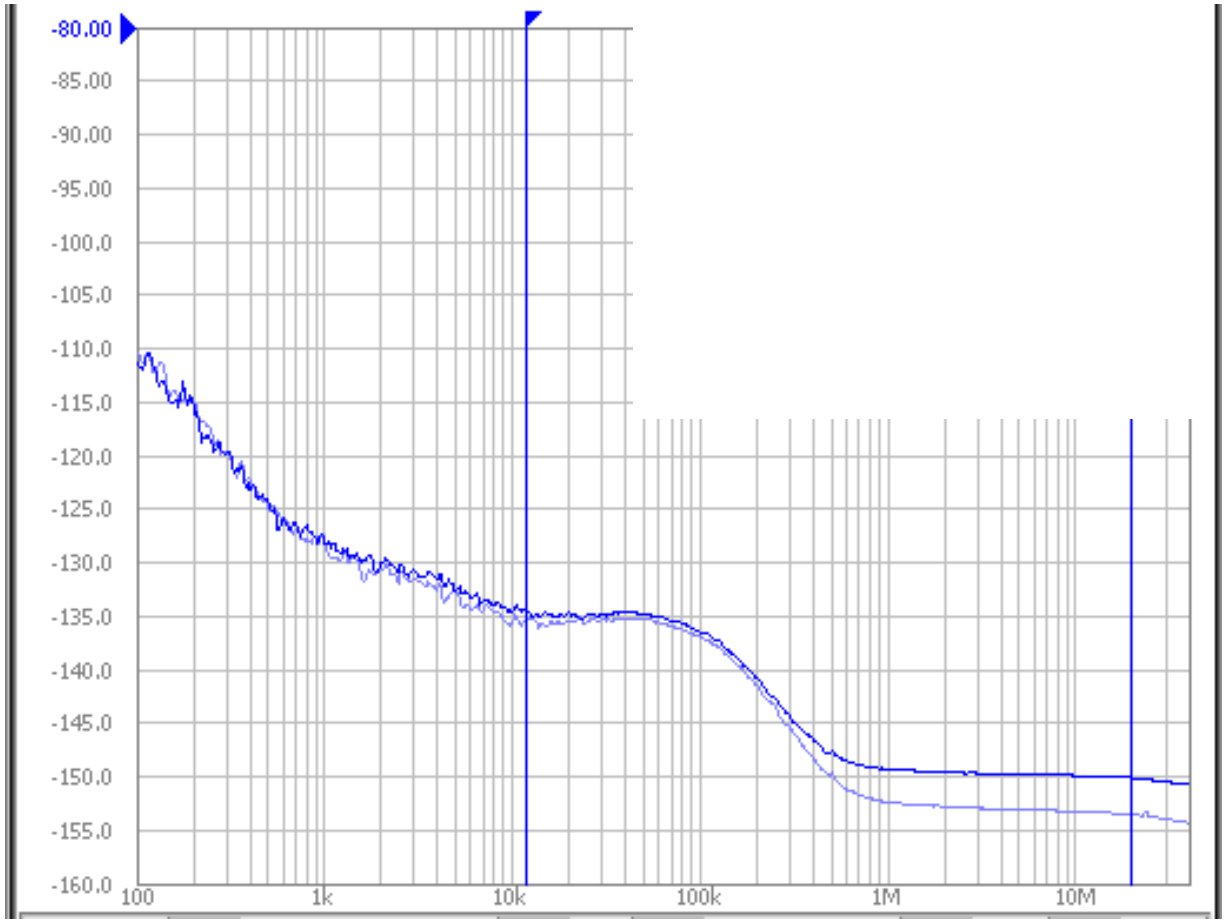


Figure 7. Typical Phase Noise Plot at $f_{carrier}$ = 1 GHz

The phase noise plot was captured using an Agilent E5052A which shows additive phase noise of the NB7LQ572 at 1 GHz, an operating voltage of 2.5 V at room temperature. The RMS Phase Jitter contributed by the device (integrated between 12 kHz and 20 MHz) is 35 fs. The input source used for the phase noise measurement is an Agilent E8663B.

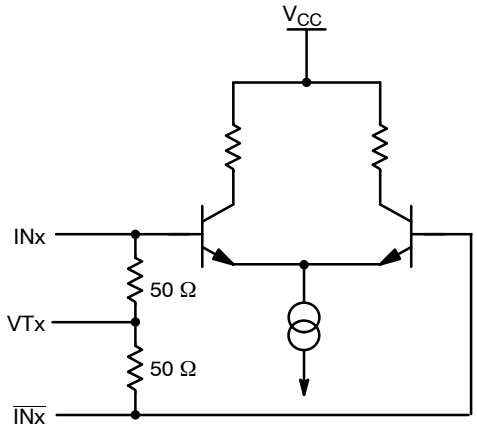


Figure 8. Input Structure

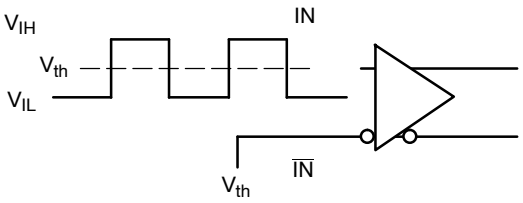


Figure 9. Differential Input Driven Single−Ended

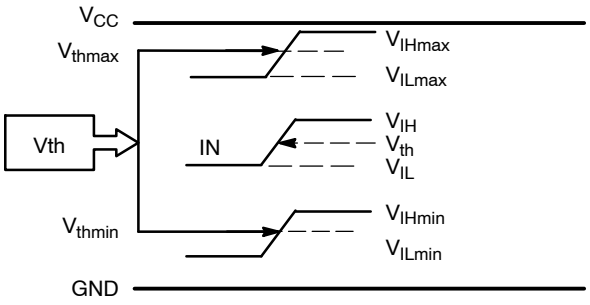


Figure 10. V_{th} Diagram

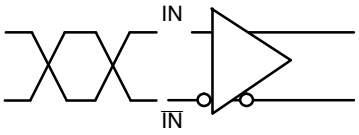


Figure 11. Differential Inputs Driven Differentially

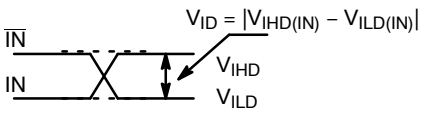


Figure 12. Differential Inputs Driven Differentially

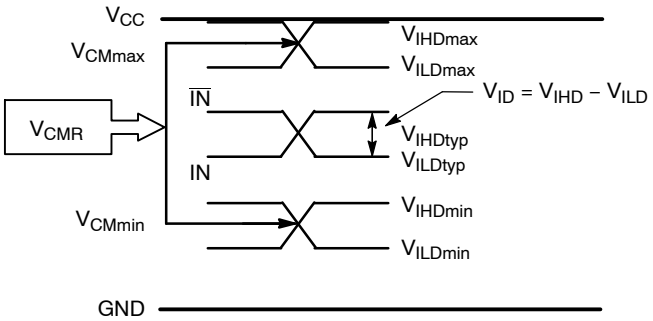


Figure 13. VCMR Diagram

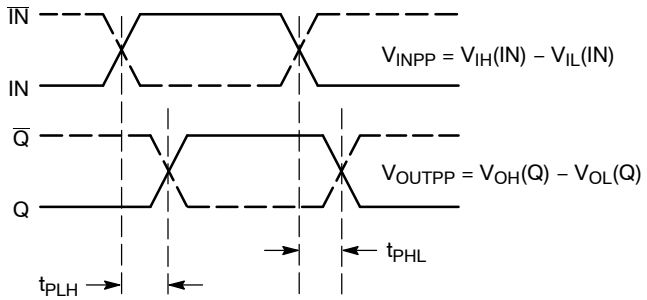


Figure 14. AC Reference Measurement

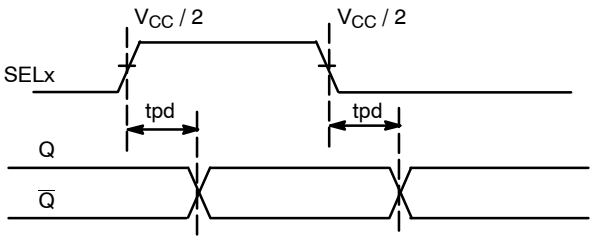


Figure 15. SELx to Qx Timing Diagram

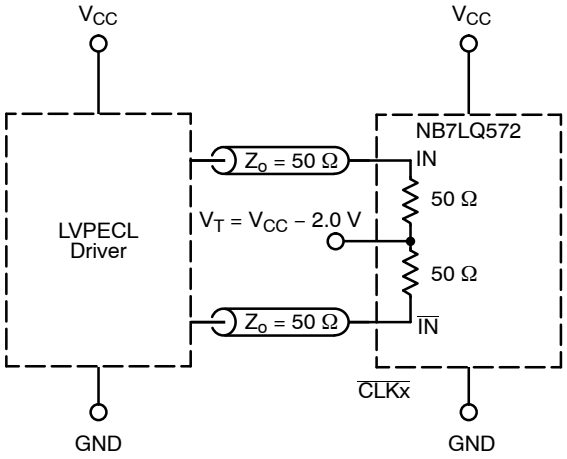


Figure 16. LVPECL Interface

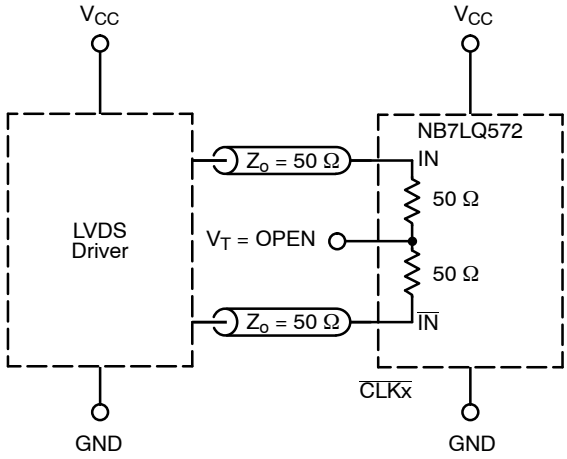


Figure 17. LVDS Interface

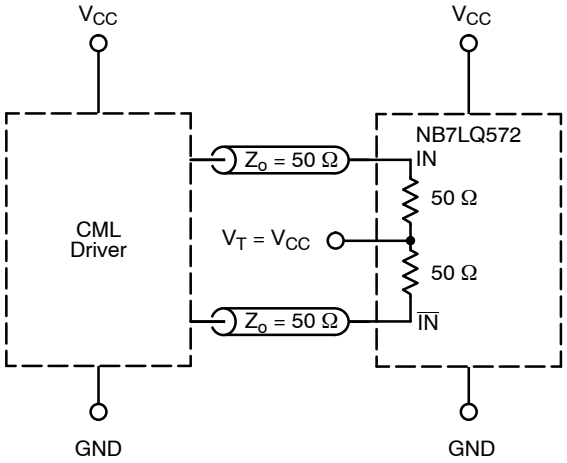


Figure 18. Standard 50 Ω Load CML Interface

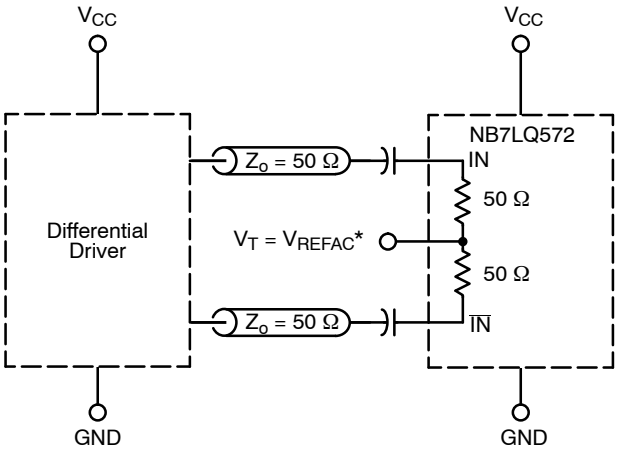


Figure 19. Capacitor–Coupled Differential Interface (V_T Connected to External V_{REFAC})

*V_{REFAC} bypassed to ground with a 0.01 μF capacitor.

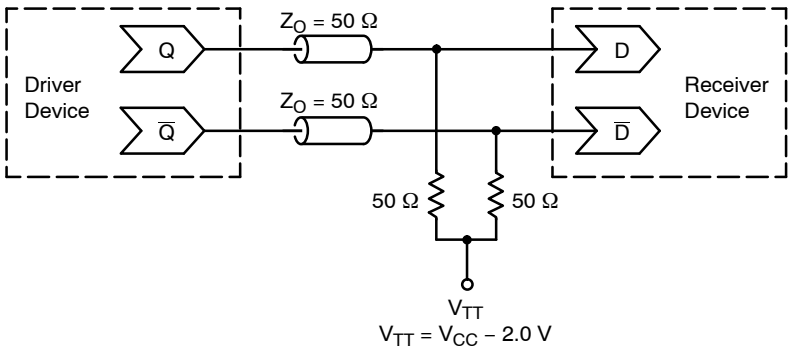


Figure 20. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices)

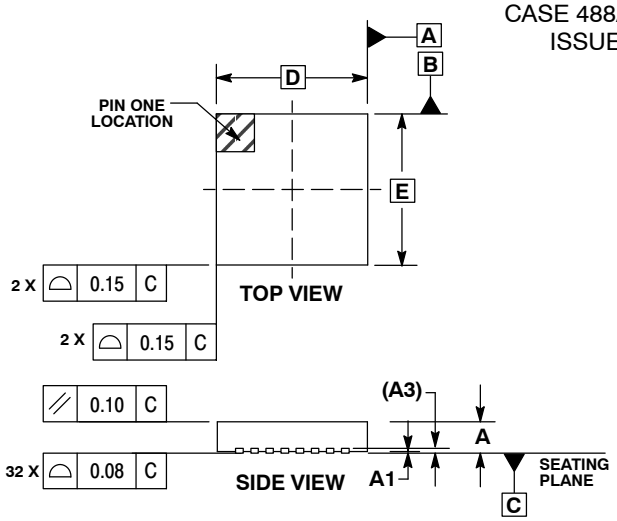
DEVICE ORDERING INFORMATION

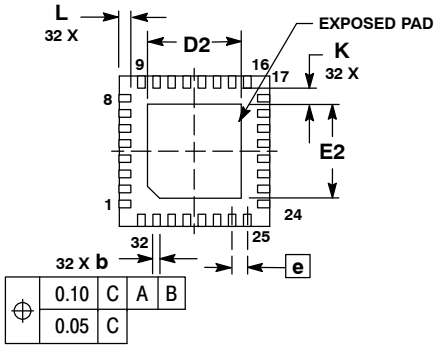
Device	Package	Shipping†
NB7LQ572MNG	QFN−32 (Pb−Free)	74 Units / Rail
NB7LQ572MNR4G	QFN−32 (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

QFN32 5*5*1 0.5 P
CASE 488AM−01
ISSUE O



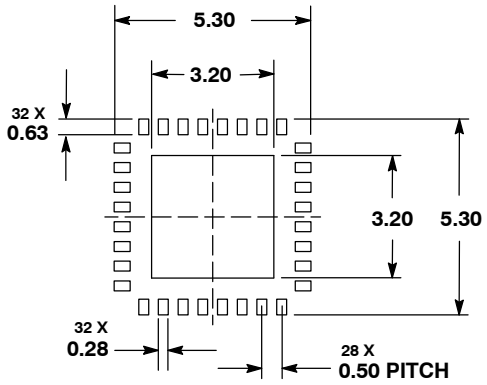


BOTTOM VIEW

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.800	0.900	1.000
A1	0.000	0.025	0.050
A3		0.200 REF	
b	0.180	0.250	0.300
D		5.00 BSC	
D2	2.950	3.100	3.250
E		5.00 BSC	
E2	2.950	3.100	3.250
e		0.500 BSC	
K	0.200	---	---
L	0.300	0.400	0.500

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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