# P420m 2.5-Inch PCIe NAND Flash SSD

## MTFDGAL350MAX, MTFDGAL700MAX

## Features

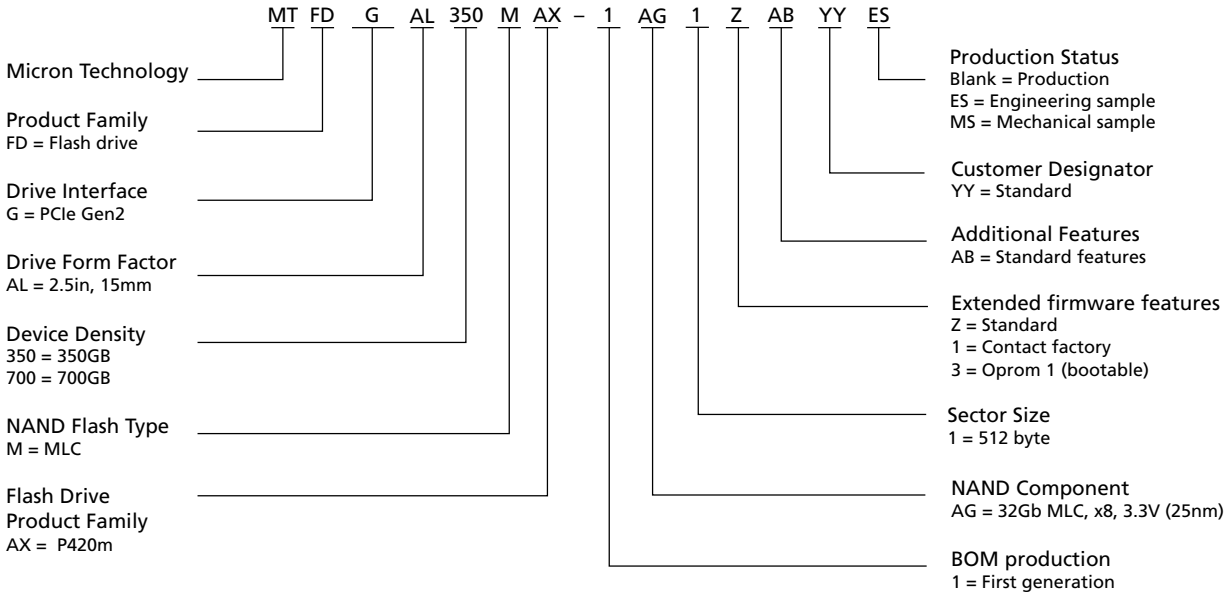
- Micron® 25nm MLC NAND Flash
- ONFI 2.1-compliant Flash interface
- PCIe Gen2 x4 host interface
- Capacity:[1] 350GB, 700GB
- Endurance[2, 3] (total bytes written):
  - 350GB: 2.3PB (4KB random write), 4.85PB (128KB sequential write)
  - 700GB: 4.6PB (4KB random write), 9.7PB (128KB sequential write)
- Temperature:
  - Operating: 0°C to +85°C[4]
  - Storage (in system): 0°C to +40°C[5]
  - Storage (on shelf): –40°C to +85°C[5]
  - Temperature throttling support
- ATA modes supported
  - PIO modes 3 and 4
  - Multiword DMA modes 0, 1, 2
  - Ultra DMA modes 0, 1, 2, 3, 4, 5, 6
  - ATA8-ACS2 command set support
  - ATA security feature command set and password login support
- Industry-standard 512-byte sector size support
- Full end-to-end data protection
- Native command queuing up to 256 commands
- Bootable[6]
- Surprise insertion/surprise removal (SISR) and hot-plug capable
- Power: <25W RMS
- Random read/write (steady state) performance[7]
  - Random read: Up to 400,000 IOPS (4KB IO size)
  - Random write: Up to 51,000 IOPS (4KB IO size)
- Sequential read/write (steady state) performance[7]
  - Sequential read: Up to 1.7 GB/s (128KB IO size)
  - Sequential write: Up to 500 MB/s (128KB IO size)
- Latency (queue depth = 1)[7]
  - READ latency: <100µs (MIN)
  - WRITE latency: ≤15µs posted (MIN)
- Custom drivers
  - Windows Server 2012 R2 (x86-64), Hyper-V (x86-64)
  - Windows Server 2012 (x86-64), Hyper-V (x86-64)
  - Windows Server 2008 R2 SP1 (x86-64), Hyper-V (x86-64)
  - Windows 8, 8.1 (x86-64 and x86)
  - Windows 7 (x86-64 and x86)
  - RHEL 5.5–5.10, 6.0–6.5, 7 (x86-64)
  - SLES 11 SP1, SP2, SP3 (x86-64)
  - VMware 5.0, 5.1 (x86-64)
  - VMware 5.5 (inbox driver)
  - Citrix XenServer 6.0.2, 6.1, 6.2
  - Ubuntu 12.04–12.04.4, 14.04 LTS Server (64-bit)
- Reliability
  - MTTF: 2.0 million hours
  - Static and dynamic wear leveling
  - Field-upgradable firmware
  - Uncorrectable bit error rate (UBER): <1 sector per $10^{17}$ bits read
  - Power Holdup Protection for MLC NAND
- Micron RAIN (redundant array of independent NAND) technology
- SMART command set support
- On-chip temperature monitoring
- Mechanical/electrical
  - 2.5-inch form factor: 69.85mm x 100.20mm x 15.00mm
  - PCIe-compliant, x4 lane combo connector
  - 12V power (±8%)
  - Weight: 350GB -142.9g; 700GB - 145.15g
- Shock (nonoperational): 400g at 2ms half-sine, 150g at 10ms half-sine
- Vibration (nonoperational): 3.1 grms 5–800Hz at 30 min/axis
- RoHS-compliant

Notes:
1. User capacity: 1GB = 1 billion bytes.
2. Lifetime endurance is measured not in years, but in the number of bytes that can be written to the device.
3. Workloads are 100% writes.
4. Operating temperature is the drive case temperature as measured by the SMART temperature attribute.
5. Assumes system is powered off and ready to be powered on.
6. Bootable option determined by part number; see Part Numbering Information (page 2). Boot ability may not be compatible with some systems.
7. See Performance Specifications (page 4) for details.

## Part Numbering Information

The Micron® P420m SSD is available in different configurations and densities. Visit www.micron.com for a list of valid part numbers.

### Figure 1: Part Number Chart



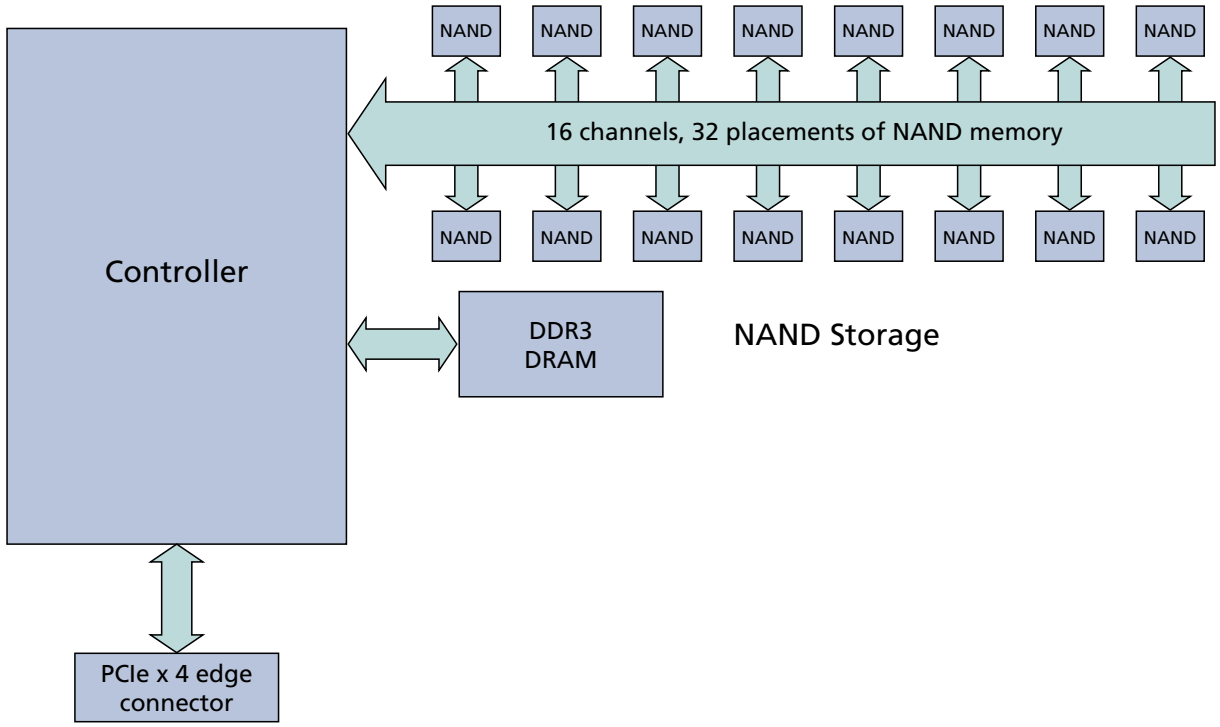

**Warranty**: Contact your Micron sales representative for further information regarding the product, including product warranties.

# General Description

Micron's solid state drive (SSD) is targeted at applications that require high performance and enterprise-class storage reliability. The P420m is designed to deliver extremely high IOPS performance by its ability to support up to 256 outstanding commands while ensuring full end-to-end data protection.

The P420m comes in a 2.5-inch form factor and uses a second-generation (Gen2) PCIe x4 lane interface on the host side and 16 ONFI 2.1-compliant channels on the Flash side.

**Figure 2: Functional Block Diagram**



# Architecture

The single-chip, Micron-developed ASIC controller, along with the host and Flash interfaces, provide an embedded ATA host bus adapter, a host/Flash translation layer, Flash maintenance, channel control, and Flash RAID (RAIN) protection.

Flash endurance and reliability are optimized through the Flash maintenance features, including static and dynamic wear leveling and RAIN protection. Most of these functions are implemented directly within the controller hardware to optimize performance. The device is shipped in the configurations shown below.

**Table 1: Configurations**

| User Capacity | NAND Flash Process | NAND Flash Density | Package Count | Die per BGA Package |
|---|---|---|---|---|
| 350GB | 25nm | 32Gb | 32 | 4 |
| 700GB | 25nm | 32Gb | 32 | 8 |

# Performance Specifications

**Table 2: Performance Specifications**

| Specification | 350GB | 700GB | Unit |
|---|---|---|---|
| Sequential read (up to) | 1.7 | 1.7 | GB/s |
| Sequential write (up to) | 310 | 500 | MB/s |
| Random read (up to) | 400,000 | 400,000 | IOPS |
| Random write (up to) | 24,000 | 51,000 | IOPS |
| READ latency | ≤100 (MIN) | ≤100 (MIN) | µs |
| WRITE latency | ≤15 posted (MIN) | ≤15 posted (MIN) | µs |

Notes:
1. Drive is erased and filled with zeroes to achieve preconditioned state .
2. 128KB transfers are used for sequential read/write values; 4KB transfers are used for random read/write values.
3. I/O performance numbers are measured in steady state using FIO with a preconditioned drive under RHEL 6.3 with a queue depth of 256 and with raw device access on systems with a single Intel Xeon E5-2667 2.90 GHz processor with 6 cores, 12 logical and hyper-threading enabled.
4. Steady state performance is defined as conforming to the SNIA V1.0 Performance Test Specification.
5. Performance numbers derived from tests at room temperature.
6. Latency performance numbers are measured using FIO with queue depth 1, random transfer, 4KB transfer size for READ latency, 4KB transfer size for WRITE latency.
7. Performance numbers are notated in base 10.

# Functional Description

## Data Retention

Data retention refers to the SSD's media (NAND Flash) capability to retain programmed data when the SSD is powered off. The two primary factors that influence data retention are degree of use (the number of PROGRAM/ERASE cycles on the media) and temperature.

The SSD provides power-off data retention of two months at 40°C (MAX) when total bytes written (TBW) is reached.

## Micron RAIN Technology

Redundant array of independent NAND (RAIN) is a technology developed by Micron designed to extend the lifespan of the P420m.

Residing in the P420m ASIC controller, RAIN is similar to redundant array of independent disks (RAID) technology, but instead of grouping and striping disks, RAIN groups and stripes storage elements on the SSD across multiple channels, generating and storing parity data along with user data (one page of parity for every seven pages of user data). This data structure (user data plus parity) enables complete, transparent data recovery if a single storage element (NAND, page, block, or die) fails. If a failure occurs, the P420m automatically detects it and transparently rebuilds the data. During this RAIN rebuild process, the drive's performance is reduced temporarily but will recover after the rebuild process completes.

## Wear Leveling

Wear leveling is a technique that spreads Flash block use over the entire memory array to equalize the PROGRAM/ERASE cycles on all blocks in the array. This helps to enhance the lifespan of the SSD. The P420m supports both static and dynamic wear leveling.

Static wear leveling considers all Flash blocks in the SSD regardless of data content or access and maintains an even level of wear across the drive. Dynamic wear leveling monitors available free space on the drive and dynamically moves data between Flash blocks to equalize wear on each block. Both techniques are used together within the controller to optimally balance the wear profile of the Flash array along with the drive's lifespan.

# SMART Attribute Summary

### Table 3: SMART Command Reference[1]

| Attribute ID | Hex ID | Name | SMART Trip | Description |
|---|---|---|---|---|
| 9 | 0x09 | Power-on hours count | No | Lifetime powered-on hours, from the time the device leaves the factory |
| 12 | 0x0C | Power cycle count | No | Count of power cycles |
| 170 | 0xAA | New failing block count | No | Grown defects |
| 171 | 0xAB | Program fail count | No | Number of NAND program status failures |
| 172 | 0xAC | Erase fail count | No | Number of NAND erase status failures |
| 174 | 0xAE | Unexpected power loss count | No | Number of unexpected power-loss occurrences |
| 187 | 0xBB | Reported uncorrectable errors count | No | Number of ECC correction failures |
| 188 | 0xBC | Command timeout count | No | Number of command timeouts, defined by an active command being interrupted by a HRESET, COMRESET, SRST, or other command |
| 194 | 0xC2 | Temperature | No | The on-die temperature sensor within the controller ASIC in degrees C, capturing the lifetime high and low temperatures measured |
| 202 | 0xCA | Percentage of the rated lifetime used | No | Cumulative erase count / lifetime erase count as expressed as a percent. Lifetime erase count is the total number of available blocks * block endurance for the flash technology, read directly from the NAND device. |
| 232 | 0xE8 | Available reserved space | No | Percentage of spare blocks remaining<br>Spare block count |
| 241 | 0xF1 | Power-on (minutes) | No | Lifetime power-on time in minutes |
| 242 | 0xF2 | Write protect progress | No | Progress toward WRITE PROTECT mode: reports 100% when the drive becomes read only |

Note: 1. Attribute/Hex IDs are noted for distribution product. Specific OEMs may have different ID values, but the same list of SMART commands applies.

# Logical Block Address Configuration

The number of logical block addresses (LBA) reported by the device ensures sufficient storage space for the specified density. Standard LBA settings based on the IDEMA standard (LBA1-02) are shown below.

**Table 4: Standard LBA Settings**

| Drive Size | Total LBA | | Max LBA | | User Available Bytes (Unformatted) |
|---|---|---|---|---|---|
| | Decimal | Hexadecimal | Decimal | Hexadecimal | |
| 350GB | 683,747,568 | 28C128F0 | 683,747,567 | 28C128EF | 350,078,754,816 |
| 700GB | 1,367,473,968 | 5181FF30 | 1,367,473,967 | 5181FF2F | 700,146,671,616 |

Note: 1. 1GB = 1 billion bytes; user capacity.

# Physical Configuration

**Table 5: Nominal Dimensions and Weight**

| Specification | Value | Unit |
|---|---|---|
| Height | 15.00 | mm |
| Width | 69.85 | mm |
| Length | 100.20 | mm |
| Unit weight | 142.9 (350GB)<br>145.15 (700GB) | g |

# Interface Connectors

The host interface connector conforms to the PCIe Electromechanical Specification V2.0, section 5, Table 5-1. It is a four-lane, gold-finger connector with 1mm pitch spacing.

A mechanical indent is used to separate the PCIe power pins from the differential signal contacts. The pins are numbered below in ascending order from left to right. Side B refers to component side and Side A refers to the solder side.

**Table 6: PCIe Interface Connector Pin Assignments**

| Type | Drive | Usage | Signal Description | Name | Mating | Pin# |
|---|---|---|---|---|---|---|
| HS | | | Ground | GND | 2nd | S1 |
| HS | Input | | DNU | SOT+(A+) | 3rd | S2 |
| HS | Input | | DNU | SOT-(A-) | 3rd | S3 |
| HS | | | Ground | GND | 2nd | S4 |
| HS | Output | | DNU | SOR-(B-) | 3rd | S5 |
| HS | Output | | DNU | SOR+(B+) | 3rd | S6 |
| HS | | | Ground | GND | 2nd | S7 |
| LS | Input | Dual port | DNU | RefClk+1 | 3rd | E1 |
| LS | Input | Dual port | SNU | RefClk+1 | 3rd | E2 |
| LS | Input | PCI opt | 3.3V for SM BUS | 3.3 AUX | 3rd | E3 |
| LS | Input | Dual port | DNU | PCIeRst1 | 3rd | E4 |
| LS | Input | PCIe only | PCIe primary reset | PCIeRst0 | 3rd | E5 |
| LS | Input | PCIe opt | Optional reserved Pin | Wake/RSVD | 3rd | E6 |
| Power | NC | | DNU | 3.3V | 3rd | P1 |
| | NC | | | | 3rd | P2 |
| | NC | | | | 2nd | P3 |
| | | All | Hot plug | Ground | 1st | P4 |
| | | All | | | 2nd | P5 |
| | | All | | | 2nd | P6 |
| | NC | | DNU | 5V | 2nd | P7 |
| | NC | | | | 3rd | P8 |
| | NC | | | | 3rd | P9 |
| | | All | | Presence detect | 2nd | P10 |
| | LED | All | | Activity/staggard spin-up | 3rd | P11 |
| | | All | Hot plug | Ground | 1st | P12 |
| | Input | All | Only power for PCIe SSD | 12V | 2nd | P13 |
| | Input | All | | | 3rd | P14 |
| | Input | All | | | 3rd | P15 |
| LS | Input | PCIe only | PCIe primary RefClk+ | RefClk0+ | 3rd | E7 |
| LS | Input | PCIe only | PCIe primary RefClk- | RefClk0- | 3rd | E8 |

**Table 6: PCIe Interface Connector Pin Assignments (Continued)**

| Type | Drive | Usage | Signal Description | Name | Mating | Pin# |
|---|---|---|---|---|---|---|
| HS | | | Ground | GND | | E9 |
| HS | Input | PCIe only | PCIe 0 transmit + | POT+ | | E10 |
| HS | Input | PCIe only | PCIe 0 transmit - | POT- | | E11 |
| HS | | | Ground | GND | | E12 |
| HS | Output | PCIe only | PCIe 0 receive - | POR- | | E13 |
| HS | Output | PCIe only | PCIe 0 receive + | POR+ | | E14 |
| HS | | | Ground | GND | | E15 |
| LS | | TBD | Reserve | RSVD | | E16 |
| HS | | | Ground | GND | 2nd | S8 |
| HS | Input | | DNU | S1T+ | 3rd | S9 |
| HS | Input | | DNU | S1T- | 3rd | S10 |
| HS | | | Ground | GND | 2nd | S11 |
| HS | Output | | DNU | S1R- | 3rd | S12 |
| HS | Output | | DNU | S1R+ | 3rd | S13 |
| HS | | | Ground | GND | 2nd | S14 |
| LS | | TBD | Reserved | RSVD | 3rd | E17 |
| HS | | | Ground | GND | 2nd | E18 |
| HS | Input | PCIe+SAS | PCIe 1 transmit + / SAS 2 transmit + | P1T+/S2T+ | 3rd | E19 |
| HS | Input | PCIe+SAS | PCIe 1 transmit - / SAS 2 transmit - | P1T-/S2T- | 3rd | E20 |
| HS | | | Ground | GND | 2nd | E21 |
| HS | Output | PCIe+SAS | PCIe 1 receive - / SAS 2 receive - | P1R-/S2R- | 3rd | E22 |
| HS | Output | PCIe+SAS | PCIe 1 receive + / SAS 2 receive + | P1R+/S2R+ | 3rd | E23 |
| HS | | | Ground | GND | 2nd | E24 |
| HS | Input | PCIe+SAS | PCIe 2 transmit + / SAS 3 transmit + | P2T+/S3T+ | 3rd | E25 |
| HS | Input | PCIe+SAS | PCIe 2 transmit - / SAS 3 transmit - | P2T-/S3T- | 3rd | E26 |
| HS | | | Ground | GND | 2rd | E27 |
| HS | Output | PCIe+SAS | PCIe 2 receive - / SAS 3 receive - | P2R-/S3R- | 3rd | E28 |
| HS | Output | PCIe+SAS | PCIe 2 receive + / SAS 3 receive + | P2R+/S3R+ | 3rd | E29 |
| HS | | | Ground | GND | 2 rd | E30 |
| HS | Input | PCIe only | PCIe 3 transmit + | P3T+ | 3rd | E31 |
| HS | Input | PCIe only | PCIe 3 transmit - | P3T- | 3rd | E32 |
| HS | | | Ground | GND | 2nd | E33 |

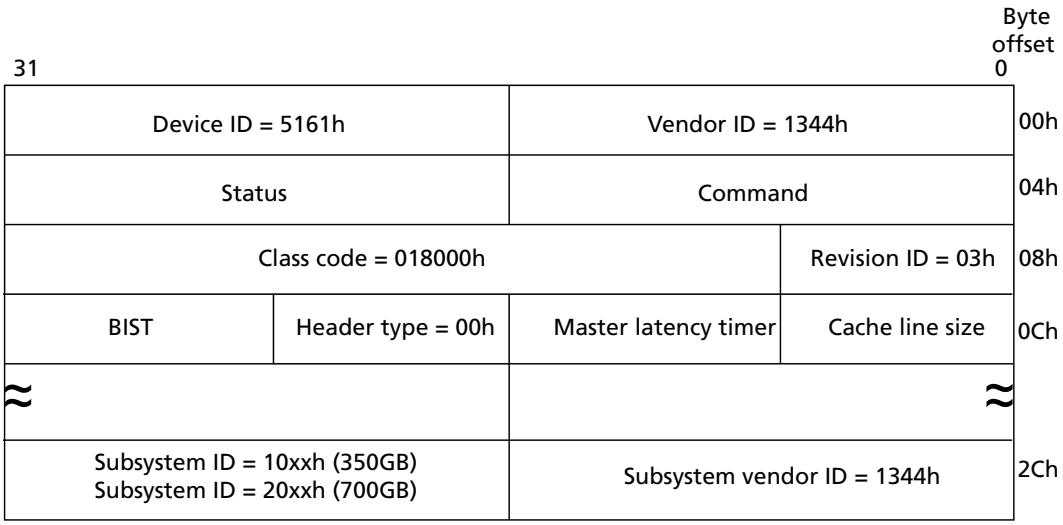
**Table 6: PCIe Interface Connector Pin Assignments (Continued)**

| Type | Drive | Usage | Signal Description | Name | Mating | Pin# |
|---|---|---|---|---|---|---|
| HS | Output | PCIe only | PCIe 3 receive - | P3R- | 3rd | E34 |
| HS | Output | PCIe only | PCIe 3 receive - | P3R+ | 3rd | E35 |
| HS | | | Ground | GND | 2nd | E36 |
| LS | Bi-Dir | PCIe opt | SM-Bus clock | SMClk | 3rd | E37 |
| LS | Bi-Dir | PCIe opt | SM-Bus clock | SMData | 3rd | E38 |
| LS | Bi-Dir | Dual port | DNU | PCIeDualEn# | 3rd | E39 |

Note: 1. Dual port is not supported.

# PCIe Header

**Figure 3: PCIe Header**




Note: 1. Standard Distribution Subsystem ID is 1000h for 350GB and 2000h for 700GB. A non-zero value for xx indicates an OEM product.

# Commands

### Table 7: Supported ATA Command Set

See ATA–8 ACS–2 specification for command details

| Commands | ATA Protocol | CMD Code | Feature Codes |
|---|---|---|---|
| CHECK POWER MODE | ND | 0xE5 | – |
| DEVICE CONFIGURATION FREEZE LOCK | ND | 0xB1 | 0xC1 |
| DEVICE CONFIGURATION IDENTIFY | PI | 0xB1 | 0xC2 |
| DEVICE CONFIGURATION RESTORE | ND | 0xB1 | 0xC0 |
| DEVICE CONFIGURATION SET | PO | 0xB1 | 0xC3 |
| DOWNLOAD MICROCODE | PO | 0x92 | – |
| EXECUTE DEVICE DIAGNOSTIC | DD | 0x90 | – |
| FLUSH CACHE | ND | 0xE7 | – |
| FLUSH CACHE EXT | ND | 0xEA | – |
| IDENTIFY DEVICE | PI | 0xEC | – |
| IDLE | ND | 0xE3 | – |
| IDLE IMMEDIATE | ND | 0xE1 | – |
| INITIALIZE DEVICE PARAMETERS | ND | 0x91 | – |
| READ BUFFER | PI | 0xE4 | – |
| READ DMA | DM | 0xC8 | – |
| READ DMA WO RETRIES | DM | 0xC9 | – |
| READ DMA EXT | PI | 0x25 | – |
| READ FPMDA QUEUED | NCQ | 0x60 | – |
| READ LOG EXT | PI | 0x2F | – |
| READ MULTIPLE | PI | 0xC4 | – |
| READ MULTIPLE EXT | PI | 0x29 | – |
| READ NATIVE MAX ADDRESS | ND | 0xF8 | – |
| READ NATIVE MAX ADDRESS EXT | ND | 0x27 | – |
| READ SECTORS | PI | 0x20 | – |
| READ SECTORS WO RETRIES | PI | 0x21 | – |
| READ SECTORS EXT | PI | 0x24 | – |
| READ VERIFY SECTORS | ND | 0x40 | – |
| READ VERIFY SECTORS WO RETRIES | ND | 0x41 | – |
| READ VERIFY SECTOR EXT | ND | 0x42 | – |
| RECALIBRATE | ND | 0x1x | – |
| SECURITY DISABLE PASSWORD | PO | 0xF6 | – |
| SECURITY ERASE PREPARE | ND | 0xF3 | – |
| SECURITY ERASE UNIT | PO | 0xF4 | – |
| SECURITY FREEZE LOCK | ND | 0xF5 | – |
| SECURITY SET PASSWORD | PO | 0xF1 | – |
| SECURITY UNLOCK | PO | 0xF2 | – |

**Table 7: Supported ATA Command Set (Continued)**

See ATA–8 ACS–2 specification for command details

| Commands | ATA Protocol | CMD Code | Feature Codes |
|---|---|---|---|
| SEEK | ND | 0x7x | – |
| SET FEATURES | ND | 0xEF | VARIOUS |
| SET MAX ADDRESS | ND | 0xF9 | 0x00 |
| SET NATIVE MAX ADDRESS EXT | ND | 0x37 | – |
| SET MAX SET PASSWORD | ND | 0xF9 | 0x01 |
| SET MAX LOCK | ND | 0xF9 | 0x02 |
| SET MAX FREEZE LOCK | ND | 0xF9 | 0x04 |
| SET MAX UNLOCK | ND | 0xF9 | 0x03 |
| SET MULTIPLE MODE | ND | 0xC6 | – |
| SLEEP | ND | 0xE6 | – |
| SMART DISABLE OPERATIONS | ND | 0xB0 | 0xD9 |
| SMART ENABLE/DISABLE AUTOSAVE | ND | 0xB0 | 0xD2 |
| SMART ENABLE OPERATIONS | ND | 0xB0 | 0xD8 |
| SMART EXECUTE OFF–LINE IMMEDIATE | ND | 0xB0 | 0xD4 |
| SMART READ DATA / READ ATTRIBUTE VALUES | PI | 0xB0 | 0xD0 |
| SMART READ LOG | PI | 0xB0 | 0xD5 |
| SMART RETURN STATUS | ND | 0xB0 | 0xDA |
| SMART WRITE LOG | PO | 0xB0 | 0xD6 |
| SMART READ ATTRIBUTE/WARRANTY THRESHOLDS | PI | 0xB0 | 0xD1 |
| STANDBY | ND | 0xE2 | – |
| STANDBY IMMEDIATE | ND | 0xE0 | – |
| WRITE DMA | DM | 0xCA | – |
| WRITE DMA WO RETRIES | DM | 0xCB | – |
| WRITE DMA EXT | DM | 0x35 | – |
| WRITE DMA FUA EXT | DM | 0x3D | – |
| WRITE FPDMA QUEUED | NCQ | 0x61 | – |
| WRITE LOG EXT | PO | 0x3F | – |
| WRITE MULTIPLE | PO | 0xC5 | – |
| WRITE MULTIPLE EXT | PO | 0x39 | – |
| WRITE MULTIPLE FUA EXT | PO | 0xCE | – |
| WRITE SECTORS | PO | 0x30 | – |
| WRITE SECTORS WO RETRIES | PO | 0x31 | – |
| WRITE SECTORS EXT | PO | 0x34 | – |

# Reliability

Micron's SSDs incorporate advanced technology for defect and error management. They use various combinations of hardware-based error correction algorithms and firmware-based static and dynamic wear-leveling algorithms.

Over the life of the SSD, uncorrectable errors may occur. An uncorrectable error is defined as data that is reported as successfully programmed to the SSD but when it is read out of the SSD, the data differs from what was programmed.

**Table 8: Uncorrectable Bit Error Rate**

| Uncorrectable Bit Error Rate | Operation |
|---|---|
| < 1 sector per $10^{17}$ bits read | READ |

## Mean Time to Failure

The mean time to failure (MTTF) for the device was measured in a Reliability Demonstration Test at over 2 million hours.

**Table 9: MTTF**

| Capacity | MTTF (Operating Hours) |
|---|---|
| 350GB | 2 million |
| 700GB | |

## Endurance

Endurance for the SSD can be predicted based on the usage conditions applied to the device, the internal NAND component PROGRAM/ERASE cycles, the write amplification factor, and the wear-leveling efficiency of the drive. The table below shows the drive lifetime for each SSD capacity based on predefined usage conditions. The SSD implements wear leveling in hardware to optimize performance and efficiency while maintaining Flash endurance. The device also provides optional long-term wear management support.

**Table 10: Drive Lifetime**

| Capacity | Workload | Drive Lifetime (Total Bytes Written) | Drive Fills Per Day | Retention |
|---|---|---|---|---|
| 350GB | 4KB 100% random writes | 2.3PB | 3.7 (5 years) | 2 months |
| | 128KB 100% sequential writes | 4.85PB | 7.6 (5 years) | 2 months |
| 700GB | 4KB 100% random writes | 4.6PB | 3.7 (5 years) | 2 months |
| | 128KB 100% sequential writes | 9.7PB | 7.6 (5 years) | 2 months |

## Power Holdup Protection

If power is interrupted at any time while data is being programmed into the NAND, it is possible that data loss may occur and the MLC NAND's lower page may become corrupted. This can cause drive errors to be reported to the host. To prevent these errors from occurring, the P420m drive implements an energy storage solution called a Power Holdup circuit that maintains power to the NAND while it is being programmed, even if power to the system is interrupted. By supporting Power Holdup, the P420m drive assures data integrity in the drive is preserved – preventing the loss of data and the reporting of drive errors to the host.

# Electrical Characteristics

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Table 11: Operating Voltage and Power

| Electrical Characteristic | Value |
|---|---|
| Voltage requirement | 12Vdc (±8%) |
| Active power | 25W RMS |
| Standby power (idle) | 8W RMS (TYP), 10W RMS (MAX) |

### Table 12: Environmental Conditions

| Parameter/Condition | Min | Max | Unit | Notes |
|---|---|---|---|---|
| Operating temperature (as indicated by SMART temperature) | 0 | 85 | °C | 1 |
| Operating ambient temperature | 0 | 55 | °C | 2 |
| Storage temperature (in system) | 0 | 40 | °C | 3 |
| Storage temperature (offline) | –40 | 85 | °C | 4 |
| Operating airflow | 1.0 | – | m/s | 5 |

Notes:
1. If SMART temperature exceeds 85°C, write performance is throttled.
2. Temperature of air impinging on the drive.
3. Assumes system is powered off and ready to be powered on.
4. Contact Micron for additional information.
5. Airflow must flow along the length of the drive, parallel to and through any cooling fins; 1.5m/s operating airflow is recommended.

### Table 13: Shock and Vibration

| Parameter/Condition | Specification |
|---|---|
| Shock (nonoperational) | 400g at 2ms half-sine, 150g at 10ms half-sine |
| Vibration (nonoperational) | 3.1 grms 5–800Hz at 30 min/axis |

# Compliance

The device complies with the following specifications:

- RoHS - Restriction of Hazardous Substances
- China RoHS
- WEEE Waste Electric and Electronic Equipment
- Halogen Free - meets IPC low-halogen requirements
- CE (Europe) EN55022/EN55024 (Class A)
- TUV (Germany) EN60950
- UL (US/Canada) EN60950
- FCC (US) 47CFR Part 15 Class A
- BSMI (Taiwan) CNS 13438 Class A
- VCCI (Japan) EN 55022/CISPR 22 Class A
- C-TICK (AUS/NZ) CISPR22
- ICES (Canada) CISPR22 Class A
- KC (Korea) - EN55022/EN55024 Class A, KCC-REM-MU2-MTFDGALZZZMAX

## FCC Rules

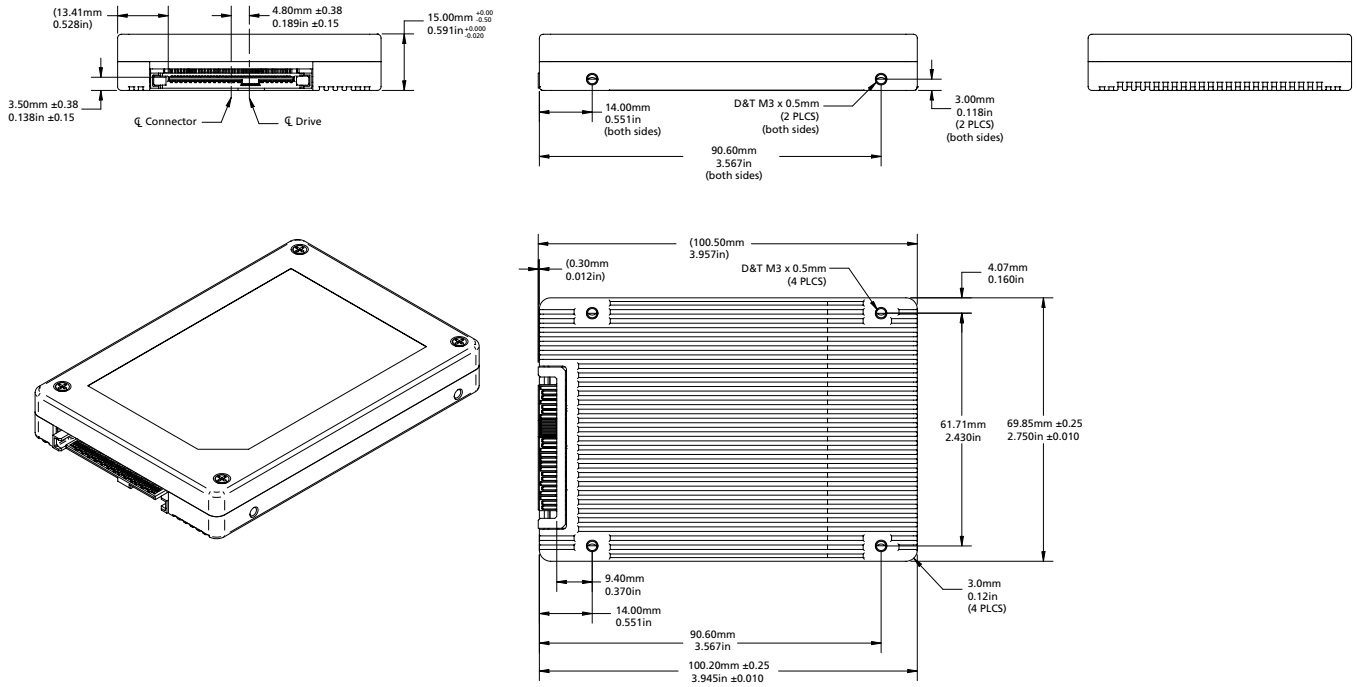
This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

# References

- PCI Express Base Specification V2.1
- PCI Express CEM Specification V2.0
- ATA8-ACS2 Specification
- IDEMA Specification
- Telcordia SR-322 Procedures
- SNIA Performance Test Specification V1.0
- SFF-8639 Specification V1.0

# Drive Dimensions

### Figure 4: 2.5-Inch Dimensions



# Revision History

## Rev. U – 8/14

- Updated custom drivers status

## Rev. T – 7/14

- Changed documentation status

## Rev. S – 7/14

- Updated custom drivers

## Rev. R – 6/14

- Updated signal descriptions in the PCIe Interface Connector Pin Assignments table

## Rev. Q – 4/14

- Status changed to Production

## Rev. P – 3/14

- Updated Compliance section

## Rev. O – 2/14

- Updated Compliance and References sections

## Rev. N – 1/14

- Updated 12V power range

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- Updated 12V power range

## Rev. M – 1/14

- Updated endurance and data retention specifications
- Updated performance specifications
- Updated electrical specifications
- Updated temperature specifications and notes
- Updated custom drivers
- Updated Figure 1: Part Number Chart
- Updated Compliance and References sections

## Rev. L – 10/13

- Updated temperature specifications and notes

## Rev. K – 10/13

- Updated custom drivers list
- Updated pin assignment descriptions

## Rev. J – 9/13

- Updated custom drivers list

## Rev. I – 7/13

- Updated note 3 in Performance Specifications section

## Rev. H – 6/13

- Added power values

## Rev. G – 4/13

- Updated Part Number chart
- Updated supported drivers
- Added drive dimensions drawing

## Rev. F – 3/13

- Updated power and WRITE latency values
- Updated supported drivers

## Rev. E – 2/13

- Updated Functional Description section

## Rev. D – 12/12

- Updated capacity values and corresponding specifications

## Rev. C – 8/12

- Updated capacity values and corresponding specifications

## Rev. B – 6/12

- Added Power Holdup Protection
- Changed Device ID and updated Subsystem ID in Figure 3

## Rev. A – 3/12

- Initial release; Preliminary status

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