MC74AC646, MC74ACT646

Octal Transceiver/Register with 3-State Outputs (Non-inverting)

The MC74AC646/74ACT646 consist of registered bus transceiver circuits, with outputs, D−type flip−flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW−to−HIGH transition of the appropriate clock pin (CAB or CBA). The four fundamental data handling functions available are illustrated Figures 1 to 4.

- Independent Registers for A and B Buses
- Multiplexed Real−Time and Stored Data Transfers
- Choice of True and Inverting Data Paths
- 3−State Outputs
- 300 mil Slim Dual In−Line Package
- Outputs Source/Sink 24 mA
- ′ACT646 Has TTL Compatible Inputs
- **These devices are available in Pb−free package(s). Specifications herein apply to both standard and Pb−free devices. Please see our website at www.onsemi.com for specific Pb−free orderable part numbers, or contact your local ON Semiconductor sales office or representative.**

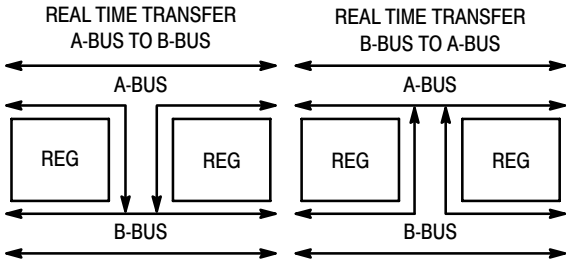

Figure 1.

Figure 2.

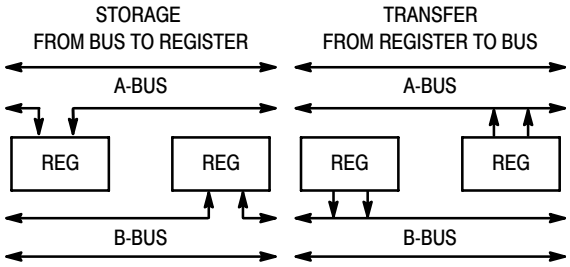

Figure 3.

Figure 4.

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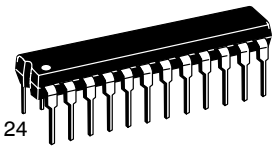
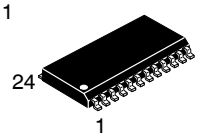


PDIP−24
N SUFFIX
CASE 724

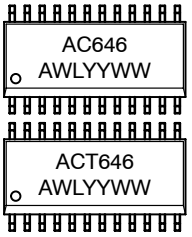


SO−24
DW SUFFIX
CASE 751E

MARKING DIAGRAMS

PDIP−24

SO−24



A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC74AC646N	PDIP−24	15 Units/Rail
MC74ACT646N	PDIP−24	15 Units/Rail
MC74AC646DW	SOIC−24	30 Units/Rail
MC74AC646DWR2	SOIC−24	1000 Tape & Reel
MC74ACT646DW	SOIC−24	30 Units/Rail
MC74ACT646DWR2	SOIC−24	1000 Tape & Reel

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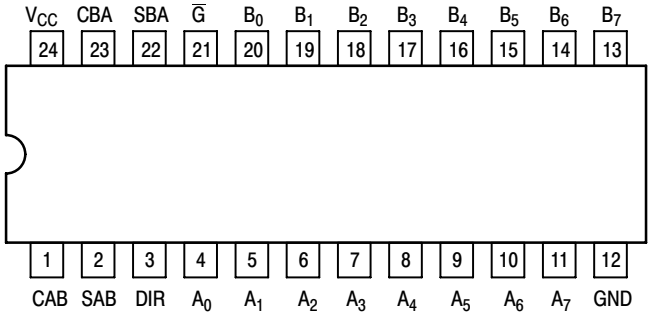


Figure 5. Pinout: 24−Lead Packages Conductors
(Top View)

PIN ASSIGNMENT

PIN	FUNCTION
A_0−A_7	Data Register Inputs Data Register A Outputs
B_0−B_7	Data Register B Inputs Data Register B Outputs
CAB, CBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
DIR, $\overline{G}$	Output Enable Inputs

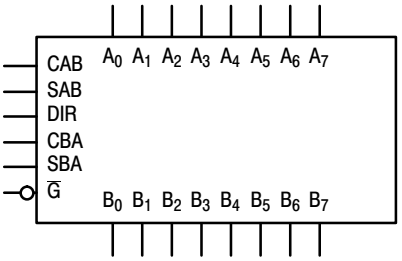
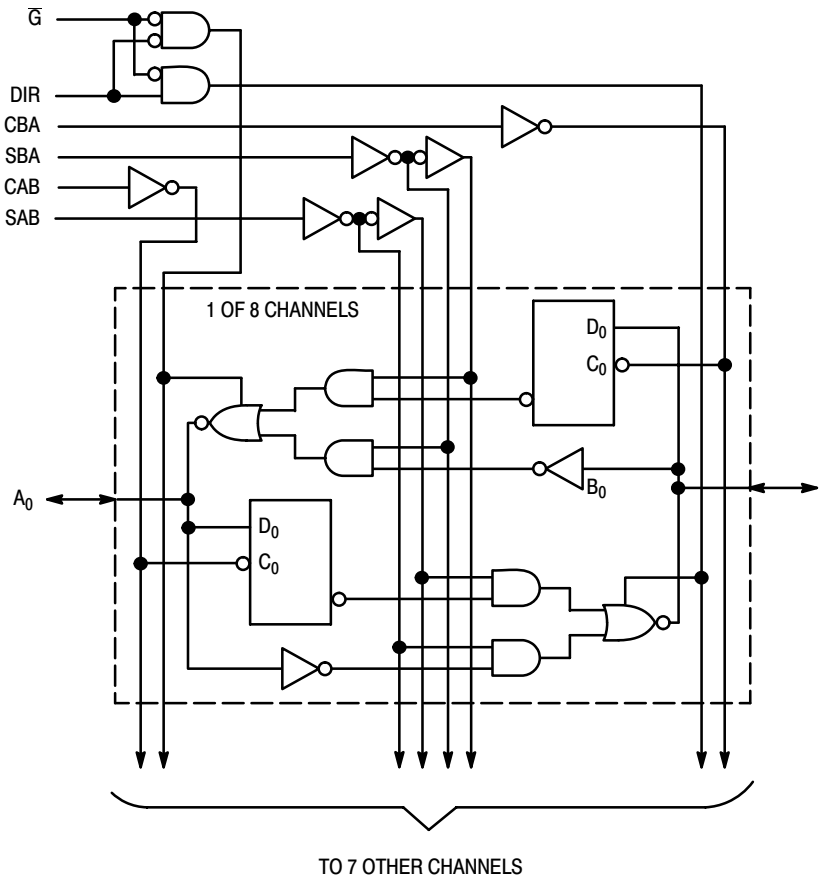


Figure 6. Logic Symbol



NOTE: This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 7. Logic Diagram

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FUNCTION TABLE

Inputs						Data I/O*		Operation or Function
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A_0–A_7	B_0–B_7	
H H	X X	H or L ⌐	H or L ⌐	X X	X X	Input	Input	Isolation Store A and B Data
L L	L L	X X	X X	X X	L H	Output	Input	Real Time B Data to A Bus Stored B Data to A Bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real Time A Data to B Bus Stored A Data to B Bus

*The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW−to−HIGH transition of the appropriate clock inputs.

NOTE: H = HIGH Voltage Level; L = LOW Voltage Level; X = Immaterial; ⌐ = LOW−to−HIGH Transition

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−0.5 to V_{CC} +0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC} +0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Sink/Source Current, per Pin	±50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	±50	mA
T_{stg}	Storage Temperature	−65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	′AC	2.0	5.0	6.0	V
		′ACT	4.5	5.0	5.5	
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Ref. to GND)		0	–	V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) ′AC Devices except Schmitt Inputs	V_{CC} @ 3.0 V	–	150	–	ns/V
		V_{CC} @ 4.5 V	–	40	–	
		V_{CC} @ 5.5 V	–	25	–	
t_r, t_f	Input Rise and Fall Time (Note 2) ′ACT Devices except Schmitt Inputs	V_{CC} @ 4.5 V	–	10	–	ns/V
		V_{CC} @ 5.5 V	–	8.0	–	
T_J	Junction Temperature (PDIP)		–	–	140	°C
T_A	Operating Ambient Temperature Range		−40	25	85	°C
I_{OH}	Output Current − High		–	–	−24	mA
I_{OL}	Output Current − Low		–	–	24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

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DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74AC		74AC	Unit	Conditions
			T_A = +25°C		T_A = –40°C to +85°C		
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	2.1 3.15 3.85	2.1 3.15 3.85	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{IL}	Maximum Low Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	0.9 1.35 1.65	0.9 1.35 1.65	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{OH}	Minimum High Level Output Voltage	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	V	I_{OUT} = –50 μA
		3.0 4.5 5.5	– – –	2.56 3.86 4.86	2.46 3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} –12 mA I_{OH} –24 mA –24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V	I_{OUT} = 50 μA
		3.0 4.5 5.5	– – –	0.36 0.36 0.36	0.44 0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	–	±0.1	±1.0	μA	V_I = V_{CC}, GND
I_{OZT}	Maximum 3-State Current	5.5	–	±0.6	±6.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5	–	–	75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5	–	–	–75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	–	8.0	80	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

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AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay Clock to Bus	3.3 5.0	4.0 2.5	10.5 7.5	16.5 12	3.0 2.0	18.5 13	ns	3–6
t_{PHL}	Propagation Delay Clock to Bus	3.3 5.0	3.0 2.0	9.5 6.5	14.5 10.5	2.5 1.5	16 11.5	ns	3–6
t_{PLH}	Propagation Delay Bus to Bus	3.3 5.0	2.5 1.5	7.5 5.0	12 8.0	2.0 1.0	13.5 9.0	ns	3–5
t_{PHL}	Propagation Delay Bus to Bus	3.3 5.0	1.5 1.5	7.5 5.0	12.5 9.0	1.5 1.0	13.5 9.5	ns	3–5
t_{PLH}	Propagation Delay SBA or SAB to A_n or B_n (w/A_n or B_n HIGH or LOW)	3.3 5.0	2.0 1.5	8.5 6.0	13.5 10	1.5 1.5	15.5 11	ns	3–6
t_{PHL}	Propagation Delay SBA or SAB to A_n or B_n (w/A_n or B_n HIGH or LOW)	3.3 5.0	1.5 1.5	8.5 6.0	13.5 10	1.5 1.5	15 11	ns	3–6
t_{PZH}	Enable Time $\overline{G}$ to A_n or B_n	3.3 5.0	2.5 1.5	7.0 5.0	11.5 8.5	2.0 1.5	12.5 9.0	ns	3–7
t_{PZL}	Enable Time $\overline{G}$ to A_n or B_n	3.3 5.0	2.5 1.5	7.5 5.5	12.5 9.0	2.0 1.5	14 10	ns	3–8
t_{PHZ}	Disable Time $\overline{G}$ to A_n or B_n	3.3 5.0	3.0 2.0	8.0 6.5	12.5 10	2.5 2.0	13.5 11	ns	3–7
t_{PLZ}	Disable Time $\overline{G}$ to A_n or B_n	3.3 5.0	2.0 1.5	7.5 6.0	12 9.5	2.0 1.5	13.5 10.5	ns	3–8
t_{PZH}	Enable Time DIR to A_n or B_n	3.3 5.0	2.0 1.5	6.5 5.0	11 7.5	1.5 1.0	12 8.5	ns	3–7
t_{PZL}	Enable Time DIR to A_n or B_n	3.3 5.0	2.5 1.5	7.0 5.0	11.5 8.0	2.0 1.0	13 9.0	ns	3–8
t_{PHZ}	Disable Time DIR to A_n or B_n	3.3 5.0	2.5 1.5	7.5 5.5	11.5 9.5	1.5 1.5	12.5 10	ns	3–7
t_{PLZ}	Disable Time DIR to A_n or B_n	3.3 5.0	1.5 1.5	7.5 5.5	12 9.5	1.5 1.5	13.5 10.5	ns	3–8

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

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AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C C_L = 50 pF		74AC T_A = −40°C to +85°C C_L = 50 pF	Unit	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW Bus to Clock	3.3 5.0	2.0 1.5	5.0 4.0	5.5 4.5	ns	3–9
t_h	Hold Time, HIGH or LOW Bus to Clock	3.3 5.0	−1.5 −0.5	0 0.5	0 1.0	ns	3–9
t_w	Clock Pulse Width HIGH or LOW	3.3 5.0	2.0 2.0	3.5 3.5	4.5 3.5	ns	3–6

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C		74ACT T_A = −40°C to +85°C	Unit	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5	– –	3.86 4.86	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5	– –	0.36 0.36	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	–	±0.1	±1.0	μA	V_I = V_{CC}, GND
ΔI_{CCT}	Additional Max. I_{CC}/Input	5.5	0.6	–	1.5	mA	V_I = V_{CC} − 2.1 V
I_{OZT}	Maximum 3-State Current	5.5	–	±0.6	±6.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5	–	–	75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5	–	–	−75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	–	8.0	80	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

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AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay Clock to Bus	5.0	3.5	12.0	14.5	3.0	16.0	ns	3–6
t_{PHL}	Propagation Delay Clock to Bus	5.0	4.0	12.0	14.5	3.5	16.0	ns	3–6
t_{PLH}	Propagation Delay Bus to Bus	5.0	3.0	8.5	11.0	2.5	12.0	ns	3–5
t_{PHL}	Propagation Delay Bus to Bus	5.0	2.5	8.5	11.0	2.0	12.0	ns	3–5
t_{PLH}	Propagation Delay SBA or SAB to A_n or B_n (w/A_n or B_n HIGH or LOW)	5.0	3.0	9.5	12.0	2.5	13.0	ns	3–6
t_{PHL}	Propagation Delay SBA or SAB to A_n or B_n (w/A_n or B_n HIGH or LOW)	5.0	3.0	9.5	12.0	2.5	13.0	ns	3–6
t_{PZH}	Enable Time $\overline{G}$ to A_n or B_n	5.0	2.0	9.0	11.0	1.5	12.0	ns	3–7
t_{PZL}	Enable Time $\overline{G}$ to A_n or B_n	5.0	3.5	9.0	11.0	3.0	12.0	ns	3–8
t_{PHZ}	Disable Time $\overline{G}$ to A_n or B_n	5.0	5.0	10.5	13.0	4.5	14.5	ns	3–7
t_{PLZ}	Disable Time $\overline{G}$ to A_n or B_n	5.0	3.5	10.0	12.5	3.0	14.0	ns	3–8
t_{PZH}	Enable Time DIR to A_n or B_n	5.0	2.0	6.5	12.5	1.5	13.5	ns	3–7
t_{PZL}	Enable Time DIR to A_n or B_n	5.0	3.5	6.5	12.5	3.0	13.5	ns	3–8
t_{PHZ}	Disable Time DIR to A_n or B_n	5.0	5.0	8.5	12.5	4.5	13.5	ns	3–7
t_{PLZ}	Disable Time DIR to A_n or B_n	5.0	3.5	8.5	12.5	3.0	13.5	ns	3–8

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

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AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C C_L = 50 pF		74ACT T_A = −40°C to +85°C C_L = 50 pF	Unit	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW Bus to Clock	5.0	–	7.0	8.0	ns	3–9
t_h	Hold Time, HIGH or LOW Bus to Clock	5.0	–	2.5	2.5	ns	3–9
t_w	Clock Pulse Width HIGH or LOW	5.0	–	7.0	8.0	ns	3–6

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
$C_{I/O}$	Input/Output Capacitance	15	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	60	pF	V_{CC} = 5.0 V

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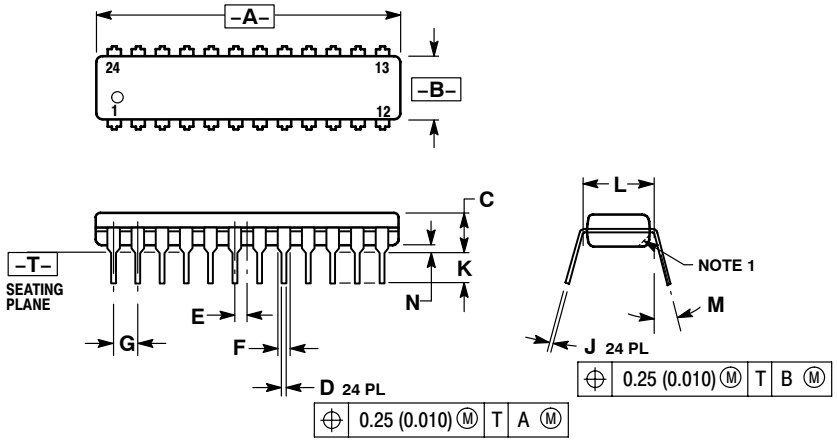
PACKAGE DIMENSIONS

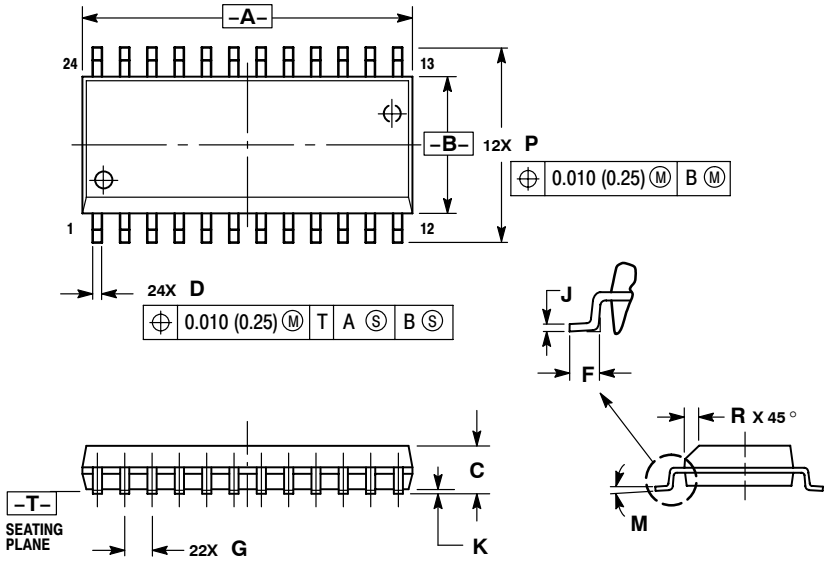
PDIP−24
N SUFFIX
24 PIN PLASTIC DIP PACKAGE
CASE 724−03
ISSUE D



NOTES:
1. CHAMFERED CONTOUR OPTIONAL.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.230	1.265	31.25	32.13
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.020	0.38	0.51
E	0.050 BSC		1.27 BSC	
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
J	0.007	0.012	0.18	0.30
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

SO−24
DW SUFFIX
24 PIN PLASTIC SOIC PACKAGE
CASE 751E−04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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Notes

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