P2042A

LCD Panel EMI Reduction IC

Product Description

The P2042A is a versatile spread spectrum frequency modulator designed specifically for digital flat panel applications. The P2042A reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of down stream clock and data dependent signals. The P2042A allows significant system cost savings by reducing the number of circuit board layers, ferrite beads, shielding, and other passive components that are traditionally required to pass EMI regulations.

The P2042A uses the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all digital method.

The P2042A modulates the output of a single PLL in order to "spread" the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal's bandwidth is called 'spread spectrum clock generation'.

Applications

The P2042A is targeted towards digital flat panel applications for notebook PCs, palm−size PCs, office automation equipments, and LCD monitors.

Features

- FCC Approved Method of EMI Attenuation
- Provides up to 15 dB of EMI Suppression
- Generates a Low EMI Spread Spectrum Clock of the Input Frequency
- Input/Output Frequency Range: 30 MHz to 110 MHz
- Optimized for 32.5 MHz, 54 MHz, 65 MHz and 108 MHz Pixel Clock Frequencies
- Internal Loop Filter Minimizes External Components and Board Space
- Eight Selectable High Spread Ranges up to ±2%
- SSON# Control Pin for Spread Spectrum Enable and Disable Options
- Low Cycle−to−Cycle Jitter
- 3.3 V ± 0.3 V Operating Range
- Low Power CMOS Design
- Supports Most Mobile Graphic Accelerator and LCD Timing Controller Specifications
- Available in 8−pin TSSOP Package
- These are Pb−Free Devices

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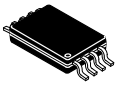
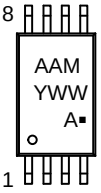


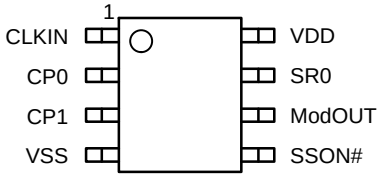
TSSOP−8
T SUFFIX
CASE 948J

MARKING DIAGRAM



AAM = Specific Device Code
Y = Year
WW = Work Week
A = Assembly Location
▪ = Pb−Free Package

PIN CONFIGURATION



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

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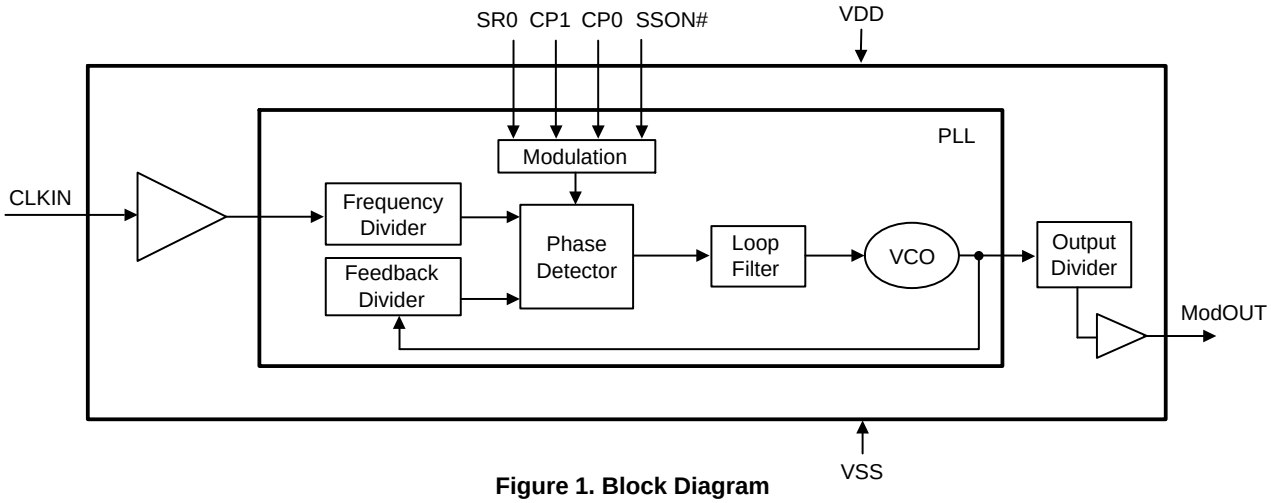

Figure 1. Block Diagram

PIN CONFIGURATION

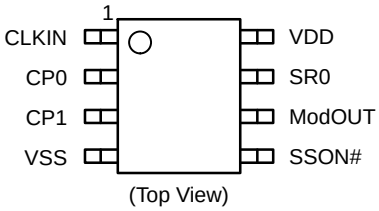

Table 1. PIN DESCRIPTION

Pin#	Pin Name	Type	Description
1	CLKIN	I	External reference frequency input. Connect to externally generated reference signal.
2	CP0	I	Digital logic input used to select Spreading Range. This pin has an internal pull−up resistor. Refer to *Modulation Selection* Table.
3	CP1	I	Digital logic input used to select Spreading Range. This pin has an internal pull−up resistor. Refer to *Modulation Selection* Table.
4	VSS	P	Ground to entire chip. Connect to system ground.
5	SSON#	I	Digital logic input used to enable Spread Spectrum function (Active LOW). Spread Spectrum function enabled when LOW, disabled when HIGH. This pin has an internal pull−low resistor.
6	ModOUT	O	Spread spectrum clock output.
7	SR0	I	Digital logic input used to select Spreading Range. This pin has an internal pull−up resistor. Refer to *Modulation Selection* Table.
8	VDD	P	Power supply for the entire chip

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Table 2. MODULATION SELECTION

CP0	CP1	SR0	Spreading Range (±%)					Modulation Rate (KHz)
			32.5 MHz	54 MHz	65 MHz	81 MHz	108 MHz	
0	0	0	1.75	1.53	1.41	1.27	1.10	(FIN /40) * 62.89 KHz
0	0	1	1.89	1.70	1.55	1.40	1.20	
0	1	0	1.39	1.20	1.10	1.00	0.90	
0	1	1	2.10	1.85	1.70	1.55	1.35	
1	0	0	0.74	0.60	0.57	0.52	0.45	
1	0	1	1.10	0.93	0.86	0.77	0.68	
1	1	0	0.32	0.30	0.28	0.26	0.23	
1	1	1	0.58	0.50	0.45	0.40	0.36	

Spread Spectrum Selection

The *Modulation Selection* Table 2 defines the possible spread spectrum options. The optimal setting should minimize system EMI to the fullest without affecting system performance. The spreading is described as a percentage deviation of the center frequency. (Note: The center frequency is the frequency of the external reference input on CLKIN, pin1).

For example, P2042A is designed for high−resolution, flat panel applications and is able to support an XGA (1024 x 768) flat panel operating at 65 MHz (FIN) clock speed. A spreading selection of CP0 = 0, CP1 = 1 and SR0 = 0 provides a percentage deviation of ±1.00% from F_{IN}. This results in the frequency on ModOUT being swept from 65.65 to 64.35 MHz at a modulation rate of 102.19 KHz. Refer to *Modulation Selection* Table 2. The example in the following illustration is a common EMI reduction method for a notebook LCD panel and has already been implemented by most of the leading OEM and mobile graphic accelerator manufacturers.

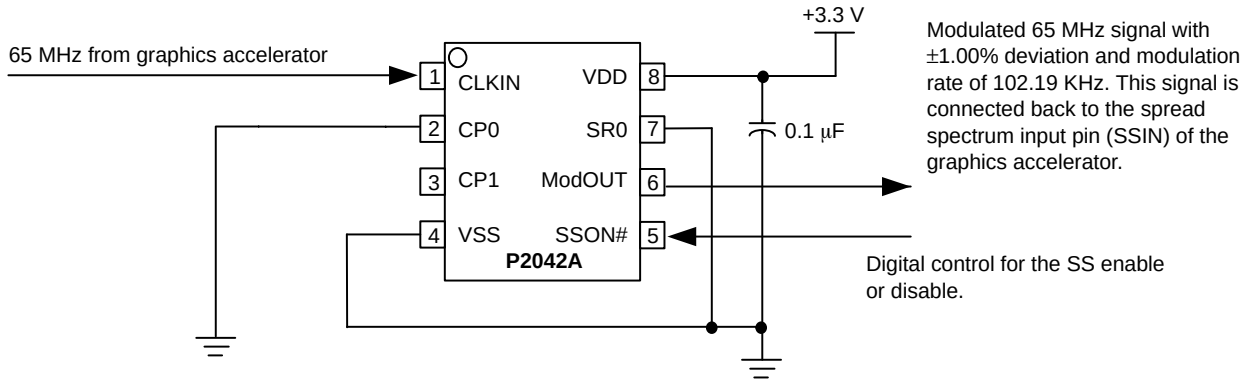

Figure 2. Application Schematic for Mobile LCD Graphics Controllers

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Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
VDD, V_{IN}	Voltage on any pin with respect to Ground	−0.5 to +4.6	V
T_{STG}	Storage Temperature Range	−65 to +125	°C
T_A	Operating Temperature Range	0 to +85	°C
T_{sol}	Wave Solder	265	°C
T_J	Junction Temperature	150	°C
θ_{JC}	Thermal Resistance (Junction−to−Case)	125	°C/W
T_{DV}	Static Discharge Voltage (As per JEDEC STD22− A114−B)	2	KV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 4. DC ELECTRICAL CHARACTERISTICS (T_A = 0°C to +85°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input low voltage	VSS−0.3		0.8	V
V_{IH}	Input high voltage	2.0		VDD+0.3	V
I_{IL}	Input low current (pull−up resistor on inputs CP0, CP1 and SR0)			−50	μA
I_{IH}	Input high current (pull−down resistor on input SSON#)			50	μA
V_{OL}	Output low voltage (V_{DD} = 3.3 V, I_{OL} = 8 mA)			0.4	V
V_{OH}	Output high voltage (V_{DD} = 3.3 V, I_{OL} = 8 mA)	2.5			V
I_{DD}	Static supply current standby mode (CLKIN pulled LOW)			300	μA
I_{CC}	Dynamic supply current (3.3 V and 10 pF loading)	6.0	15	22	mA
V_{DD}	Operating voltage	3.0	3.3	3.6	V
t_{ON}	Power−up time (first locked cycle after power up)			3.0	ms
Z_{OUT}	Clock output impedance		35		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 5. AC ELECTRICAL CHARACTERISTICS (T_A = 0°C to +85°C)

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input frequency	30	74	110	MHz
f_{OUT}	Output frequency	30	74	110	MHz
t_{LH} (Note 1)	Output rise time (measured at 0.8 V to 2.0 V)	1.1	1.5	2.0	ns
t_{HL} (Note 1)	Output fall time (measured at 2.0 V to 0.8 V)	0.8	1.2	1.8	ns
t_{JC}	Jitter (cycle−to−cycle) <50 MHz Jitter (cycle−to−cycle) ≥50 MHz			±250 ±200	ps
t_D	Output duty cycle	45	50	55	%

1. t_{LH} and t_{HL} are measured into a capacitive load of 10 pF.

Table 6. ORDERING INFORMATION

Part Number	Marking	Temperature	Package	Shipping†
P2042AF−08TR	AAM	0°C to +85°C	TSSOP−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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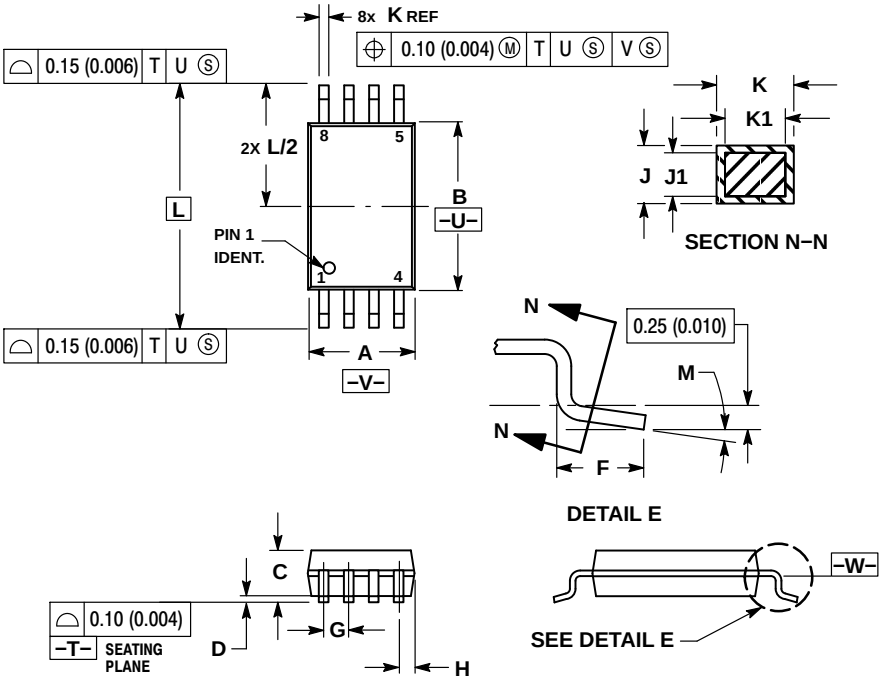
PACKAGE DIMENSIONS

TSSOP8
CASE 948J
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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