

DDR4 SDRAM RDIMM

Addendum

MTA9ASF2G72PZ – 16GB

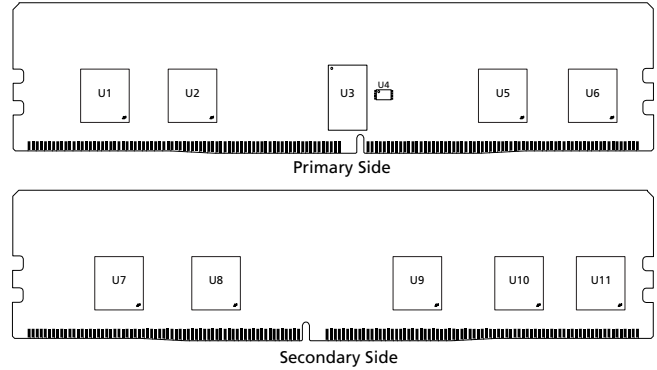
Introduction

Information provided here is in addition to or supersedes information provided in the Micron DDR4 RDIMM Core data sheet.

Features

- DDR4 functionality and operations supported as defined in the component data sheet
- Features and specifications supported in the Micron DDR4 RDIMM core data sheet
- 288-pin, registered dual in-line memory module (RDIMM)
- Fast data transfer rate: PC4-2933, PC4-3200
- 16GB (2 Gig x 72)
- Supports ECC error detection and correction
- Data bus inversion (DBI) for data bus
- Single-rank
- 16 internal banks; 4 groups of 4 banks each

Figure 1: 288-Pin RDIMM (R/C-D1)



Options

- Operating temperature
 - Commercial ($0^{\circ}\text{C} \leq T_{\text{OPER}} \leq +95^{\circ}\text{C}$)
- Package
 - 288-pin DIMM (halogen-free)
- Frequency/CAS latency
 - 0.625ns @ CL = 22 (DDR4-3200)
 - 0.682ns @ CL = 21 (DDR4-2933)

Marking

None
Z
-3G2
-2G9

Table 1: Addressing

Parameter	16GB
Row address	128K A[16:0]
Column address	1K A[9:0]
Device bank group address	4 BG[1:0]
Device bank address per group	4 BA[1:0]
Device configuration	16Gb (2 Gig x 8), 16 banks
Module rank address	1 CS0_n

Table 2: Part Numbers and Timing Parameters – 16GB ModulesBase device: MT40A2G8,¹ 16Gb DDR4 SDRAM

Part Number ²	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-nRCD-nRP)
MTA9ASF2G72PZ-3G2__	16GB	2 Gig x 72	25.6 GB/s	0.625ns/3200 MT/s	22-22-22
MTA9ASF2G72PZ-2G9__	16GB	2 Gig x 72	23.47 GB/s	0.682ns/2933 MT/s	21-21-21

- Notes:
1. The data sheet for the base device can be found on micron.com.
 2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MTA9ASF2G72PZ-3G2B1.

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DQ Map

Table 3: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	10	23	U2	0	26	45
	1	9	161		1	25	183
	2	11	168		2	27	190
	3	8	16		3	24	38
	4	15	166		4	31	188
	5	12	14		5	28	36
	6	14	21		6	30	43
	7	13	159		7	29	181
U5	0	42	115	U6	0	58	137
	1	41	253		1	57	275
	2	43	260		2	59	282
	3	40	108		3	56	130
	4	47	258		4	63	280
	5	44	106		5	60	128
	6	46	113		6	62	135
	7	45	251		7	61	273
U7	0	52	117	U8	0	36	95
	1	54	124		1	38	102
	2	53	262		2	37	240
	3	55	267		3	39	247
	4	48	119		4	32	97
	5	51	271		5	35	249
	6	49	264		6	33	242
	7	50	126		7	34	104
U9	0	CB4	47	U10	0	20	25
	1	CB6	54		1	22	32
	2	CB5	192		2	21	170
	3	CB7	199		3	23	177
	4	CB0	49		4	16	27
	5	CB3	201		5	19	179
	6	CB1	194		6	17	172
	7	CB2	56		7	18	34

Table 3: Component-to-Module DQ Map (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U11	0	4	1				
	1	6	10				
	2	5	148				
	3	7	155				
	4	0	5				
	5	3	157				
	6	1	150				
	7	2	12				

I_{DD} Specifications

Table 4: DDR4 I_{DD} Specifications and Conditions – 16GB (Die Revision E)

Values are for the MT40A2G8 DDR4 SDRAM only and are computed from values specified in the 16Gb (2 Gig x 8) component data sheet

Parameter	Symbol	3200	2933	Units
One bank ACTIVATE-PRECHARGE current	I _{DD0}	540	531	mA
One bank ACTIVATE-PRECHARGE, word line boost, I _{pp} current	I _{PP0}	27	27	mA
One bank ACTIVATE-READ-PRECHARGE current	I _{DD1}	639	630	mA
Precharge standby current	I _{DD2N}	405	396	mA
Precharge standby ODT current	I _{DD2NT}	459	450	mA
Precharge power-down current	I _{DD2P}	342	342	mA
Precharge quiet standby current	I _{DD2Q}	378	378	mA
Active standby current	I _{DD3N}	549	540	mA
Active standby I _{pp} current	I _{PP3N}	18	18	mA
Active power-down current	I _{DD3P}	450	441	mA
Burst read current	I _{DD4R}	1458	1386	mA
Burst write current	I _{DD4W}	1152	1107	mA
Burst refresh current (1 x REF)	I _{DD5R}	612	612	mA
Burst refresh I _{pp} current (1 x REF)	I _{PP5R}	36	36	mA
Self refresh current: Normal temperature range (0°C to +85°C)	I _{DD6N}	477	477	mA
Self refresh current: Extended temperature range (0°C to +95°C)	I _{DD6E}	1017	1017	mA
Self refresh current: Reduced temperature range (0°C to +45°C)	I _{DD6R}	180	180	mA
Auto self refresh current (25°C)	I _{DD6A}	99	99	mA
Auto self refresh current (45°C)	I _{DD6A}	180	180	mA
Auto self refresh current (75°C)	I _{DD6A}	459	459	mA
Auto self refresh current (95°C)	I _{DD6A}	1017	1017	mA
Auto self refresh I _{pp} current	I _{PP6X}	54	54	mA
Bank interleave read current	I _{DD7}	1665	1647	mA
Bank interleave read I _{pp} current	I _{PP7}	72	72	mA
Maximum power-down current	I _{DD8}	324	324	mA

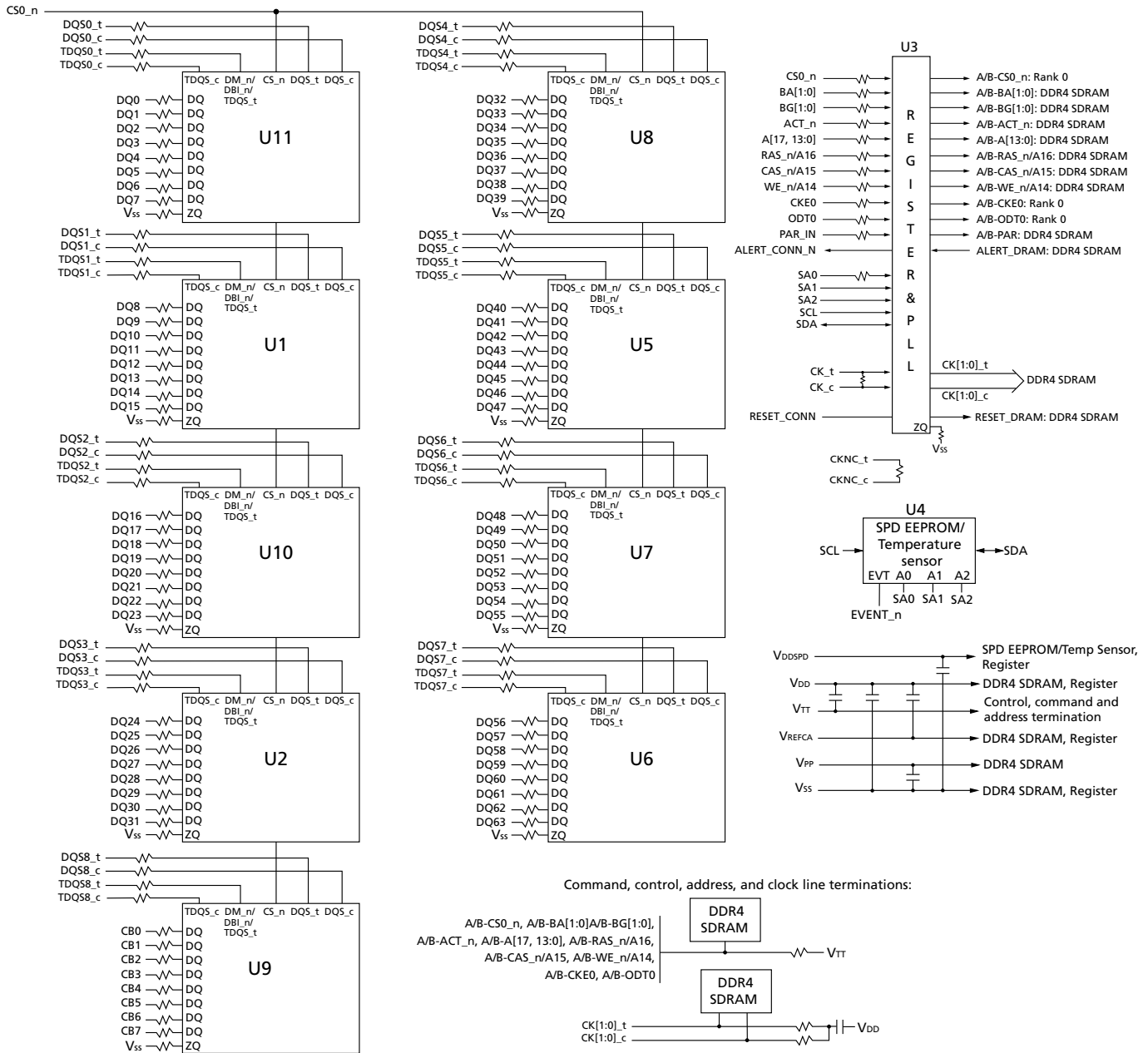
Table 5: DDR4 I_{DD} Specifications and Conditions – 16GB (Die Revision B)

Values are for the MT40A2G8 DDR4 SDRAM only and are computed from values specified in the 16Gb (2 Gig x 8) component data sheet

Parameter	Symbol	3200	2933	Units
One bank ACTIVATE-PRECHARGE current	I _{DD0}	567	558	mA
One bank ACTIVATE-PRECHARGE, word line boost, I _{pp} current	I _{PP0}	36	36	mA
One bank ACTIVATE-READ-PRECHARGE current	I _{DD1}	666	657	mA
Precharge standby current	I _{DD2N}	468	459	mA
Precharge standby ODT current	I _{DD2NT}	504	495	mA
Precharge power-down current	I _{DD2P}	387	387	mA
Precharge quiet standby current	I _{DD2Q}	423	423	mA
Active standby current	I _{DD3N}	720	711	mA
Active standby I _{pp} current	I _{PP3N}	27	27	mA
Active power-down current	I _{DD3P}	621	621	mA
Burst read current	I _{DD4R}	1818	1728	mA
Burst write current	I _{DD4W}	1647	1575	mA
Burst refresh current (1 x REF)	I _{DD5R}	711	702	mA
Burst refresh I _{pp} current (1 x REF)	I _{PP5R}	45	45	mA
Self refresh current: Normal temperature range (0°C to +85°C)	I _{DD6N}	603	603	mA
Self refresh current: Extended temperature range (0°C to +95°C)	I _{DD6E}	1089	1089	mA
Self refresh current: Reduced temperature range (0°C to +45°C)	I _{DD6R}	261	261	mA
Auto self refresh current (25°C)	I _{DD6A}	90	90	mA
Auto self refresh current (45°C)	I _{DD6A}	261	261	mA
Auto self refresh current (75°C)	I _{DD6A}	549	549	mA
Auto self refresh current (95°C)	I _{DD6A}	1089	1089	mA
Auto self refresh I _{pp} current	I _{PP6X}	99	99	mA
Bank interleave read current	I _{DD7}	1764	1737	mA
Bank interleave read I _{pp} current	I _{PP7}	90	90	mA
Maximum power-down current	I _{DD8}	360	360	mA

Functional Block Diagram

Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR4 component is connected to an external $240\Omega \pm 1\%$ resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.



16GB (x72, ECC, SR) 288-Pin DDR4 RDIMM Functional Block Diagram

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Although considered final, these specifications are subject to change, as further product development and data characterization some-
times occur.