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# MC100LVE111

## 3.3V ECL 1:9 Differential Clock Driver

The MC100LVE111 is a low skew 1−to−9 differential driver, designed with clock distribution in mind. The MC100LVE111's function and performance are similar to the popular MC100E111, with the added feature of low voltage operation. It accepts one signal input, which can be either differential or single−ended if the $V_{BB}$ output is used. The signal is fanned out to 9 identical differential outputs.

The LVE111 is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate to gate skew within a device, and empirical modeling is used to determine process control limits that ensure consistent $t_{pd}$ distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50 Ω, even if only one side is being used. In most applications, all nine differential pairs will be used and therefore terminated. In the case where fewer than nine pairs are used, it is necessary to terminate at least the output pairs on the same package side as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10−20 ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

The MC100LVE111, as with most other ECL devices, can be operated from a positive $V_{CC}$ supply in PECL mode. This allows the LVE111 to be used for high performance clock distribution in +3.3 V systems. Designers can take advantage of the LVE111's performance to distribute low skew clocks across the backplane or the board. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For systems incorporating GTL, parallel termination offers the lowest power by taking advantage of the 1.2 V supply as a terminating voltage. For more information on using PECL, designers should refer to Application Note AN1406/D.

The $V_{BB}$ pin, an internally generated voltage supply, is available to this device only. For single−ended input conditions, the unused differential input is connected to $V_{BB}$ as a switching reference voltage. $V_{BB}$ may also rebias AC coupled inputs. When used, decouple $V_{BB}$ and $V_{CC}$ via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, $V_{BB}$ should be left open.

### Features

- 200 ps Part−to−Part Skew
- 50 ps Output−to−Output Skew
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: $V_{CC}$ = 3.0 V to 3.8 V with $V_{EE}$ = 0 V
- NECL Mode Operating Range: $V_{CC}$ = 0 V with $V_{EE}$ = −3.0 V to −3.8 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at $V_{EE}$
- These are Pb−Free Devices*

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### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC100LVE111
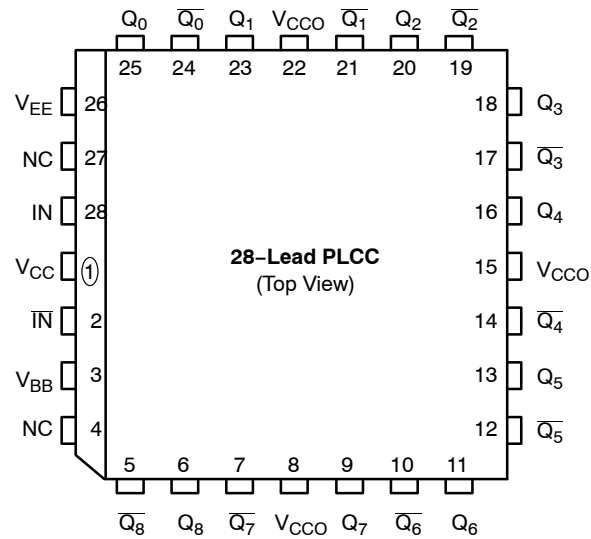


Warning: All $V_{CC}$, $V_{CCO}$, and $V_{EE}$ pins must be externally connected to Power Supply to guarantee proper operation.

**Figure 1. Pinout** (Top View) **and Logic Diagram**
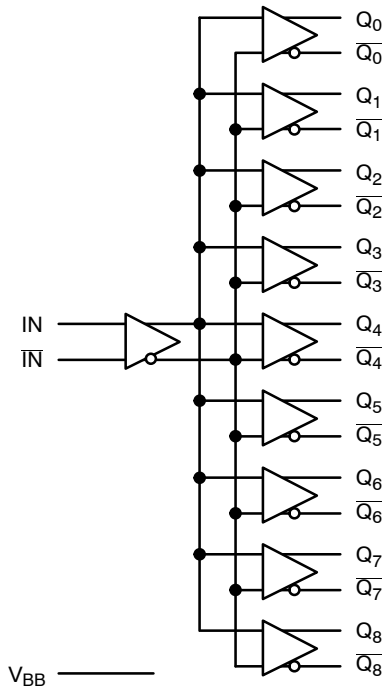


**Figure 2. Logic Symbol**

**Table 1. PIN DESCRIPTION**

| Pin | Function |
|---|---|
| IN, $\overline{IN}$ | ECL Differential Input Pair |
| $Q_0$, $\overline{Q_0}$–$Q_8$, $\overline{Q_8}$ | ECL Differential Outputs |
| $V_{BB}$ | Reference Voltage Output |
| $V_{CC}$, $V_{CCO}$ | Positive Supply |
| $V_{EE}$ | Negative Supply |
| NC | No Connect |

**Table 2. ATTRIBUTES**

| Characteristics | | Value |
|---|---|---|
| Internal Input Pulldown Resistor | | 75 kΩ |
| Internal Input Pullup Resistor | | N/A |
| ESD Protection | Human Body Model<br>Machine Model | > 2 kV<br>> 200 V |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | | Level 3 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V−0 @ 0.125 in |
| Transistor Count | | 250 |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | |

1.  For additional information, see Application Note AND8003/D.

**Table 3. MAXIMUM RATINGS**

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | PECL Mode Power Supply | $V_{EE} = 0$ V | | 8 to 0 | V |
| $V_{EE}$ | NECL Mode Power Supply | $V_{CC} = 0$ V | | −8 to 0 | V |
| $V_I$ | PECL Mode Input Voltage<br>NECL Mode Input Voltage | $V_{EE} = 0$ V<br>$V_{CC} = 0$ V | $V_I \leq V_{CC}$<br>$V_I \geq V_{EE}$ | 6 to 0<br>−6 to 0 | V<br>V |
| $I_{out}$ | Output Current | Continuous<br>Surge | | 50<br>100 | mA<br>mA |
| $I_{BB}$ | $V_{BB}$ Sink/Source | | | ± 0.5 | mA |
| $T_A$ | Operating Temperature Range | | | −40 to +85 | °C |
| $T_{stg}$ | Storage Temperature Range | | | −65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) | 0 lfpm<br>500 lfpm | PLCC−28<br>PLCC−28 | 63.5<br>43.5 | °C/W<br>°C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction−to−Case) | Standard Board | PLCC−28 | 22 to 26 ± 5% | °C/W |
| $T_{sol}$ | Wave Solder                Pb<br>Pb−Free | <2 to 3 sec @ 248°C<br><2 to 3 sec @ 260°C | | 265<br>265 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Table 4. LVPECL DC CHARACTERISTICS** $V_{CC}$ = 3.3 V; $V_{EE}$ = 0 V (Note 2)

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | | 55 | 66 | | 55 | 66 | | 65 | 78 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 3) | 2215 | 2345 | 2420 | 2275 | 2345 | 2420 | 2275 | 2345 | 2420 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 3) | 1490 | 1595 | 1680 | 1490 | 1595 | 1680 | 1490 | 1595 | 1680 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) | 2135 | | 2420 | 2135 | | 2420 | 2135 | | 2420 | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) | 1490 | | 1825 | 1490 | | 1825 | 1490 | | 1825 | mV |
| $V_{BB}$ | Output Voltage Reference | 1.92 | | 2.04 | 1.92 | | 2.04 | 1.92 | | 2.04 | V |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4) | 1.8 | | 2.9 | 1.8 | | 2.9 | 1.8 | | 2.9 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary ±0.3 V.
3. Outputs are terminated through a 50 Ω resistor to $V_{CC}$ − 2.0 V.
4. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, maximum varies 1:1 with $V_{CC}$. $V_{IHCMR}$ is defined as the range within which the $V_{IH}$ level may vary, with the device still meeting the propagation delay specification. The $V_{IL}$ level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to $V_{PP}$(min).

**Table 5. LVNECL DC CHARACTERISTICS** $V_{CC}$ = 0 V; $V_{EE}$ = −3.3 V (Note 5)

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | | 55 | 66 | | 55 | 66 | | 65 | 78 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 6) | −1085 | −955 | −880 | −1025 | −955 | −880 | −1025 | −955 | −880 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 6) | −1810 | −1705 | −1620 | −1810 | −1705 | −1620 | −1810 | −1705 | −1620 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) | −1165 | | −880 | −1165 | | −880 | −1165 | | −880 | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) | −1810 | | −1475 | −1810 | | −1475 | −1810 | | −1475 | mV |
| $V_{BB}$ | Output Voltage Reference | −1.38 | | −1.26 | −1.38 | | −1.26 | −1.38 | | −1.26 | V |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 7) | −1.5 | | −0.4 | −1.5 | | −0.4 | −1.5 | | −0.4 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary ±0.3 V.
6. Outputs are terminated through a 50 Ω resistor to $V_{CC}$ − 2.0 V.
7. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, maximum varies 1:1 with $V_{CC}$. $V_{IHCMR}$ is defined as the range within which the $V_{IH}$ level may vary, with the device still meeting the propagation delay specification. The $V_{IL}$ level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to $V_{PP}$(min).

**Table 6. AC CHARACTERISTICS** $V_{CC}$ = 3.3 V; $V_{EE}$ = 0 V or $V_{CC}$ = 0 V; $V_{EE}$ = −3.3 V (Note 8)

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{max}$ | Maximum Toggle Frequency | | > 1.5 | | | > 1.5 | | | > 1.5 | | GHz |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay to Output IN (Differential Configuration) (Note 9) sIN (Single−Ended) (Note 10) | 400 350 | | 650 700 | 440 390 | | 630 680 | 445 395 | | 635 685 | ps |
| $t_{skew}$ | Within−Device Skew (Note 11) Part−to−Part Skew (Differential Configuration) | | | 50 250 | | | 50 200 | | | 50 200 | ps |
| $t_{JITTER}$ | Cycle−to−Cycle Jitter | | 0.2 | < 1 | | 0.2 | < 1 | | 0.2 | < 1 | ps |
| $V_{PP}$ | Input Swing (Note 12) | 500 | | 1000 | 500 | | 1000 | 500 | | 1000 | mV |
| $t_r/t_f$ | Output Rise/Fall Time (20%−80%) | 200 | | 600 | 200 | | 600 | 200 | | 600 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

8. $V_{EE}$ can vary ±0.3 V.
9. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
10. The single−ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
11. The within−device skew is defined as the worst case difference between any two similar delay paths within a single device.
12. $V_{PP}$(min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The $V_{PP}$(min) is AC limited for the E111 as a differential input as low as 50 mV will still produce full ECL levels at the output.
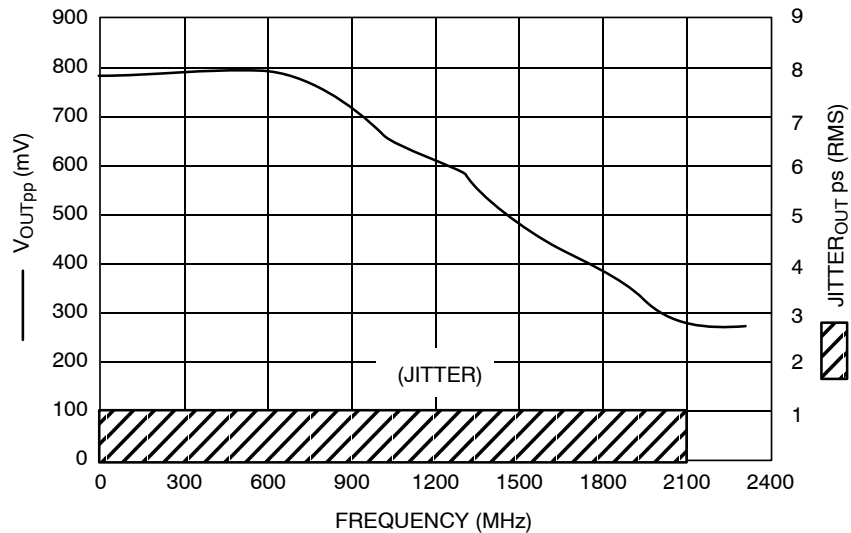

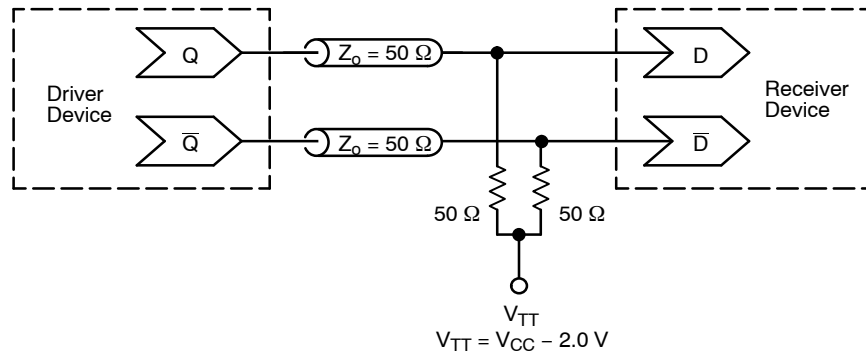
**Figure 3. $F_{max}$/Jitter**

# MC100LVE111



**Figure 4. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices.)**

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC100LVE111FNG | PLCC−28 (Pb−Free) | 37 Units / Rail |
| MC100LVE111FNR2G | PLCC−28 (Pb−Free) | 500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

### Resource Reference of Application Notes

**AN1405/D** – ECL Clock Distribution Techniques

**AN1406/D** – Designing with PECL (ECL at +5.0 V)

**AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit

**AN1504/D** – Metastability and the ECLinPS Family

**AN1568/D** – Interfacing Between LVDS and ECL

**AN1672/D** – The ECL Translator Guide

**AND8001/D** – Odd Number Counters Design

**AND8002/D** – Marking and Date Codes

**AND8020/D** – Termination of ECL Logic Devices

**AND8066/D** – Interfacing with ECLinPS

**AND8090/D** – AC Characteristics of ECL Devices
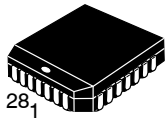
**28 LEAD PLCC**
CASE 776–02
ISSUE G

DATE 06 APR 2021

SCALE 1:1



VIEW D–D

VIEW S

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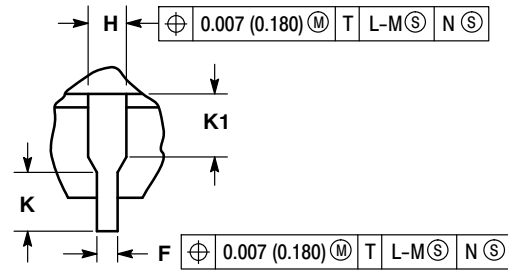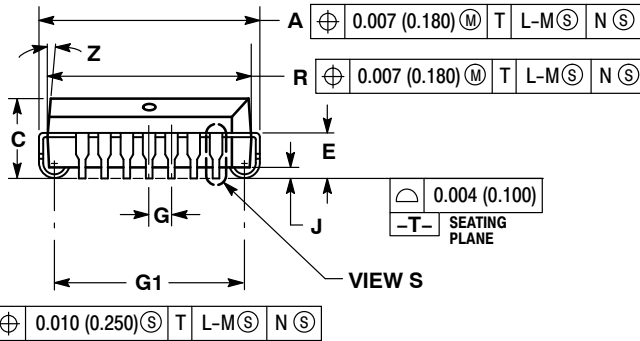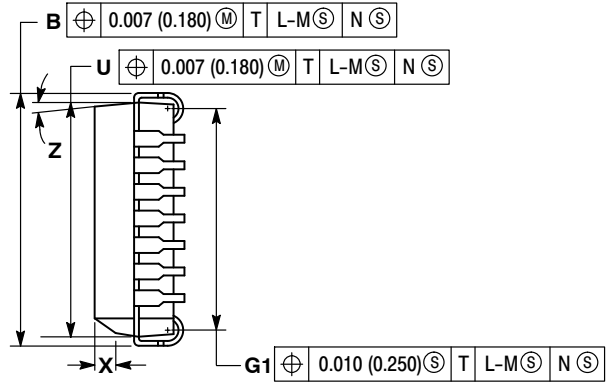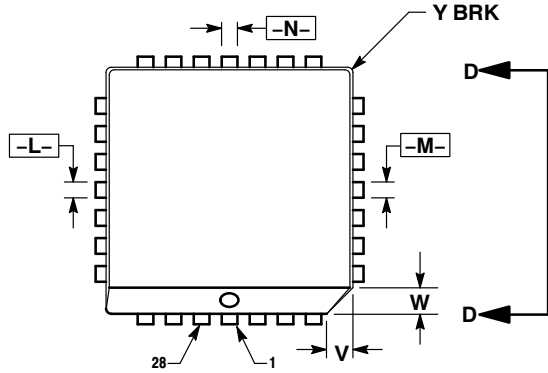
**NOTES:**
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

| DIM | INCHES MIN | INCHES MAX | MILLIMETERS MIN | MILLIMETERS MAX |
|-----|-----|-----|-----|-----|
| A | 0.485 | 0.495 | 12.32 | 12.57 |
| B | 0.485 | 0.495 | 12.32 | 12.57 |
| C | 0.165 | 0.180 | 4.20 | 4.57 |
| E | 0.090 | 0.110 | 2.29 | 2.79 |
| F | 0.013 | 0.021 | 0.33 | 0.53 |
| G | 0.050 BSC | | 1.27 BSC | |
| H | 0.026 | 0.032 | 0.66 | 0.81 |
| J | 0.020 | --- | 0.51 | --- |
| K | 0.025 | --- | 0.64 | --- |
| R | 0.450 | 0.456 | 11.43 | 11.58 |
| U | 0.450 | 0.456 | 11.43 | 11.58 |
| V | 0.042 | 0.048 | 1.07 | 1.21 |
| W | 0.042 | 0.048 | 1.07 | 1.21 |
| X | 0.042 | 0.056 | 1.07 | 1.42 |
| Y | --- | 0.020 | --- | 0.50 |
| Z | 2° | 10° | 2° | 10° |
| G1 | 0.410 | 0.430 | 10.42 | 10.92 |
| K1 | 0.040 | --- | 1.02 | --- |

**GENERIC MARKING DIAGRAM***

1 28

XXXXXXXXXXXX
XXXXXXXXXXXG
AWLYYWW
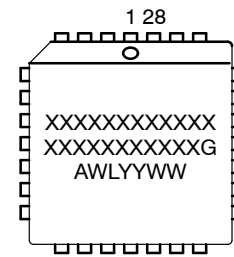
XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot " ▪", may or may not be present.

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|---|---|---|
| DESCRIPTION: | 28 LEAD PLCC | PAGE 1 OF 1 |

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