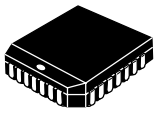
MC10H642, MC100H642

68030/040 PECL to TTL Clock Driver

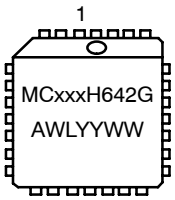
ON Semiconductor®

http://onsemi.com



PLCC−28
FN SUFFIX
CASE 776

MARKING DIAGRAM*



xxx	= 10 or 100
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

Description

The MC10H/100H642 generates the necessary clocks for the 68030, 68040 and similar microprocessors. It is guaranteed to meet the clock specifications required by the 68030 and 68040 in terms of part−to−part skew, within−part skew and also duty cycle skew.

The user has a choice of using either TTL or PECL (ECL referenced to +5.0 V) for the input clock. TTL clocks are typically used in present MPU systems. However, as clock speeds increase to 50 MHz and beyond, the inherent superiority of ECL (particularly differential ECL) as a means of clock signal distribution becomes increasingly evident. The H642 also uses differential PECL internally to achieve its superior skew characteristic.

The H642 includes divide−by−two and divide−by−four stages, both to achieve the necessary duty cycle skew and to generate MPU clocks as required. A typical 50 MHz processor application would use an input clock running at 100 MHz, thus obtaining output clocks at 50 MHz and 25 MHz (see Logic Diagram).

The 10H version is compatible with MECL 10H™ ECL logic levels, while the 100H version is compatible with 100K levels (referenced to +5.0 V).

Features

- Generates Clocks for 68030/040
- Meets 030/040 Skew Requirements
- TTL or PECL Input Clock
- Extra TTL and PECL Power/Ground Pins
- Asynchronous Reset
- Single +5.0 V Supply
- Pb−Free Packages are Available*

Function

Reset(R): LOW on RESET forces all Q outputs LOW.

Select(SEL): LOW selects the ECL input source (DE/$\overline{DE}$). HIGH selects the TTL input source (DT).

The H642 also contains circuitry to force a stable input state of the ECL differential input pair, should both sides be left open. In this Case, the DE side of the input is pulled LOW, and $\overline{DE}$ goes HIGH.

Power Up: The device is designed to have positive edges of the ÷2 and ÷4 outputs synchronized at Power Up.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

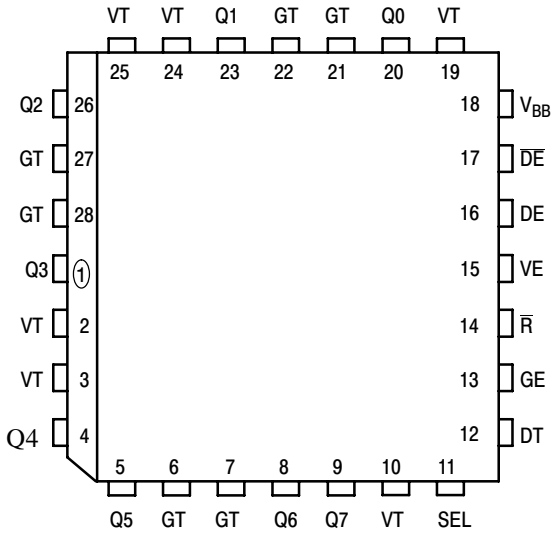


Figure 1. Pinout: PLCC−28
(Top View)

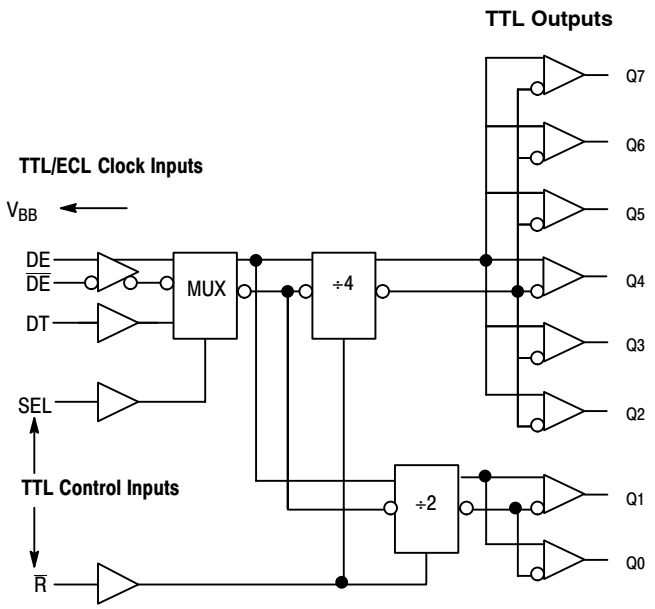


Figure 2. Logic Diagram

Table 1. PIN DESCRIPTION

Pin	Symbol	Description	Pin	Symbol	Description
1	Q3	Signal Output (TTL)**	15	VE	ECL V_{CC} (+5.0 V)
2	VT	TTL V_{CC} (+5.0 V)	16	DE	ECL Signal Input (Non−Inverting)
3	VT	TTL V_{CC} (+5.0 V)	17	$\overline{DE}$	ECL Signal Input (Inverting)
4	Q4	Signal Output (TTL)**	18	V_{BB}	V_{BB} Reference Output
5	Q5	Signal Output (TTL)**	19	VT	TTL V_{CC} (+5.0 V)
6	GT	TTL Ground (0 V)	20	Q0	Signal Output (TTL)*
7	GT	TTL Ground (0 V)	21	GT	TTL Ground (0 V)
8	Q6	Signal Output (TTL)**	22	GT	TTL Ground (0 V)
9	Q7	Signal Output (TTL)**	23	Q1	Signal Output (TTL)*
10	VT	TTL V_{CC} (+5.0 V)	24	VT	TTL V_{CC} (+5.0 V)
11	SEL	Input Select (TTL)	25	VT	TTL V_{CC} (+5.0 V)
12	DT	TTL Signal Input	26	Q2	Signal Output (TTL)**
13	GE	ECL Ground (0 V)	27	GT	TTL Ground (0 V)
14	R	Reset (TTL)	28	GT	TTL Ground (0 V)

* Divide by 2
**Divide by 4

Table 2. 10H PECL CHARACTERISTICS ($V_T = V_E = 5.0$ V ±5%)

Symbol	Characteristic	Condition	T_A = 0°C		T_A = 25°C		T_A = 85°C		Unit
			Min	Max	Min	Max	Min	Max	
I_{INH} I_{INL}	Input HIGH Current Input LOW Current		 0.5	255	 0.5	175	 0.5	175	μA
V_{IH} V_{IL}	Input HIGH Voltage (Note 1) Input LOW Voltage (Note 1)	V_{EE} = 5.0 V	3.83 3.05	4.16 3.52	3.87 3.05	4.19 3.52	3.94 3.05	4.28 3.555	V
V_{BB}	Output Reference Voltage (Note 1)		3.62	3.73	3.65	3.75	3.69	3.81	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. PECL LEVELS are referenced to V_{CC} and will vary 1:1 with the power supply. The VALUES shown are for V_{CC} = 5.0 V.

Table 3. 100H PECL CHARACTERISTICS ($V_T = V_E = 5.0$ V ±5%)

Symbol	Characteristic	Condition	T_A = 0°C		T_A = 25°C		T_A = 85°C		Unit
			Min	Max	Min	Max	Min	Max	
I_{INH} I_{INL}	Input HIGH Current Input LOW Current		 0.5	255	 0.5	175	 0.5	175	μA
V_{IH} V_{IL}	Input HIGH Voltage (Note 2) Input LOW Voltage (Note 2)	V_{EE} = 5.0 V	3.835 3.190	4.120 3.525	3.835 3.190	4.120 3.525	3.835 3.190	4.120 3.525	V
V_{BB}	Output Reference Voltage (Note 2)		3.620	3.740	3.620	3.740	3.620	3.740	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. PECL LEVELS are referenced to V_{CC} and will vary 1:1 with the power supply. The VALUES shown are for V_{CC} = 5.0 V.

Table 4. 10H/100H DC CHARACTERISTICS ($V_T = V_E = 5.0$ V ±5%)

Symbol	Characteristic		Condition	T_A = 0°C		T_A = 25°C		T_A = 85°C		Unit
				Min	Max	Min	Max	Min	Max	
I_{EE}	Power Supply Current	PECL	VE Pin		57		57		57	mA
I_{CCH}		TTL	Total All VT Pins		30		30		30	mA
I_{CCL}					30		30		30	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 5. 10H/100H TTL DC CHARACTERISTICS ($V_T = V_E = 5.0$ V ±5%)

Symbol	Characteristic	Condition	T_A = 0°C		T_A = 25°C		T_A = 85°C		Unit
			Min	Max	Min	Max	Min	Max	
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage		2.0	 0.8	2.0	 0.8	2.0	 0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V V_{IN} = 7.0 V		20 100		20 100		20 100	μA
I_{IL}	Input LOW Current	V_{IN} = 0.5 V		−0.6		−0.6		−0.6	mA
V_{OH}	Output HIGH Voltage	I_{OH} = −3.0 mA I_{OH} = −15 mA	2.5 2.0		2.5 2.0		2.5 2.0		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA		0.5		0.5		0.5	V
V_{IK}	Input Clamp Voltage	I_{IN} = −18 mA		−1.2		−1.2		−1.2	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0 V	−100	−225	−100	−225	−100	−225	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 6. AC CHARACTERISTICS ($V_T = V_E = 5.0$ V ±5%)

Symbol	Characteristic		Condition	T_A = 0°C		T_A = 25°C		T_A = 85°C		Unit
				Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay D to Output	Q2−Q7 C ECL C TTL	CL = 25 pF	 4.70 4.70	 5.70 5.70	 4.75 4.75	 5.75 5.75	 4.60 4.50	 5.60 5.50	ns
tskpp	Part−to−Part Skew				1.0		1.0		1.0	ns
tskwd*	Within−Device Skew				0.5		0.5		0.5	ns
t_{PLH}	Propagation Delay D to Output	Q0, Q1 C ECL C TTL	CL = 25 pF	 4.30 4.30	 5.30 5.30	 4.50 4.50	 5.50 5.50	 4.25 4.25	 5.25 5.25	ns
tskpp	Part−to−Part Skew	All Outputs	CL = 25 pF		2.0		2.0		2.0	ns
tskwd	Within−Device Skew		CL = 25 pF		1.0		1.0		1.0	ns
t_{PD}	Propagation Delay R to Output	All Outputs	CL = 25 pF	4.3	6.3	4.0	6.0	4.5	6.5	ns
t_R t_F	Output Rise/Fall Time 0.8 V to 2.0 V	All Outputs	CL = 25 pF		2.5 2.5		2.5 2.5		2.5 2.5	ns
f_{MAX}**	Maximum Input Frequency		CL = 25 pF	100		100		100		MHz
RPW	Reset Pulse Width			1.5		1.5		1.5		ns
RRT	Reset Recovery Time			1.25		1.25		1.25		ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

* Within−Device Skew defined as identical transactions on similar paths through a device.

**MAX Frequency is 135 MHz.

10/100H642 – DUTY CYCLE CONTROL

To maintain a duty cycle of ±5% at 50 MHz, limit the load capacitance and/or power supply variation as shown in Figures 1 and 2. For a ±2.5% duty cycle limit, see Figures 3 and 4. Figures 5 and 6 show duty cycle variation with temperature. Figure 7 shows typical TPD versus load. Figure 8 shows reset recovery time. Figure 9 shows output states after power up.

Best duty cycle control is obtained with a single μP load and minimum line length.

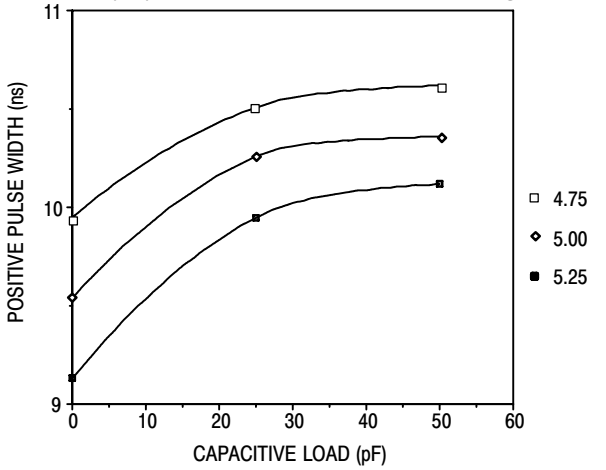


Figure 3. MC10H642 Positive PW versus Load @ ±5% V_{CC}, T_A = 25°C

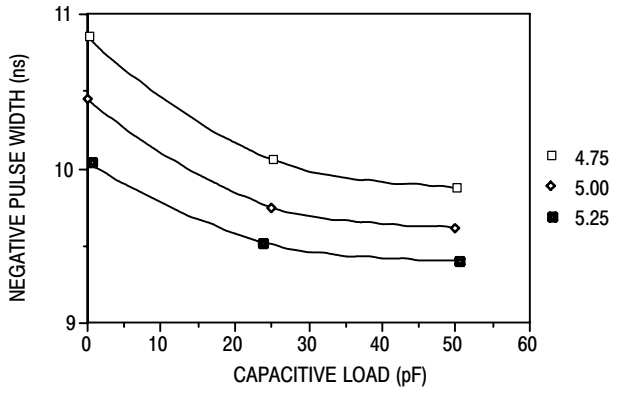


Figure 4. MC10H642 Negative PW versus Load @ ±5% V_{CC}, T_A = 25°C

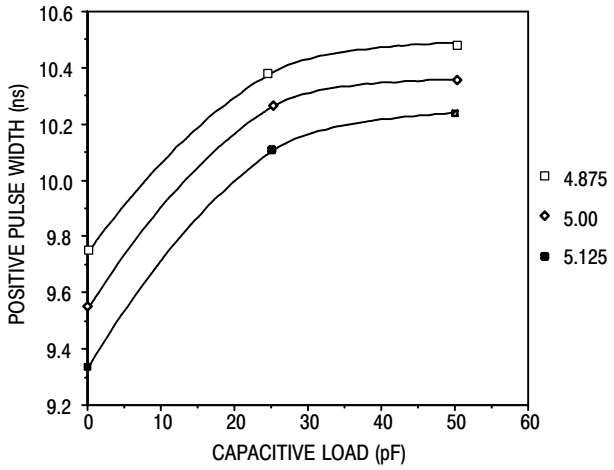


Figure 5. MC10H642 Positive PW versus Load @ ±2.5% V_{CC}, T_A = 25°C

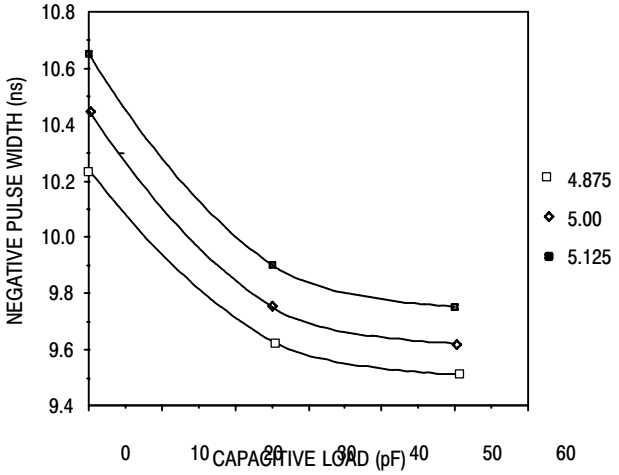


Figure 6. MC10H642 Negative PW versus Load @ ±2.5% V_{CC}, T_A = 25°C

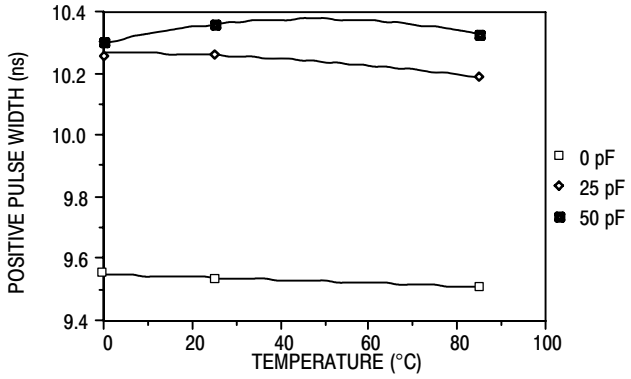


Figure 7. MC10H642 Positive PW versus Temperature, V_{CC} = 5.0 V

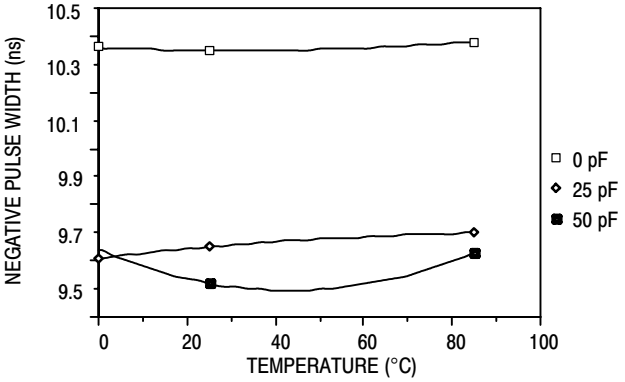


Figure 8. MC10H642 Negative PW versus Temperature, V_{CC} = 5.0 V

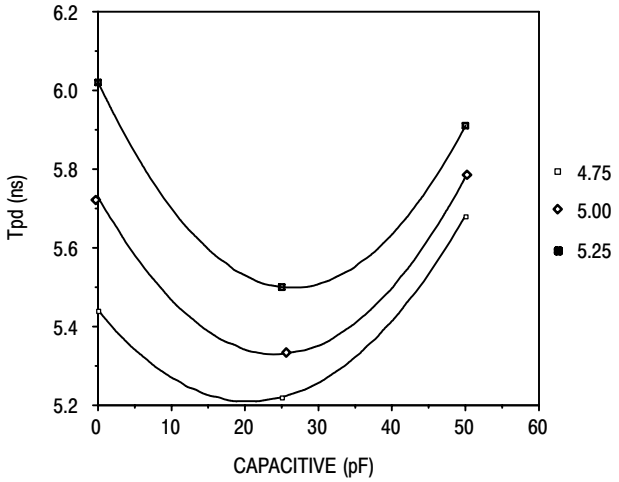


Figure 9. MC10H642 + Tpd versus Load, V_{CC} ±5%, T_A = 25°C (Overshoot at 50 MHz with no load makes graph non linear)

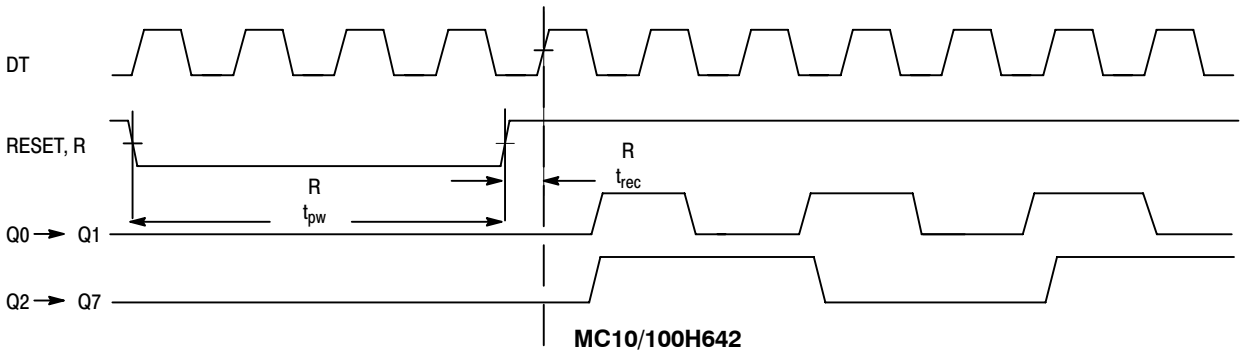


Figure 10. Clock Phase and Reset Recovery Time After Reset Pulse

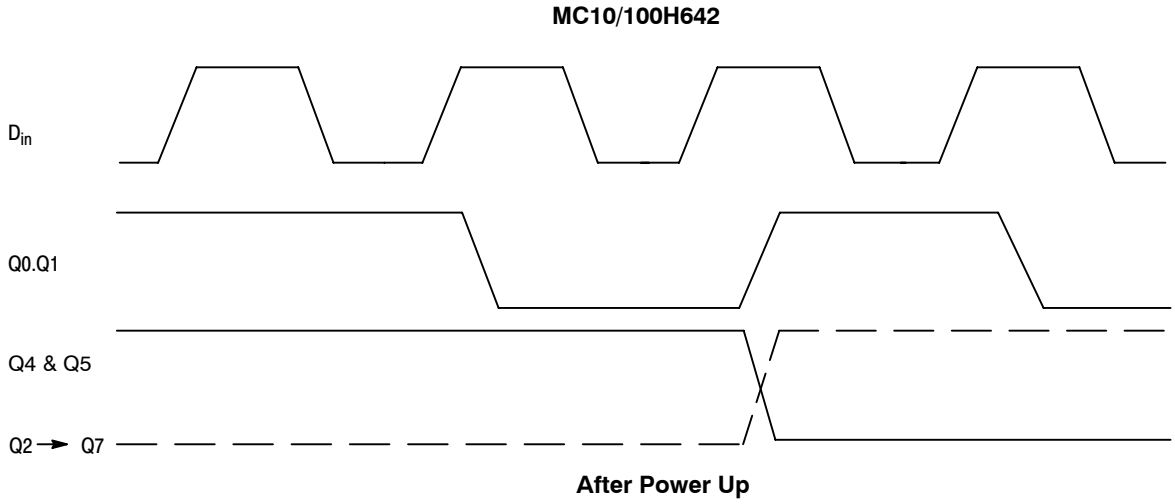


Figure 11. Q2 → Q7 will Synchronize with Pos Edges of D_{in} & Q0 → Q1 Outputs

Switching Circuit PECL:

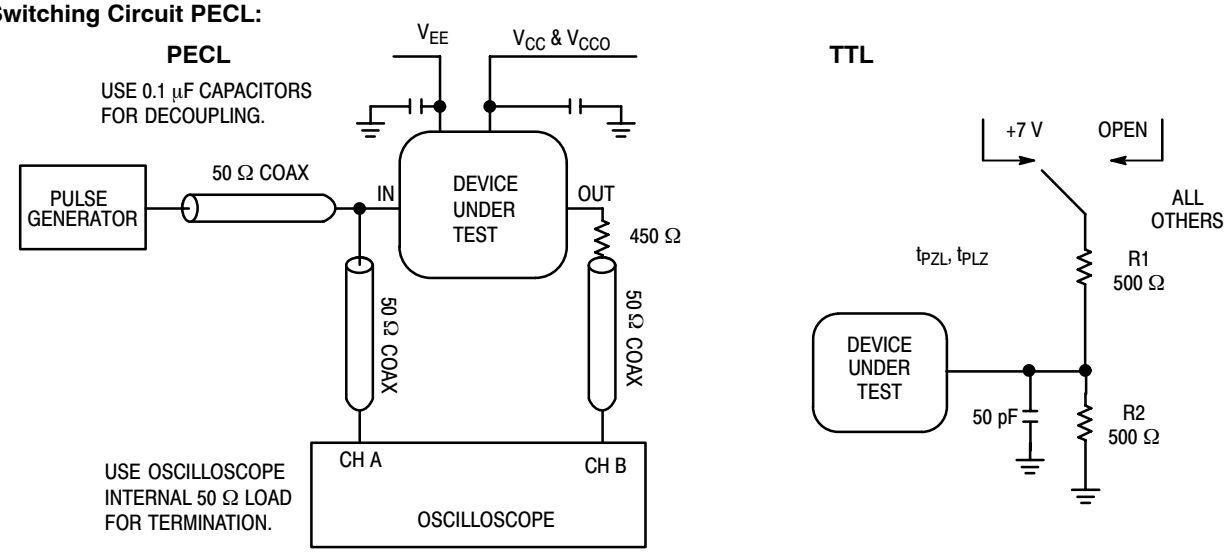


Figure 12. Switching Circuit and Waveforms

PECL/TTL

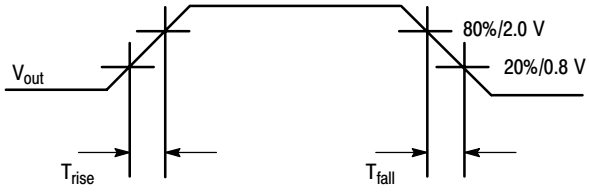


Figure 14. Waveforms: Rise and Fall Times

PECL/TTL

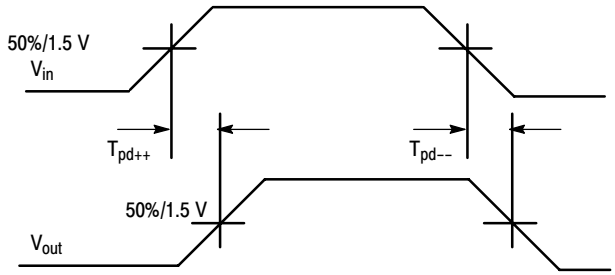


Figure 13. Propagation Delay — Single−Ended

ORDERING INFORMATION

Device	Package	Shipping†
MC10H642FN	PLCC−28	37 Units / Rail
MC10H642FNG	PLCC−28 (Pb−Free)	37 Units / Rail
MC10H642FNR2	PLCC−28	500 / Tape & Reel
MC10H642FNR2G	PLCC−28 (Pb−Free)	500 / Tape & Reel
MC100H642FN	PLCC−28	37 Units / Rail
MC100H642FNG	PLCC−28 (Pb−Free)	37 Units / Rail
MC100H642FNR2	PLCC−28	500 / Tape & Reel
MC100H642FNR2G	PLCC−28 (Pb−Free)	500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

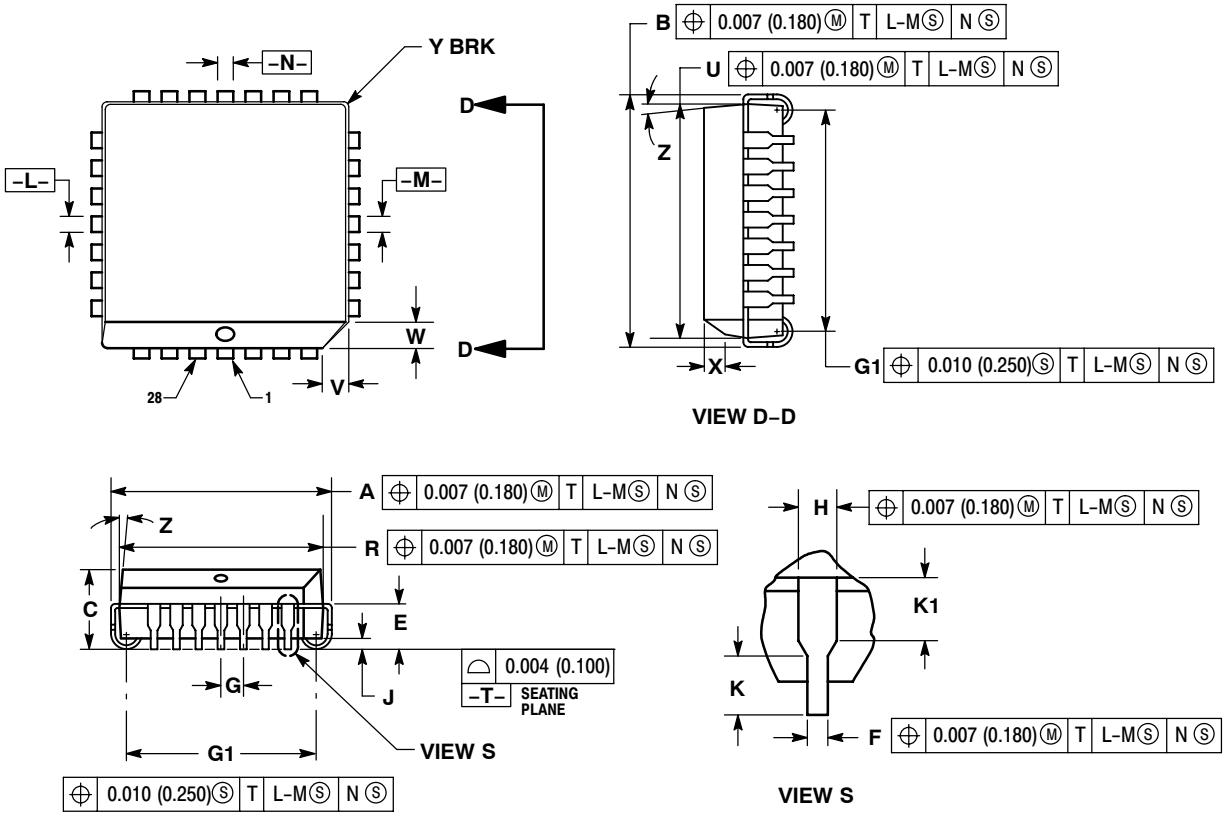
AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

PLCC−28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776−02
ISSUE E



NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

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MECL 10H is a trademark of Motorola, Inc.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

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