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74ALVCH245
Low Voltage Bidirectional Transceiver with Bushold

General Description

The ALVCH245 contains eight non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The T/$\overline{R}$ input determines the direction of data flow. The $\overline{OE}$ input disables both the A and B Ports by placing them in a high impedance state. The ALVCH245 data inputs include active bushold circuitry, eliminating the need for external pull-up resistors to hold unused or floating data inputs at a valid logic level.

The 74ALVCH245 is designed for low voltage (1.65V to 3.6V) V_{CC} applications.

The 74ALVCH245 is fabricated with an advanced CMOS technology to achieve high-speed operation while maintaining low CMOS power dissipation.

Features

■ 1.65V to 3.6V V_{CC} supply operation

■ Bushold on data inputs eliminates the need for external pull-up/pull-down resistors

■ t_{PD}
  3.6 ns max for 3.0V to 3.6V V_{CC}
  4.2 ns max for 2.3V to 2.7V V_{CC}
  6 ns max for 1.65V to 1.95V V_{CC}

■ Uses patented Quiet Series noise/EMI reduction circuitry

■ Latchup conforms to JEDEC JED78

■ ESD performance:
  Human body model > 2000V
  Machine model > 200V

Ordering Code:

Order Number	Package Number	Package Description
74ALVCH245WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ALVCH245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
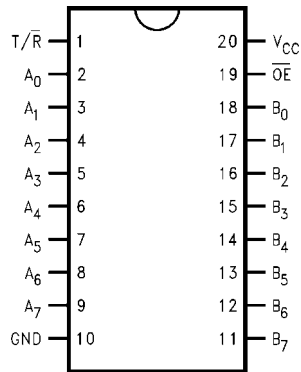
Logic Symbol
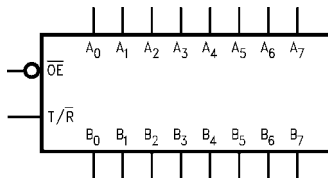
Pin Descriptions

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Bushold Inputs or 3-STATE Outputs
B_0–B_7	Side B Bushold Inputs or 3-STATE Outputs

Quiet Series™ is a trademark of Fairchild Semiconductor Corporation.

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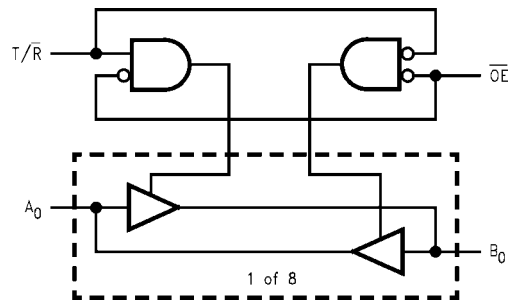
Connection Diagram

Pin			Pin
$T/\overline{R}$	1	20	V_{CC}
A_0	2	19	$\overline{OE}$
A_1	3	18	B_0
A_2	4	17	B_1
A_3	5	16	B_2
A_4	6	15	B_3
A_5	7	14	B_4
A_6	8	13	B_5
A_7	9	12	B_6
GND	10	11	B_7

Truth Table

Inputs		Outputs
$\overline{OE}$	$T/\overline{R}$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH Z State on A_0–A_7, B_0–B_7

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram

1 of 8

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage (V_I)	−0.5V to 4.6V
Output Voltage (V_O) (Note 2)	−0.5V to V_{CC} +0.5V
DC Input Diode Current (I_{IK})	
V_I < 0V	−50 mA
DC Output Diode Current (I_{OK})	
V_O < 0V	−50 mA
DC Output Source/Sink Current	
(I_{OH}/I_{OL})	±50 mA
DC V_{CC} or GND Current per	
Supply Pin (I_{CC} or GND)	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C

Recommended Operating Conditions (Note 3)

Power Supply	
Operating	1.65V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10 ns/V

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed, limited to 4.6V.

Note 3: Floating or unused control inputs must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		1.65 - 1.95	0.65 x V_{CC}		
			2.3 - 2.7	1.7		V
			2.7 - 3.6	2.0		
V_{IL}	LOW Level Input Voltage		1.65 - 1.95		0.35 x V_{CC}	
			2.3 - 2.7		0.7	V
			2.7 - 3.6		0.8	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	1.65 - 3.6	V_{CC} - 0.2		
		I_{OH} = −4 mA	1.65	1.2		
		I_{OH} = −6 mA	2.3	2.0		
		I_{OH} = −12 mA	2.3	1.7		V
			2.7	2.2		
			3.0	2.4		
		I_{OH} = −24 mA	3.0	2		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	1.65 - 3.6		0.2	
		I_{OL} = 4 mA	1.65		0.45	
		I_{OL} = 6 mA	2.3		0.4	
		I_{OL} = 12 mA	2.3		0.7	V
			2.7		0.4	
		I_{OL} = 24 mA	3.0			
I_I	Input Leakage Current	$0 \leq V_I \leq 3.6V$	3.6		±5.0	μA
$I_{I(HOLD)}$	Bushold Input Minimum Drive Hold Current	V_{IN} = 0.58V	1.65	25		
		V_{IN} = 1.07V	1.65	−25		
		V_{IN} = 0.7V	2.3	45		
		V_{IN} = 1.7V	2.3	−45		μA
		V_{IN} = 0.8V	3.0	75		
		V_{IN} = 2.0V	3.0	−75		
		$0 < V_O \leq 3.6V$	3.6		±500	
I_{OZ}	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$	3.6		±10	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND, I_O = 0	3.6		10	μA
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC}$ − 0.6V	3 - 3.6		750	μA

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AC Electrical Characteristics

		$T_A = -40°C$ to $+85°C$, $R_L = 500\Omega$								Units
Symbol	Parameter	$C_L = 50$ pF				$C_L = 30$ pF				
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 1.8V \pm 0.15V$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PHL}, t_{PLH}	Propagation Delay	1.3	3.6		4.2	1.0	3.7	1.5	6.0	ns
t_{PZL}, t_{PZH}	Output Enable Time	1.6	5.5		6.3	2.0	6.0	2.9	8.6	ns
t_{PLZ}, t_{PHZ}	Output Disable Time	1.7	5.5		5.3	0.8	4.8	1.5	8.0	ns

Capacitance

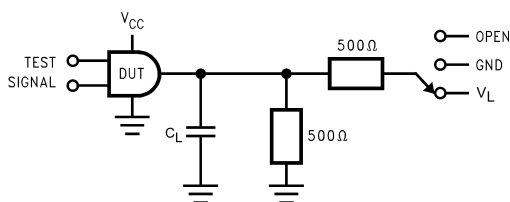| Symbol	Parameter	Conditions		$T_A = +25°C$		Units
				V_{CC}	Typical	
C_{IN}	Input Capacitance	Control	$V_I = 0V$ or V_{CC}	3.3	4.5	pF
$C_{I/O}$	Input/Output Capacitance	A or B Ports	$V_I = 0V$ or V_{CC}	3.3	12	pF
C_{PD}	Power Dissipation Capacitance	Outputs Enabled	$f = 10$ MHz, $C_L = 0$ pF	3.3	31	pF
				2.5	28	
				1.8	25	
		Outputs Disabled	$f = 10$ MHz, $C_L = 50$ pF	3.3	0	
				2.5	0	
				1.8	0	

AC Loading and Waveforms

FIGURE 1. AC Test Circuit

TABLE 1. Values for Figure 1

TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_L
t_{PZH}, t_{PHZ}	GND

TABLE 2. Variable Matrix
(Input Characteristics: f = 1MHz; t_r = t_f = 2ns; Z_0 = 50Ω)

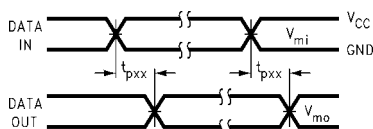| Symbol	V_{CC}			
	3.3V $\pm$ 0.3V	2.7V	2.5V $\pm$ 0.2V	1.8V $\pm$ 0.15V
V_{mi}	1.5V	1.5V	V_{CC}/2	V_{CC}/2
V_{mo}	1.5V	1.5V	V_{CC}/2	V_{CC}/2
V_x	V_{OL} + 0.3V	V_{OL} + 0.3V	V_{OL} + 0.15V	V_{OL} + 0.15V
V_y	V_{OH} − 0.3V	V_{OH} − 0.3V	V_{OH} − 0.15V	V_{OH} − 0.15V
V_L	6V	6V	V_{CC}*2	V_{CC}*2

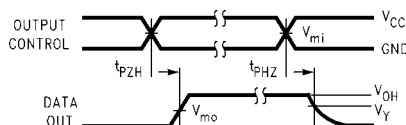**FIGURE 2. Waveform for Inverting and Non-inverting Functions**

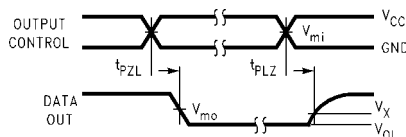**FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic**

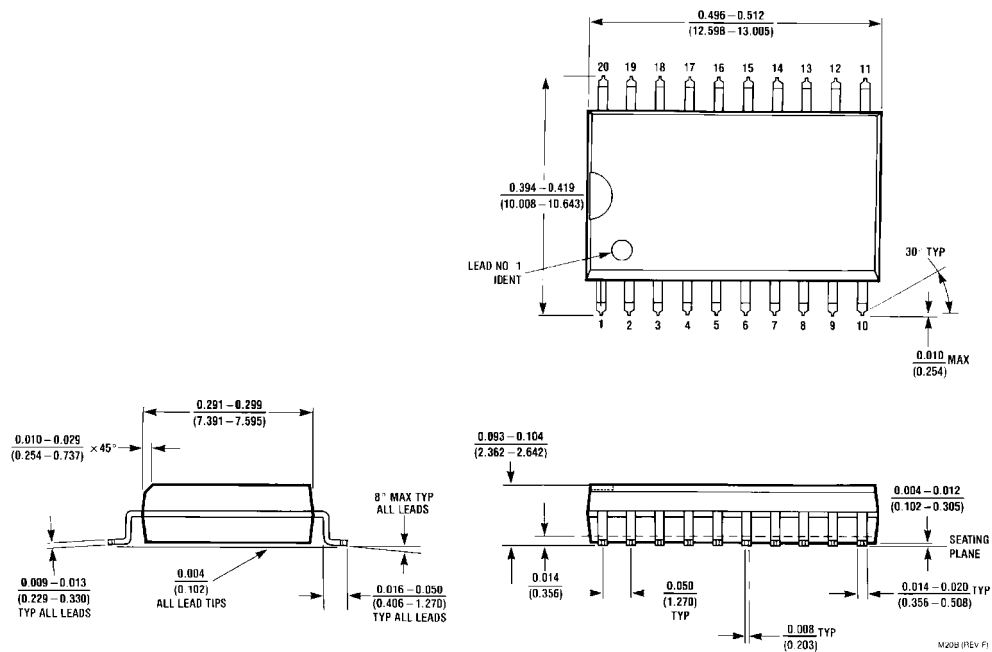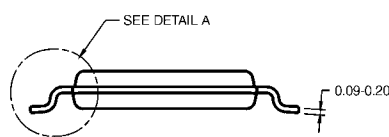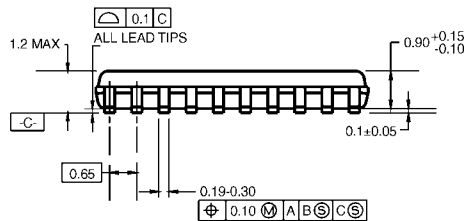**FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic**

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Physical Dimensions inches (millimeters) unless otherwise noted

20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

LAND PATTERN RECOMMENDATION
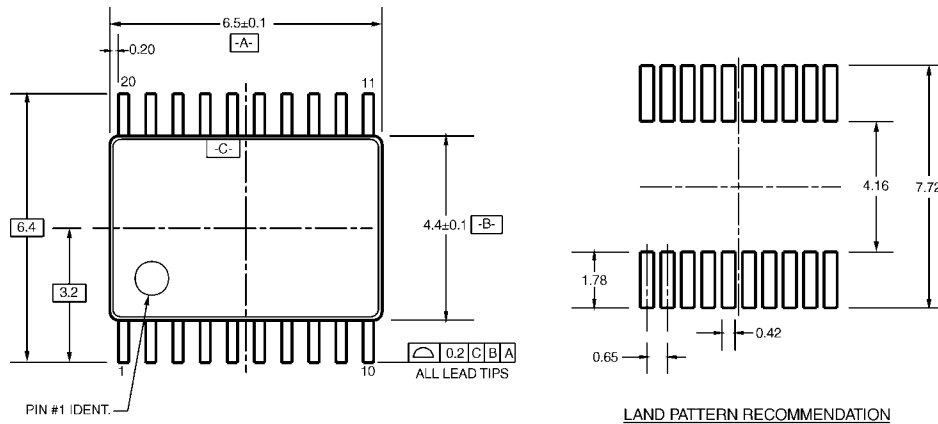
DIMENSIONS ARE IN MILLIMETERS

NOTES:
A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20RevD1

SEE DETAIL A

DETAIL A

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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