GDDR6X SGRAM

MT61K256M32

2 Channels x 256 Meg x 16 I/O, 2 Channels x 512 Meg x 8 I/O

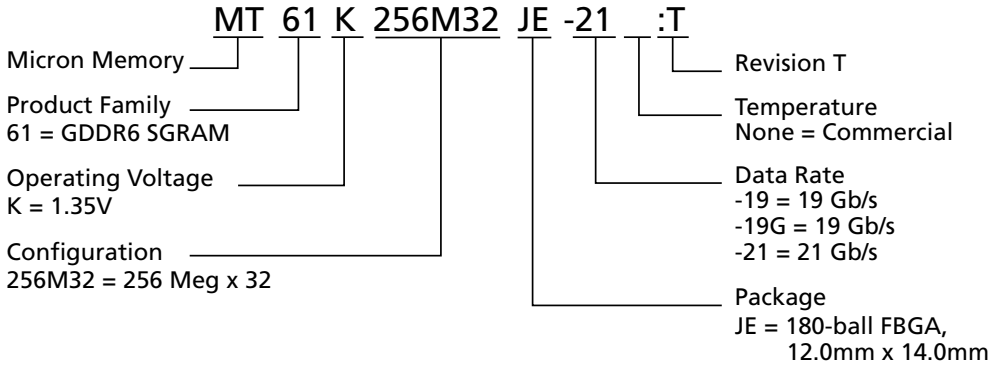
Features

- $V_{DD} = V_{DDQ}$ = 1.35V ±3% and 1.25V ±3%
- V_{PP} = 1.8V –3%/+6%
- Data rate:
  - 19 Gb/s (9.5 GBaud)
  - 21 Gb/s (10.5 GBaud)
- 2 separate independent channels (x16)
- x16/x8 mode configurations set at reset
- Single ended interfaces per channel for command/address (CA) and data
- Differential clock input CK_t/CK_c for CA per 2 channels
- One differential clock input WCK_t/WCK_c per channel for data (DQ, DBI, EDC)
- Double data rate (DDR) command/address (CK)
- Double data or symbol rate data (WCK)
- 16*n* prefetch architecture
- 16 internal banks
- 4 bank groups
- Programmable READ latency
- Programmable WRITE latency
- Write data mask function via CA bus with single and double byte mask granularity
- CA bus inversion (CABI)
- CA bus training via DQ/DBI/EDC signals
- WCK2CK clock training via EDC signals
- Data read and write training via read FIFO
- Read/write data transmission integrity secured by cyclic redundancy check
- Programmable CRC READ latency
- Programmable CRC WRITE latency
- Programmable EDC hold pattern for CDR
- RDQS mode on EDC pins
- Low power modes
- On-chip temperature sensor with read-out
- Auto precharge option for each burst access
- Auto refresh mode (32ms, 16k cycles)
- Temperature sensor controlled self refresh rate
- Hibernate self refresh mode with V_{DDQ} off option
- Digital ^{t}RAS lockout
- On-die termination (ODT) for all high-speed inputs
- Pseudo open drain (POD135 and POD125) compatible CA, CK, and WCK inputs
- PAM4 compatible data I/O (DQ, DBI, EDC)
- ODT and output driver strength auto calibration with external resistor ZQ pin (360Ω)
- Internal V_{REF} for data inputs
- Selectable external or internal V_{REF} for CA inputs
- Vendor ID for device identification
- IEEE 1149.1 compliant boundary scan
- 180-ball BGA package
- Lead-free (RoHS-compliant) and halogen-free packaging
- T_C = 0°C to +95°C/+105°C

Options[1]	Marking
• Organization	
– 256 Meg × 32 (words × bits)	256M32
• FBGA package	
– 180-ball (12.0mm × 14.0mm)	JE
• Timing – maximum data rate	
– 19 Gb/s (9.5 GBaud)	-19
– 19 Gb/s (9.5 GBaud)	-19G
– 21 Gb/s (10.5 GBaud)	-21
• Operating temperature	
– Commercial ($0°C \le T_C \le +95°C/+105°C$)	None
• Revision	:T

Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.

Figure 1: Part Numbering



FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on Micron's web site: http://www.micron.com.

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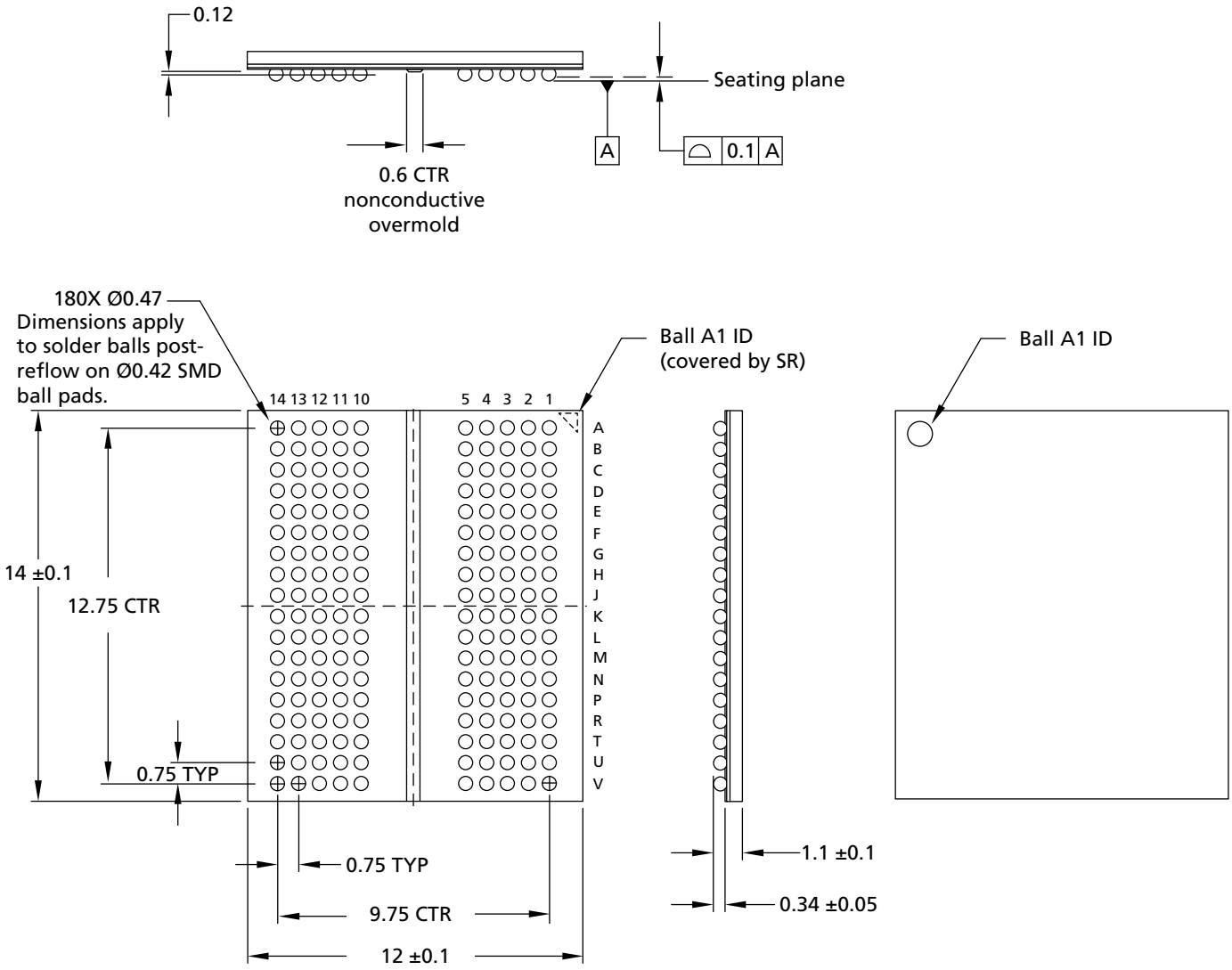
Package Dimensions

Figure 2: 180-Ball FBGA (JE)



Notes:
1. Package dimension specification is compliant to JC11 MO328 variation PBGA-B180[252]_I0p75-R12p0x14p0Z#-C0p525Z0p22.
2. All dimensions are in millimeters.
3. Solder ball material: SAC-Q (92.5% Sn, 4% Ag, 3% Bi, 0.5% Cu).

Functional Description

The GDDR6X SGRAM is a high-speed dynamic random-access memory designed for applications requiring highest bandwidth. It is internally configured as 16-bank memory and contains 8,589,934,592 bits.

The GDDR6X SGRAM's high-speed interface is optimized for point-to-point connections to a host controller. On-die termination (ODT) is provided for all high-speed interface signals to eliminate the need for termination resistors in the system.

GDDR6X uses a 16*n*-prefetch architecture. The device's architecture consists of two 16-bit-wide fully independent channels.

Read and write accesses consist of a total of 8 PAM4-encoded data words in PAM4 mode, and a total of 16 data words in RDQS mode.

Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ, WRITE (WOM), or masked WRITE (WDM, WSM) command. The row and bank address to be accessed is registered coincident with the ACTIVATE command. The address bits registered coincident with the READ, WRITE, or masked WRITE command are used to select the bank and the starting column location for the burst access.

Clocking

GDDR6X operates from a differential clock CK_t and CK_c. CK is common to both channels. Command and address (CA) are registered at every rising and falling CK edge. There are both single-cycle and multi-cycle commands. See Command Truth Table for details.

GDDR6X uses a free running differential forwarded clock (WCK_t/WCK_c) with both input and output data registered and driven respectively at both edges of the forwarded WCK.

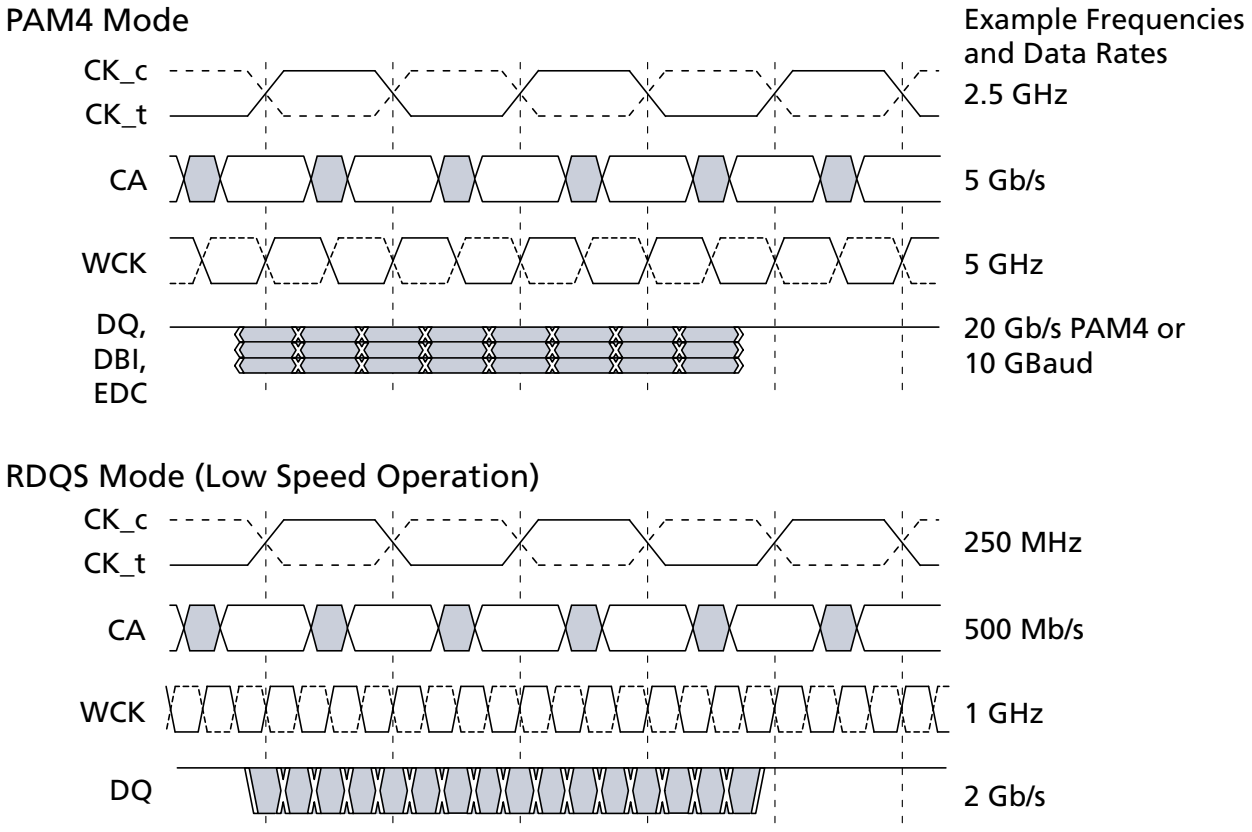
GDDR6X supports DDR operating modes for WCK frequency which differ in the DQ/DBI/EDC pin to WCK clock frequency ratio between PAM4 and RDQS mode. The figure below illustrates the difference between both modes.

This GDDR6X SGRAM supports WCK/word granularity which is equivalent to one WCK per channel.

Table 1: Example Clock and Interface Signal Frequency Relationship

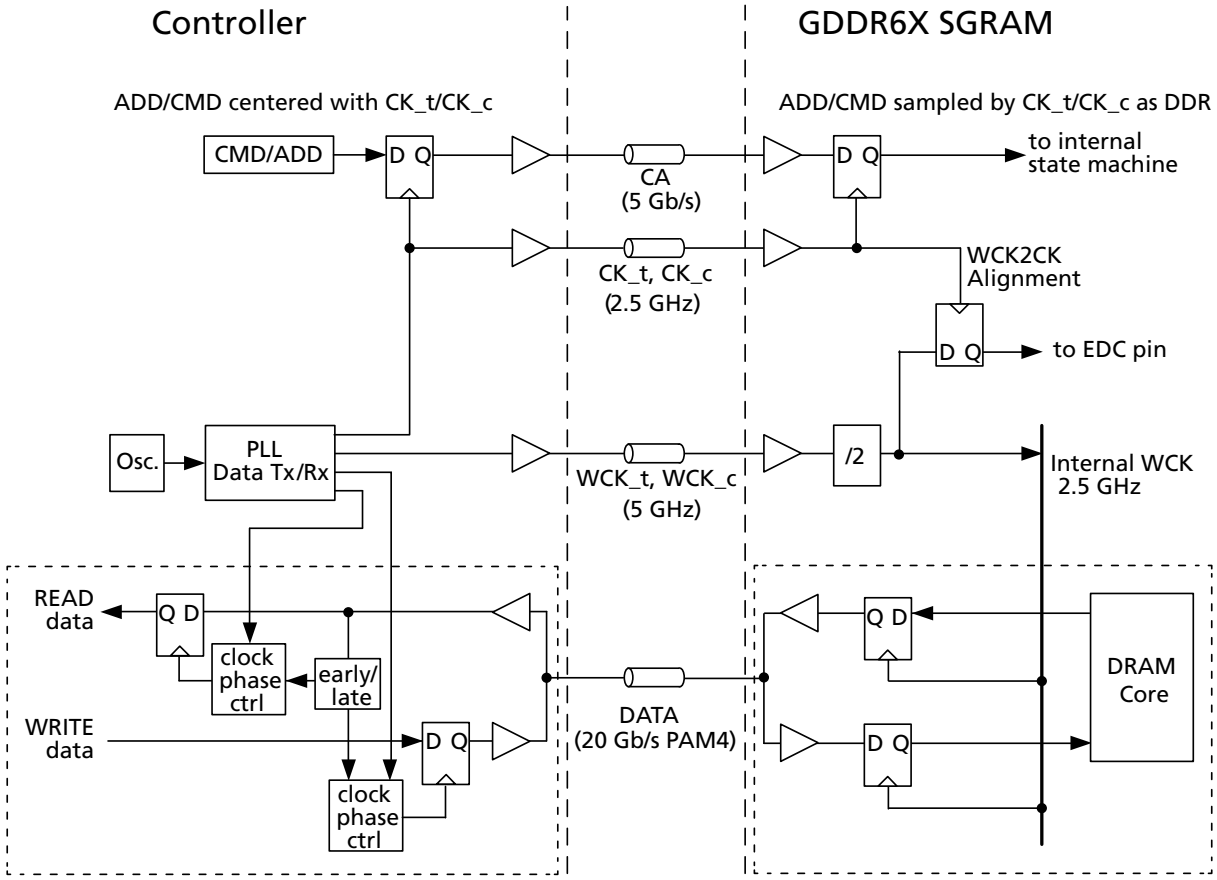
Pin	PAM4 Mode		RDQS Mode	
	Value	Unit	Value	Unit
CK_t, CK_c	2.5	GHz	250	MHz
CA	5	Gb/s/pin	500	Mb/s/pin
WCK_t, WCK_c	5	GHz	1	GHz
DQ, DBI	20	Gb/s/pin	2	Gb/s/pin
	10	GBaud/pin		
EDC	10	Gb/s/pin	2	Gb/s/pin

Figure 3: Clocking and Interface Relationship



Note: 1. The figure shows the relationship between the data or symbol rate of the buses and the clocks; it is not a timing diagram.

Figure 4: Block Diagram of an Example Clock System



Addressing

GDDR6X addressing is defined for a single channel with devices having two channels per device.

Table 2: Addressing

Parameter	8Gb Density	
	x16 Mode	x8 Mode
Number of channels	2	
Memory density (per channel)	4Gb	
Memory prefetch (per channel)	256b	128b
Bank address (per channel)	BA[3:0]	
Row address (per channel)	R[13:0]	
Column address (per channel)	C[5:0]	C[6:0]
Page size (per channel)	2KB	
Refresh	16k/32ms	

Notes:
1. The column address notation for GDDR6X does not include the lower four address bits as the burst order is always fixed for READ and WRITE.
2. Page size = 2^COLBITS × (Prefetch_Size/8) where COLBITS is the number of column address bits.

Operations

Command Truth Table

GDDR6X uses a packetized DDR command/address bus that encodes all commands and addresses on a 10-bit CA bus as outlined in the table below.

Figure 5: Command Truth Table

Operation	Symbol	CK Edge	CKE_n		CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	Notes
			n - 1	n											
NO OPERATION	NOP (1)	R	L	L	H	H	V	V	V	V	V	V	V	V	1, 10
		F			H	H	V	V	V	V	V	V	V	V	
	NOP (2)	R	L	L	H	H	V	V	V	V	V	V	V	V	
		F			H	L	V	V	V	V	V	V	V	V	
	NOP (3)	R	L	L	H	L	V	V	V	V	V	V	V	V	
		F			H	H	V	V	V	V	V	V	V	V	
MODE REGISTER SET	MRS	R	L	L	H	L	M3	M2	M1	M0	OP3	OP2	OP1	OP0	1, 2, 3, 11
		F			H	L	OP11	OP10	OP9	OP8	OP7	OP6	OP5	OP4	
ACTIVATE	ACT	R	L	L	L	V	BA3	BA2	BA1	BA0	R3	R2	R1	R0	1, 2, 4
		F			R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	
READ	RD	R	L	L	H	H	BA3	BA2	BA1	BA0	C3	C2	C1	C0	1, 2, 5, 6
		F			L	H	L	L	V	L	H	C6	C5	C4	
READ with AUTO PRECHARGE	RDA	R	L	L	H	H	BA3	BA2	BA1	BA0	C3	C2	C1	C0	1, 2, 5, 6
		F			L	H	L	L	V	H	H	C6	C5	C4	
LOAD FIFO	LDFF	R	L	L	H	H	B3	B2	B1	B0	D3	D2	D1	D0	1, 2, 8
		F			L	H	H	L	D9	D8	D7	D6	D5	D4	
READ TRAINING	RDTR	R	L	L	H	H	V	V	V	V	V	V	V	V	1, 2, 6
		F			L	H	H	H	V	L	H	V	V	V	
WRITE	WOM	R	L	L	H	H	BA3	BA2	BA1	BA0	C3	C2	C1	C0	1, 2, 5, 6
		F			L	L	L	L	V	L	H	C6	C5	C4	
WRITE with AUTO PRECHARGE	WOMA	R	L	L	H	H	BA3	BA2	BA1	BA0	C3	C2	C1	C0	1, 2, 5, 6
		F			L	L	L	L	V	H	H	C6	C5	C4	
WRITE SINGLE BYTE MASK	WSM	R	L	L	H	H	BA3	BA2	BA1	BA0	C3	C2	C1	C0	1, 2, 5, 6
		F			L	L	L	H	V	L	H	C6	C5	C4	
		R			H	H	Byte 0 BST7	Byte 0 BST6	Byte 0 BST5	Byte 0 BST4	Byte 0 BST3	Byte 0 BST2	Byte 0 BST1	Byte 0 BST0	
		F			H	H	Byte 0 BST15	Byte 0 BST14	Byte 0 BST13	Byte 0 BST12	Byte 0 BST11	Byte 0 BST10	Byte 0 BST9	Byte 0 BST8	
		R			H	H	Byte 1 BST7	Byte 1 BST6	Byte 1 BST5	Byte 1 BST4	Byte 1 BST3	Byte 1 BST2	Byte 1 BST1	Byte 1 BST0	
		F			H	H	Byte 1 BST15	Byte 1 BST14	Byte 1 BST13	Byte 1 BST12	Byte 1 BST11	Byte 1 BST10	Byte 1 BST9	Byte 1 BST8	

Figure 6: Command Truth Table (Continued)

Operation	Symbol	CK Edge	CKE_n		CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	Notes
			n - 1	n											
WRITE SINGLE BYTE MASK with AUTO PRECHARGE	WSMA	R	L	L	H	H	BA3	BA2	BA1	BA0	C3	C2	C1	C0	1, 2, 5, 6
		F			L	L	L	H	V	H	H	C6	C5	C4	
		R			H	H	Byte 0 BST7	Byte 0 BST6	Byte 0 BST5	Byte 0 BST4	Byte 0 BST3	Byte 0 BST2	Byte 0 BST1	Byte 0 BST0	
		F			H	H	Byte 0 BST15	Byte 0 BST14	Byte 0 BST13	Byte 0 BST12	Byte 0 BST11	Byte 0 BST10	Byte 0 BST9	Byte 0 BST8	
		R			H	H	Byte 1 BST7	Byte 1 BST6	Byte 1 BST5	Byte 1 BST4	Byte 1 BST3	Byte 1 BST2	Byte 1 BST1	Byte 1 BST0	
		F			H	H	Byte 1 BST15	Byte 1 BST14	Byte 1 BST13	Byte 1 BST12	Byte 1 BST11	Byte 1 BST10	Byte 1 BST9	Byte 1 BST8	
WRITE DOUBLE BYTE MASK	WDM	R	L	L	H	H	BA3	BA2	BA1	BA0	C3	C2	C1	C0	1, 2, 5, 6
		F			L	L	H	L	V	L	H	C6	C5	C4	
		R			H	H	BST7	BST6	BST5	BST4	BST3	BST2	BST1	BST0	
		F			H	H	BST15	BST14	BST13	BST12	BST11	BST10	BST9	BST8	
WRITE DOUBLE BYTE MASK with AUTO PRECHARGE	WDMA	R	L	L	H	H	BA3	BA2	BA1	BA0	C3	C2	C1	C0	1, 2, 5, 6
		F			L	L	H	L	V	H	H	C6	C5	C4	
		R			H	H	BST7	BST6	BST5	BST4	BST3	BST2	BST1	BST0	
		F			H	H	BST15	BST14	BST13	BST12	BST11	BST10	BST9	BST8	
WRITE TRAINING	WRTR	R	L	L	H	H	V	V	V	V	V	V	V	V	1, 2, 6
		F			L	L	H	H	V	L	H	V	V	V	
PRECHARGE	PREpb	R	L	L	H	L	BA3	BA2	BA1	BA0	V	V	V	V	1, 2, 9
		F			L	L	V	V	V	L	V	V	V	V	
PRECHARGE ALL	PREab	R	L	L	H	L	V	V	V	V	V	V	V	V	1, 2
		F			L	L	V	V	V	H	V	V	V	V	
PER-BANK REFRESH	REFpb/ REFp2b	R	L	L	H	L	BA3	BA2	BA1	BA0	V	V	V	V	1, 2, 7, 9
		F			L	H	V	V	V	L	V	V	V	V	
REFRESH	REFab	R	L	L	H	L	V	V	V	V	V	V	V	V	1, 2, 7
		F			L	H	V	V	V	H	V	V	V	V	
POWER-DOWN ENTRY	PDE	R	L	H	H	H	V	V	V	V	V	V	V	V	1, 2
		F			H	H	V	V	V	V	V	V	V	V	
POWER-DOWN EXIT	PDX	R	H	L	H	H	V	V	V	V	V	V	V	V	1, 2
		F			H	H	V	V	V	V	V	V	V	V	
SELF REFRESH ENTRY	SRE	R	L	H	H	L	V	V	V	V	V	V	V	V	1, 2, 7
		F			L	H	V	V	V	V	V	V	V	V	
SELF REFRESH EXIT	SRX	R	H	L	H	H	V	V	V	V	V	V	V	V	1, 2
		F			H	H	V	V	V	V	V	V	V	V	
COMMAND/ADDRESS TRAINING CAPTURE	CAT	R	L	H	V	V	V	V	V	V	V	V	V	V	1, 2
		F			V	V	V	V	V	V	V	V	V	V	

Notes: 1. H = Logic HIGH level; L = Logic LOW level; V = Valid signal (H or L, but not floating). R, F = Rising, Falling CK clock edge.

2. Values shown for CA[9:0] are logical values; the physical values are inverted when command/address bus inversion (CABI) is enabled and CABI_n = L.
3. M[3:0] provide the mode register address (MRA), OP[11:0] the opcode to be loaded.
4. BA[3:0] provide the bank address, R[13:0] provide the row address.
5. BA[3:0] provide the bank address, C[6:0] provide the column address; no sub-word addressing within a burst of 16. BST[15:0] provide the write data mask for each burst position with WDM(A) and WSM(A) commands.
6. (blank)
7. The command is REFRESH or PER-BANK REFRESH/PER-2-BANK REFRESH when CKE_n(n) = L and SELF REFRESH ENTRY when CKE_n(n) = H.
8. B[3:0] select the burst position, and D[9:0] provide the data.
9. BA[3:0] provide the bank address.
10. All three encodings perform the same NOP. NOP (2) and NOP (3) encodings are only allowed during CA Training.
11. MRS command to MR15 with M[3:0] = 1111, CKE_n(n-1) = H, and CKE_n(n) = H is allowed during the change to the mapping while in CA training mode or the exit of CA training mode. See CA training for more details.

Operating Conditions

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 3: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	–0.3	2.0	V	1
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	–0.3	2.0	V	1
V_{PP}	Voltage on V_{PP} pin relative to V_{SS}	–0.3	2.3	V	2
V_{IN}/V_{OUT}	Voltage on any pins relative to V_{SS}	–0.3	2.0	V	
T_{STG}	Storage temperature	–55	+125	°C	3

Notes:
1. V_{DD} and V_{DDQ} must be within 300mV of each other at all times the device is powered-up except when the device is in hibernate self refresh with V_{DDQ} off state.
2. V_{PP} must be equal or greater than V_{DD} and V_{DDQ} at all times the device is powered-up.
3. Storage temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, refer to the JESD51-2 standard.

Basic DC Operating Conditions

Table 4: Basic DC Operating Conditions

Symbol	Parameter	High			Low			Unit	Notes
		Min	Typ	Max	Min	Typ	Max		
V_{DD}	Device supply voltage	1.3095	1.35	1.3905	1.2125	1.25	1.2875	V	1, 2
V_{DDQ}	Output supply voltage	1.3095	1.35	1.3905	1.2125	1.25	1.2875	V	1, 2
V_{PP}	Pump voltage	1.746	1.8	1.908	1.746	1.8	1.908	V	2

Notes:
1. GDDR6X SGRAM are designed to tolerate PCB designs with separate V_{DD} and V_{DDQ} power regulators.
2. DC bandwidth is limited to 20 MHz.

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.