MC10EP139, MC100EP139

3.3 V / 5 V ECL ÷2/4, ÷4/5/6 Clock Generation Chip

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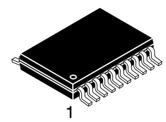
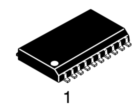
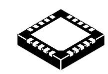


TSSOP−20 WB
DT SUFFIX
CASE 948E

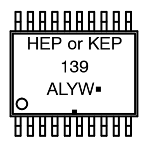


SOIC−20 WB
DW SUFFIX
CASE 751D

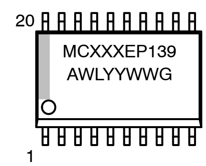


QFN−20
MN SUFFIX
CASE 485E

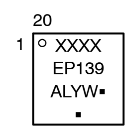
MARKING DIAGRAMS*



TSSOP−20 WB



SOIC−20 WB



QFN−20

HEP	=	MC10EP
KEP	=	MC100EP
XXX	=	10 or 100
A	=	Assembly Location
L,WL	=	Wafer Lot
Y, YY	=	Year
W, WW	=	Work Week
G or ▪	=	Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

Description

The MC10/100EP139 is a low skew ÷2/4, ÷4/5/6 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned.

The common enable ($\overline{EN}$) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon start-up, the internal flip-flops will attain a random state; therefore the master reset (MR) input may require assertion to ensure system synchronization. Internal divider design ensures synchronization between the ÷2/4 and the ÷4/5/6 outputs within a device. All V_{CC} and V_{EE} pins must be externally connected to power supply to guarantee proper operation.

The V_{BB} Pin, an internally generated voltage supply, is available to this device only. For Single-Ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, VBB should be left open.

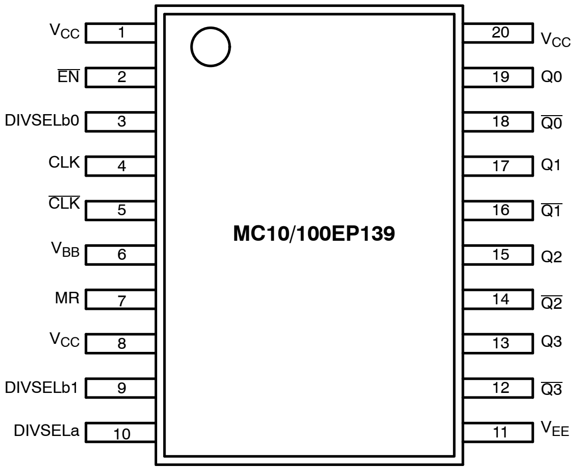
The 100 Series contains temperature compensation.

Features

- Maximum Frequency = > 1.0 GHz Typical
- 50 ps Output-to-Output Skew
- PECL Mode Operating Range:
  V_{CC} = 3.0 V to 5.5 V with V_{EE} = 0 V
- NECL Mode Operating Range:
  V_{CC} = 0 V with V_{EE} = −3.0 V to −5.5 V
- Open Input Default State
- Safety Clamp on Inputs
- Synchronous Enable/Disable
- Master Reset for Synchronization of Multiple Chips
- V_{BB} Output
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

August, 2016 − Rev. 14

Publication Order Number:
MC10EP139/D



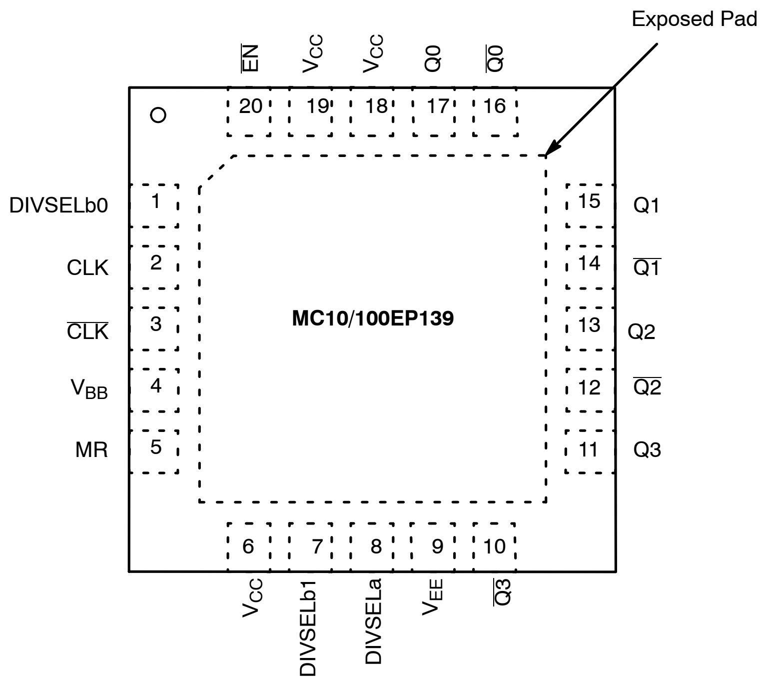
Warning: All V_{CC} and V_{EE} pins must be externally connected to a Power Supply to guarantee proper operation.

Figure 1. 20-Lead Pinout (Top View)

Table 1. PIN DESCRIPTION

PIN	FUNCTION
CLK*, $\overline{\text{CLK}}$*	ECL Differential Clock Inputs
$\overline{\text{EN}}$*	ECL Sync Enable
MR*	ECL Master Reset
V_{BB}	ECL Reference Output
Q0, Q1, $\overline{\text{Q0}}$, $\overline{\text{Q1}}$	ECL Differential ÷2/4 Outputs
Q2, Q3, $\overline{\text{Q2}}$, $\overline{\text{Q3}}$	ECL Differential ÷4/5/6 Outputs
DIVSELa*	ECL Frequency Select Input ÷2/4
DIVSELb0*	ECL Frequency Select Input ÷4/5/6
DIVSELb1*	ECL Frequency Select Input ÷4/5/6
V_{CC}	ECL Positive Supply
V_{EE}	ECL Negative Supply
EP	Exposed Pad

*Pins will default low when left open.



Warning: All V_{CC} and V_{EE} pins must be externally connected to a Power Supply to guarantee proper operation.
The Exposed Pad (EP) on package bottom must be attached to a heat-sinking conduit. The Exposed Pad may only be electrically connected to V_{EE}.

Figure 2. QFN-20 Pinout (Top View)

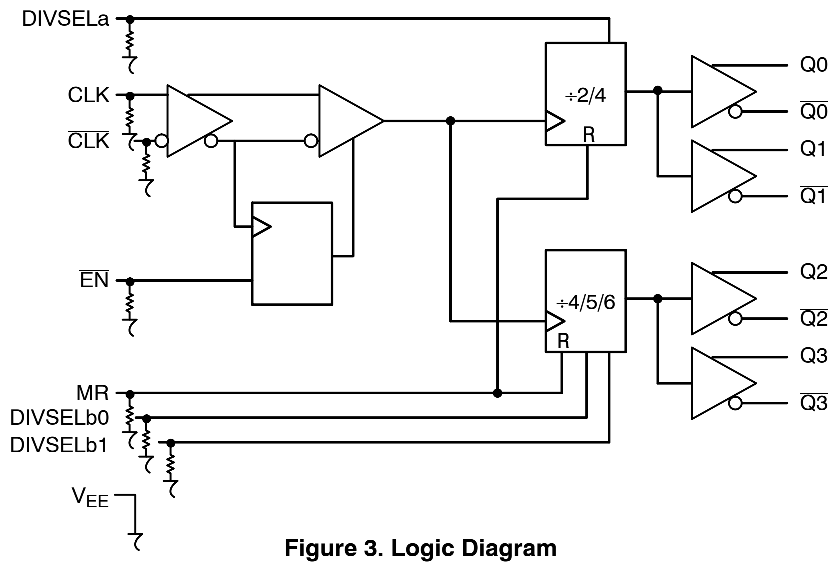


Figure 3. Logic Diagram

Table 2. FUNCTION TABLES

CLK	$\overline{EN}$	MR	Function
Z	L	L	Divide
ZZ	H	L	Hold Q0:3
X	X	H	Reset Q0:3

Z = Low-to-High Transition
ZZ = High-to-Low Transition

DIVSELa	Q0:1 Outputs
L	Divide by 2
H	Divide by 4

DIVSELb0	DIVSELb1	Q2:3 Outputs
L	L	Divide by 4
H	L	Divide by 6
L	H	Divide by 5
H	H	Divide by 5

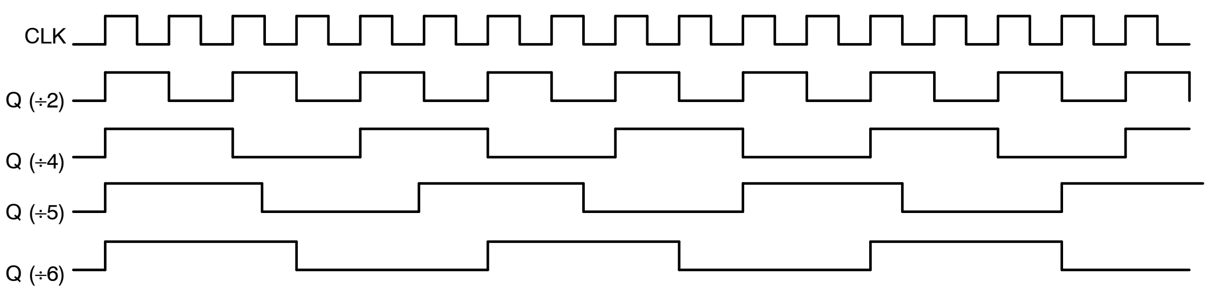


Figure 4. CLK and OUTPUT Timing Diagram

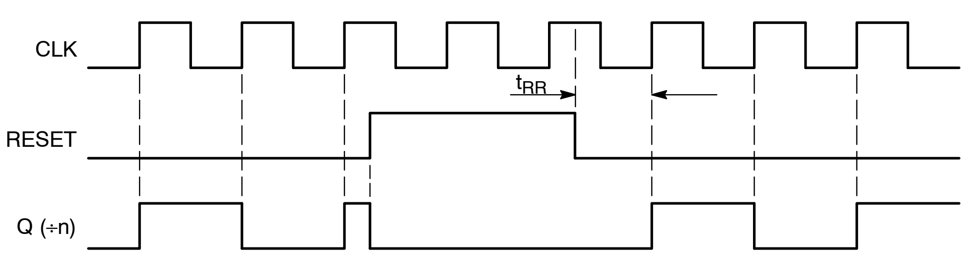


Figure 5. Timing Diagram

Table 3. ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pullup Resistor		N/A
ESD Protection Human Body Model Machine Model Charged Device Model		 > 2 kV > 100 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Pb-Free Pkg
SOIC−20 WB TSSOP−20 WB QFN−20		Level 3 Level 1 Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		758 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		6	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		−6	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 −6	V
I_{out}	Output Current	Continuous Surge		50 100	mA
I_{BB}	V_{BB} Sink/Source			±0.5	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP−20 WB TSSOP−20 WB	140 100	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP−20 WB	23 to 41	°C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC−20 WB SOIC−20 WB	90 60	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC−20 WB	33 to 35	°C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	QFN−20 QFN−20	47 33	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	QFN−20	18	°C/W
T_{sol}	Wave Solder (Pb-Free)	< 2 to 3 sec @ 260°C		265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 5. 10EP DC CHARACTERISTICS, PECL (V_{CC} = 3.3 V, V_{EE} = 0 V (Note 1))

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	65	82	105	65	83	105	65	84	105	mA
V_{OH}	Output HIGH Voltage (Note 2)	2165	2290	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 2)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1365		1690	1460		1755	1490		1815	mV
V_{BB}	Output Voltage Reference	1790	1890	1990	1855	1955	2055	1915	2015	2115	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3 V to −2.2 V.
2. All loading with 50 Ω to V_{CC} − 2.0 V (see Figure 10).
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 6. 10EP DC CHARACTERISTICS, PECL (V_{CC} = 5.0 V, V_{EE} = 0 V (Note 1))

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	65	82	105	65	83	105	65	84	105	mA
V_{OH}	Output HIGH Voltage (Note 2)	3865	3990	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage (Note 2)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	3790		4115	3855		4180	3915		4240	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3065		3390	3130		3455	3190		3515	mV
V_{BB}	Output Voltage Reference	3490	3590	3690	3555	3655	3755	3615	3715	3815	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +2.0 V to −0.5 V.
2. All loading with 50 Ω to V_{CC} − 2.0 V (see Figure 10).
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 7. 10EP DC CHARACTERISTICS, NECL (V_{CC} = 0 V, V_{EE} = −5.5 V to −3.0 V (Note 1))

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	65	82	105	65	83	105	65	84	105	mA
V_{OH}	Output HIGH Voltage (Note 2)	−1135	−1010	−885	−1070	−945	−820	−1010	−885	−760	mV
V_{OL}	Output LOW Voltage (Note 2)	−1935	−1810	−1685	−1870	−1745	−1620	−1810	−1685	−1560	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	−1210		−885	−1145		−820	−1085		−760	mV
V_{IL}	Input LOW Voltage (Single-Ended)	−1935		−1610	−1870		−1545	−1810		−1485	mV
V_{BB}	Output Voltage Reference	−1510	−1410	−1310	−1445	−1345	−1245	−1385	−1285	−1185	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC}.
2. All loading with 50 Ω to V_{CC} − 2.0 V (see Figure 10).
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 8. 100EP DC CHARACTERISTICS, PECL (V_{CC} = 3.3 V, V_{EE} = 0 V (Note 1))

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	70	83	100	70	87	105	75	90	110	mA
V_{OH}	Output HIGH Voltage (Note 2)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 2)	1305	1480	1605	1305	1480	1605	1305	1480	1605	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2075		2420	2075		2420	2075		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1305		1675	1305		1675	1305		1675	mV
V_{BB}	Output Voltage Reference	1725	1825	1925	1725	1825	1925	1725	1825	1925	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3 V to −2.2 V.
2. All loading with 50 Ω to V_{CC} − 2.0 V (see Figure 10).
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 9. 100EP DC CHARACTERISTICS, PECL (V_{CC} = 5.0 V, V_{EE} = 0 V (Note 1))

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	70	85	100	70	90	105	75	95	110	mA
V_{OH}	Output HIGH Voltage (Note 2)	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
V_{OL}	Output LOW Voltage (Note 2)	3005	3180	3305	3005	3180	3305	3005	3180	3305	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	3775		4120	3775		4120	3775		4120	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3005		3375	3005		3375	3005		3375	mV
V_{BB}	Output Voltage Reference	3425	3525	3625	3425	3525	3625	3425	3525	3625	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +2.0 V to −0.5 V.
2. All loading with 50 Ω to V_{CC} − 2.0 V (see Figure 10).
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 10. 100EP DC CHARACTERISTICS, NECL (V_{CC} = 0 V, V_{EE} = −5.5 V to −3.0 V (Note 1))

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	70	85	100	70	90	105	75	95	110	mA
V_{OH}	Output HIGH Voltage (Note 2)	−1145	−1020	−895	−1145	−1020	−895	−1145	−1020	−895	mV
V_{OL}	Output LOW Voltage (Note 2)	−1995	−1820	−1695	−1995	−1820	−1695	−1995	−1820	−1695	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	−1225		−880	−1225		−880	−1225		−880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	−1995		−1625	−1995		−1625	−1995		−1625	mV
V_{BB}	Output Voltage Reference	−1575	−1475	−1375	−1575	−1475	−1375	−1575	−1475	−1375	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC}.
2. All loading with 50 Ω to V_{CC} − 2.0 V (see Figure 10).
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 11. AC CHARACTERISTICS (V_{CC} = 0 V; V_{EE} = −3.0 V to −5.5 V or V_{CC} = 3.0 V to 5.5 V; V_{EE} = 0 V (Note 1))

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency (See Figures 6, 7, 8 and 9 F_{max} /JITTER)		> 1			> 1			> 1		GHz
t_{PLH}, t_{PHL}	Propagation Delay CLK, Q (Diff) MR, Q	 550 700	 700 800	 800 900	 600 700	 750 850	 900 1000	 675 800	 825 950	 975 1100	ps
t_{RR}	Reset Recovery	200	100		200	100		200	100		ps
t_s	Setup Time $\overline{EN}$, $\overline{CLK}$ DIVSEL, CLK	 200 400	 120 180		 200 400	 120 180		 200 400	 120 180		ps
t_h	Hold Time $\overline{CLK}$, $\overline{EN}$ CLK, DIVSEL	 100 200	 50 140		 100 200	 50 140		 100 200	 50 140		ps
t_{PW}	Minimum Pulse Width MR	 550	 450		 550	 450		 550	 450		ps
t_{SKEW}	Within Device Skew Q, $\overline{Q}$ Device-to-Device Skew (Note 2)		50 200	100 300		50 200	100 300		50 200	100 300	ps
t_{JITTER}	Random Clock Jitter (RMS) (See Figures 6, 7, 8 and 9 F_{max}/JITTER)		0.2	< 1.0		0.2	< 1.0		0.2	< 1.5	ps
V_{PP}	Input Voltage Swing (Differential Configuration)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times Q, $\overline{Q}$ (20%−80%)	110	180	250	125	190	275	150	215	300	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC} − 2.0 V (see Figure 10).
2. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

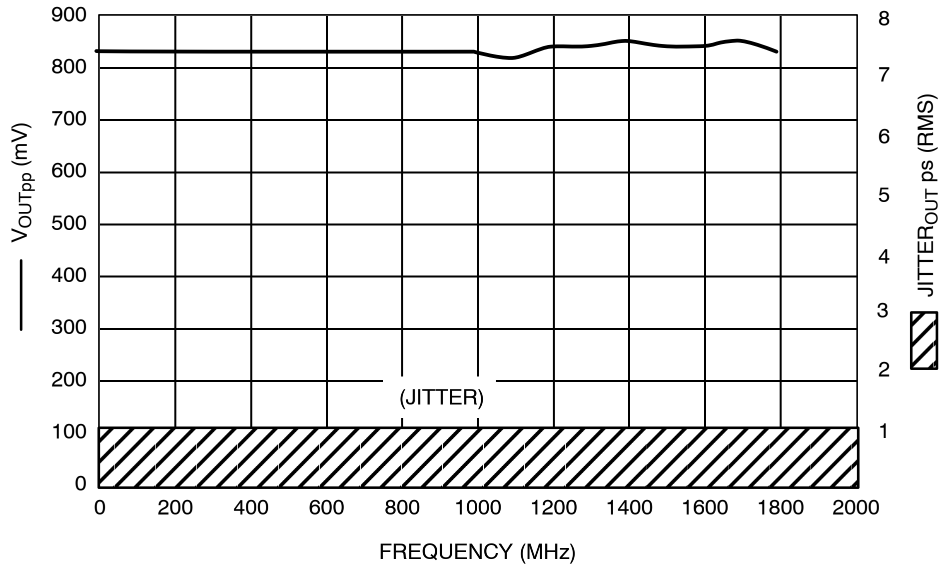


Figure 6. ÷2, F_{max}/Jitter

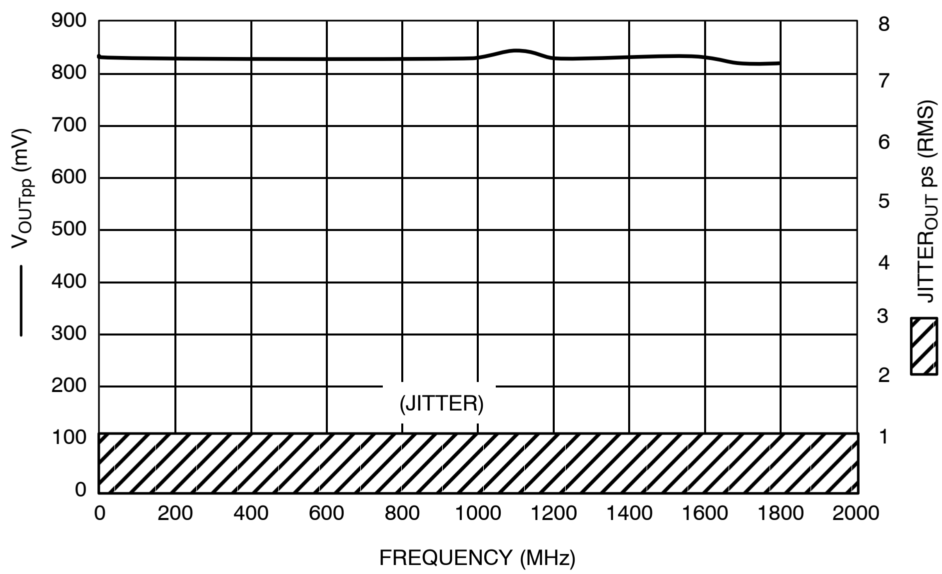


Figure 7. ÷5, F_{max}/Jitter

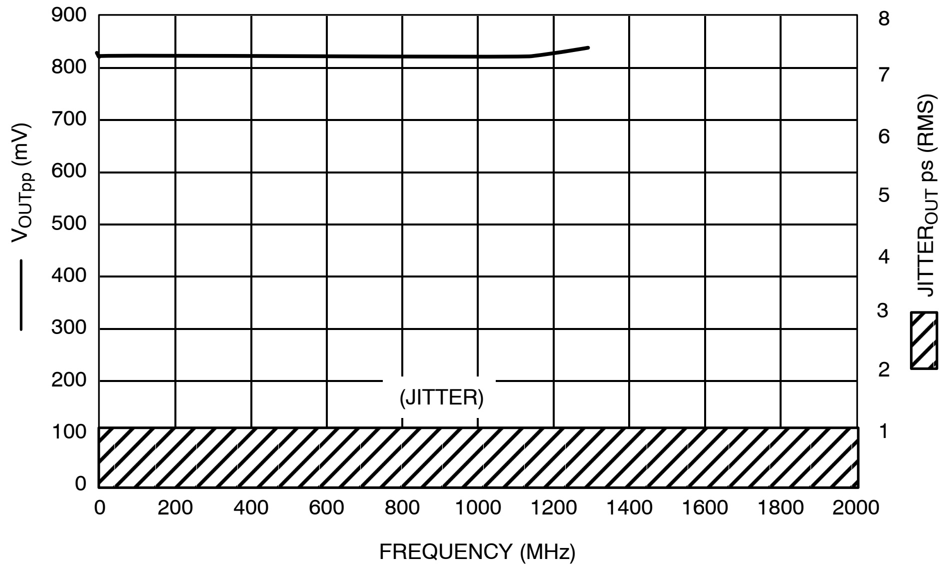


Figure 8. ÷4, F_{max}/Jitter

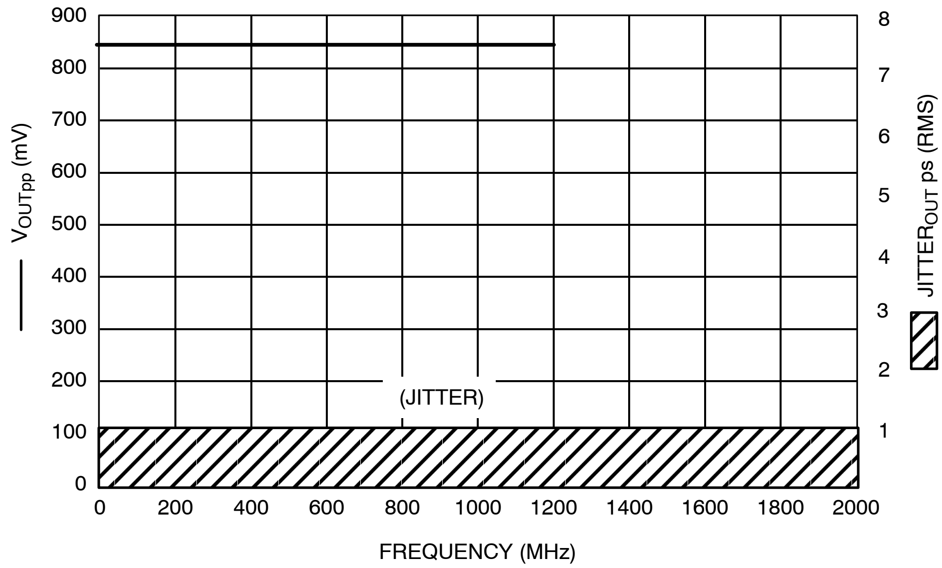


Figure 9. ÷6, F_{max}/Jitter

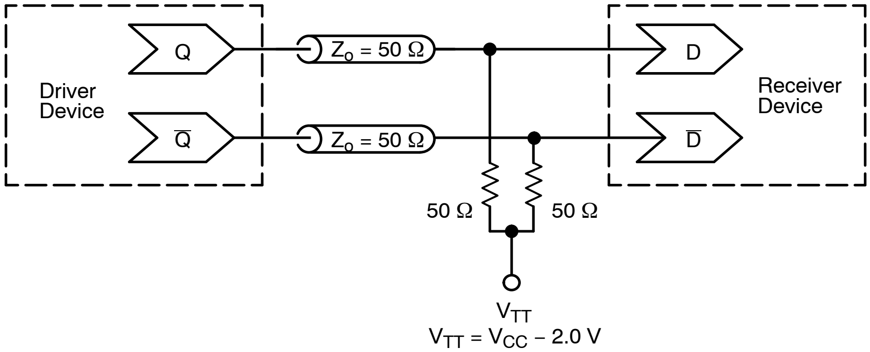


Figure 10. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices)

ORDERING INFORMATION

Device	Package	Shipping†
MC10EP139DTG	TSSOP−20 WB (Pb-Free)	75 Units / Tube
MC10EP139DTR2G	TSSOP−20 WB (Pb-Free)	2500 / Tape & Reel
MC10EP139DWG	SOIC−20 WB (Pb-Free)	38 Units / Tube
MC10EP139DWR2G	SOIC−20 WB (Pb-Free)	1000 / Tape & Reel
MC100EP139DTG	TSSOP−20 WB (Pb-Free)	75 Units / Tube
MC100EP139DTR2G	TSSOP−20 WB (Pb-Free)	2500 / Tape & Reel
MC100EP139DWG	SOIC−20 WB (Pb-Free)	38 Units / Tube
MC100EP139DWR2G	SOIC−20 WB (Pb-Free)	1000 / Tape & Reel
MC100EP139MNG	QFN−20 (Pb-Free)	92 Units / Tube
MC100EP139MNTXG	QFN−20 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

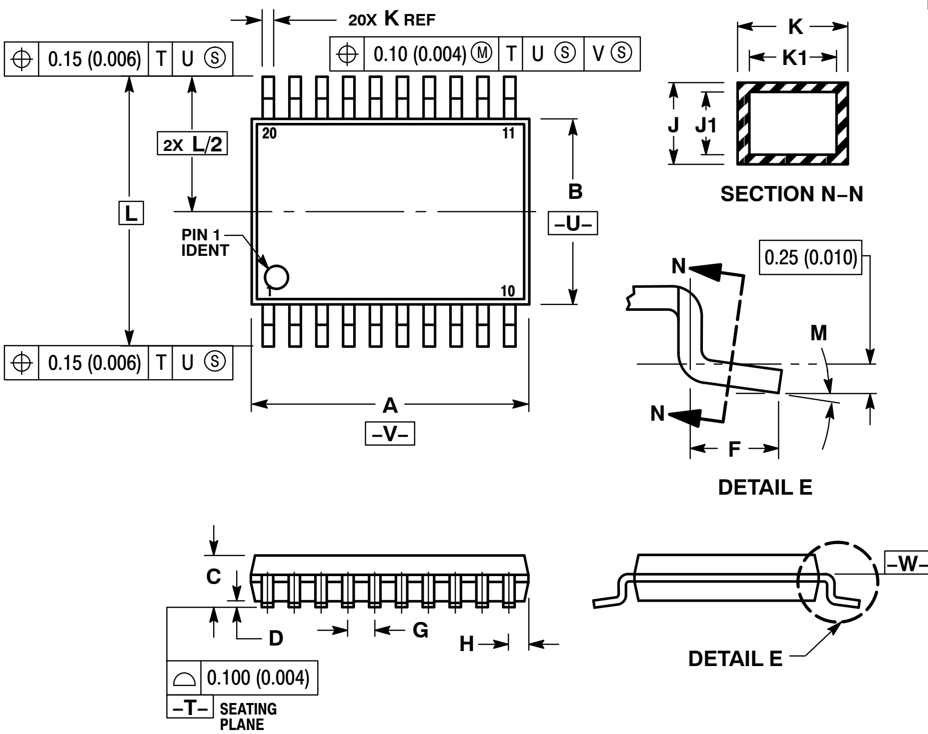
AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

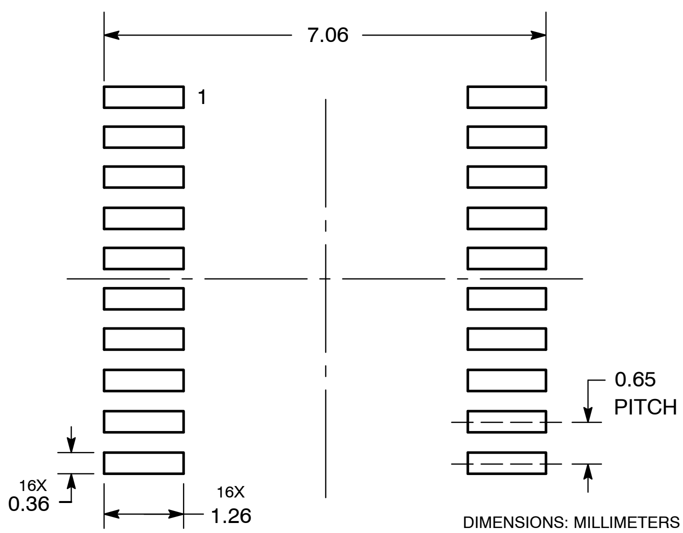
TSSOP−20 WB
CASE 948E
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

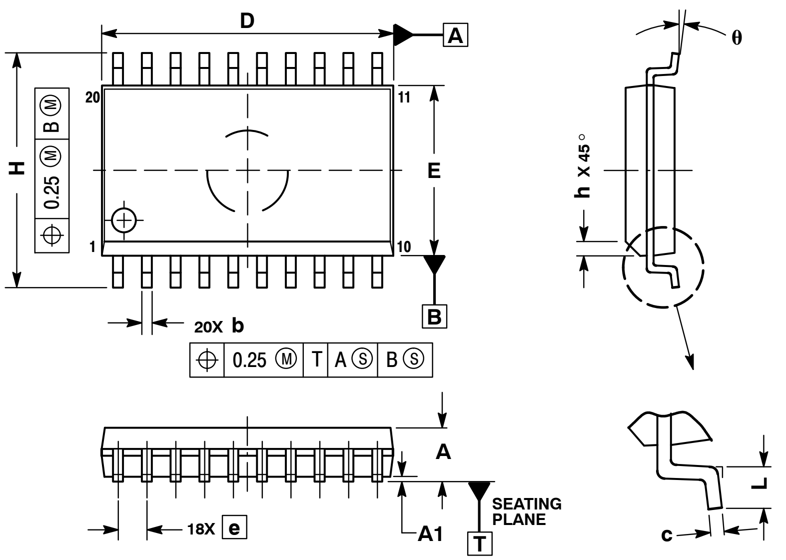
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



PACKAGE DIMENSIONS

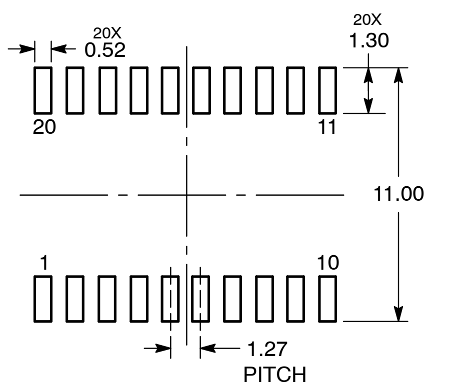
SOIC−20 WB
CASE 751D−05
ISSUE H



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

RECOMMENDED SOLDERING FOOTPRINT*

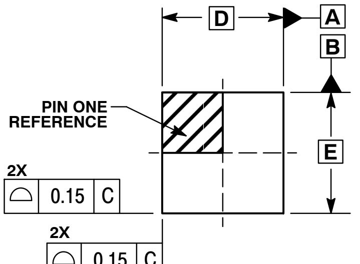


DIMENSIONS: MILLIMETERS

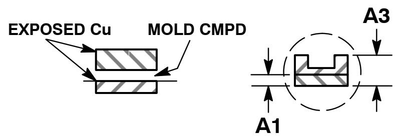
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

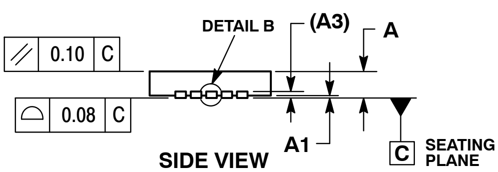
QFN−20, 4x4, 0.5P
CASE 485E−01
ISSUE B



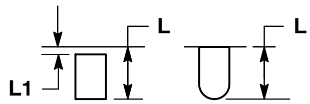
TOP VIEW



DETAIL B
OPTIONAL CONSTRUCTIONS



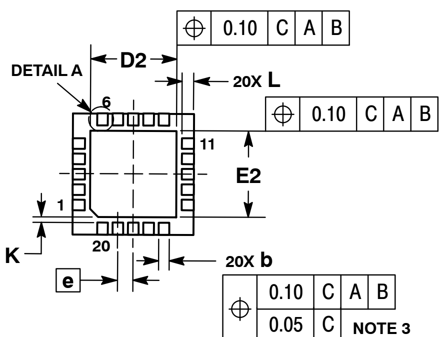
SIDE VIEW



DETAIL A
OPTIONAL CONSTRUCTIONS

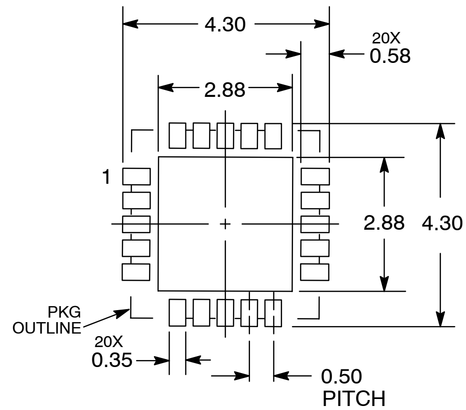
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.20	0.30
D	4.00 BSC	
D2	2.60	2.90
E	4.00 BSC	
E2	2.60	2.90
e	0.50 BSC	
K	0.20 REF	
L	0.35	0.45
L1	0.00	0.15



BOTTOM VIEW

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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