

# LC3564B, BS, BM, BT-70/10

# 64K (8192-word $\times$ 8-bit) SRAM with $\overline{OE}$ , $\overline{CE1}$ , and CE2 Control Pins

# Overview

The LC3564B, LC3564BS, LC3564BM, and LC3564BT are 8192-word × 8-bit asynchronous silicon gate CMOS SRAMs. These are full CMOS type SRAMs that adopt a six-transistor memory cell and feature fast access times, low operating power dissipation, and an ultralow standby current. These SRAMs provide three control signal inputs: an  $\overline{OE}$  input for high-speed memory access, and two chip enable lines,  $\overline{CE1}$  and CE2, for low power mode and device selection. These means that these SRAMs area ideal for systems that require low power and battery backup, and that they support easy memory expansion. The ultralow standby current that is a feature of these SRAMs allows them to be used with capacitor backup as well. Since these SRAMs support 3-V operation, they are also appropriate for use in portable battery operated systems.

# Features

- Supply voltage range: 2.7 to 5.5 V
- In 5-V operation mode:  $5.0 \text{ V} \pm 10\%$
- In 3-V operation mode: 3.0 V  $\pm 10\%$
- Address access time (t<sub>AA</sub>)
  - In 5-V operation mode: LC3564B, BS, BM, and BT-70: 70 ns (max) LC3564B, BS, BM, and BT-10: 100 ns (max)
  - In 3-V operation mode: LC3564B, BS, BM, and BT-70: 200 ns (max) LC3564B, BS, BM, and BT-10: 500 ns (max)
- Ultralow standby current
  - In 5-V operation mode: 1.0  $\mu$ A (Ta  $\leq$  70°C), 3.0  $\mu$ A (Ta  $\leq$  85°C)
  - In 3-V operation mode: 0.8  $\mu$ A (Ta  $\leq$  70°C), 2.5  $\mu$ A (Ta  $\leq$  85°C)
- Operating temperature range
  - In 5-V operation mode: -40 to 85°C
  - In 3-V operation mode: -40 to 85°C
- Data retention supply voltage: 2.0 to 5.5 V
- All input and output levels:
  - In 5-V operation mode: TTL compatible levels
  - In 3-V operation mode:  $V_{CC}$  –0.2 V/0.2 V

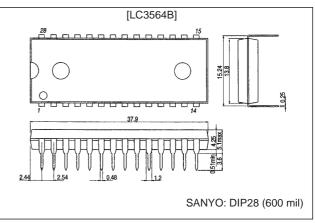
- Three control inputs:  $\overline{OE}$ ,  $\overline{CE1}$ , and CE2
- Shared input and output pins, three-state outputs
- · No clock required
- Packages

28-pin DIP (600 mil) plastic package: LC3564B
28-pin DIP (300 mil) plastic package: LC3564BS
28-pin SOP (450 mil) plastic package: LC3564BM
28-pin TSOP (8 × 13.4 mm) plastic package: LC3564BT

# Package Dimensions

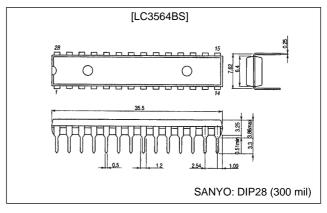
unit: mm

## 3012A-DIP28 (600 mil)



unit: mm

#### 3133-DIP28 (300 mil)

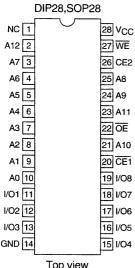


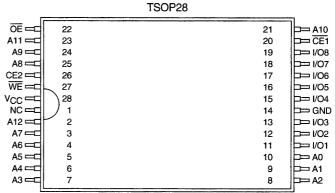
SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

## LC3564B, BS, BM, BT-70/10

#### unit: mm unit: mm 3187-SOP28 3221-TSOP28 (type I) [LC3564BT] [LC3564BM] 21 ARAARAABBAAAAAA $\cap$ 18.0 0.55 • 0 125 8 0.4 1.27 SANYO: SOP28 SANYO: TSOP28 (type I) ŝ

## **Pin Assignments**

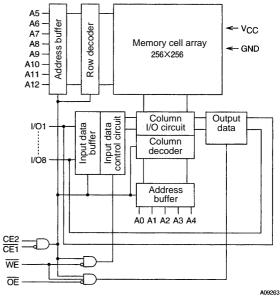




Top view



#### **Block Diagram**



# **Pin Functions**

A0 to A12	Address inputs
WE	Read/write control input
ŌĒ	Output enable input
CE1, CE2	Chip enable inputs
I/O1 to I/O8	Data I/O
V <sub>CC</sub> , GND	Power supply and ground

## **Function Table**

Mode	CE1	CE2	ŌE	WE	I/O	Supply current
Read cycle	L	Н	L	Н	Data output	I <sub>CCA</sub>
Write cycle	L	Н	х	L	Data input	I <sub>CCA</sub>
Output disable	L	Н	Н	Н	High impedance	I <sub>CCA</sub>
Not selected	Н	Х	х	Х	High impedance	Iccs
	Х	L	Х	Х	High impedance	Iccs

X : H or L

1/02 12 GND 14 Top view A0926

# **Specifications** Absolute Maximum Ratings at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>CC</sub> max		7.0	V
Input voltage	V <sub>IN</sub>		-0.3* to V <sub>CC</sub> + 0.3	V
I/O voltage	V <sub>I/O</sub>		-0.3 to V <sub>CC</sub> + 0.3	V
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +125	°C

Note: For pulse widths less than 30 ns: -3.0 V

## Input and Output Capacitances at $Ta = 25^{\circ}C$ , f = 1 MHz

Parameter	Symbol	Conditions		Ratings		Unit
Falameter	Symbol	ol Conditions —		typ	max	Unit
I/O pin capacitance	C <sub>I/O</sub>	$V_{I/O} = 0 V$		6	10	pF
Input pin capacitance	C <sub>IN</sub>	$V_{IN} = 0 V$		6	10	pF

Note: These parameters are sampled, and are not measured for every unit.

# [5-V Operation]

# DC Allowable Operating Ranges at Ta = -40 to +85°C, $V_{CC}$ = 4.5 to 5.5 V

Parameter	Symbol	Conditions		Ratings		Unit
Falalletei	Symbol	Symbol Conditions -		typ	max	Unit
Supply voltage	V <sub>CC</sub>		4.5	5.0	5.5	V
Input voltage	V <sub>IH</sub>		2.2		V <sub>CC</sub> + 0.3	V
	V <sub>IL</sub>		-0.3*		+0.8	V

Note: For pulse widths less than 30 ns: -3.0 V

# DC Electrical Characteristics at Ta = –40 to +85°C, $V_{CC}$ = 4.5 to 5.5 $\rm V$

Deserve	-4	O maked	0	-1141				Ratings		1.1 14
Parame	eter	Symbol	Con	Conditions		min	typ *	max	Unit	
Input leakage current		ILI	$V_{IN} = 0$ to $V_{CC}$				-1.0		+1.0	μA
I/O leakage current		ILO	$V_{\overline{CE1}} = V_{IH} \text{ or } V_{CE2} = V_{\overline{WE}} = V_{IL}, V_{I/O} = 0 \text{ to}$		V <sub>OE</sub> = \	/ <sub>IH</sub> or	-1.0		+1.0	μA
Output high-level voltage		V <sub>OH</sub>	I <sub>OH</sub> = -1.0 mA				2.4			V
Output low-level voltage		V <sub>OL</sub>	I <sub>OL</sub> = 2.0 mA						0.4	V
		I <sub>CCA1</sub>	$V_{\overline{CE1}} \le 0.2 \text{ V}, V_{CE2} \ge$ $I_{I/O} = 0 \text{ mA}, V_{IN} \le 0.2 \text{ V}$	00	0.2 V,	Ta ≤ 70°C		0.01	1.0	μA
	V <sub>CC</sub> – 0.2 V/0.2 V	·CCAT	$V_{\rm IN} \ge V_{\rm CC} - 0.2 V$			Ta ≤ 85°C			3.0	
	inputs		$V_{\overline{CE1}} \le 0.2 \text{ V}$ , min LC3564B,BS, B		B,BS, BM, BT-70			35	mA	
		I <sub>CCA4</sub>	$V_{CE2} \ge V_{CC} - 0.2 V,$ $I_{I/O} = 0 mA,$	cycle	LC3564E	3,BS,BM,BT-10			30	11D V
				1 µs c	ycle			4		mA
Operating supply current		I <sub>CCA2</sub>	$V_{\overline{CE1}} = V_{IL}, V_{CE2} = V_{IN}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	/ <sub>IH</sub> , I <sub>I/O</sub> :	= 0 mA,				7	mA
	TTL inputs		$V_{\overline{CE1}} = V_{IL},$	min	LC3564E	8,BS, BM, BT-70			40	mA
		I <sub>CCA3</sub>	$V_{CE2} = V_{IH},$ $I_{I/O} = 0 \text{ mA},$	cycle	LC3564B,BS,BM,BT-10				35	110.0
			DUTY = 100%	1 µs c	ycle			7		mA
Standby mode supply	V <sub>CC</sub> – 0.2 V/0.2 V	I <sub>CCS1</sub>	$V_{CE2} \le 0.2 \text{ V or}$ $V_{CE1} \ge V_{CC} - 0.2 \text{ V}$			Ta ≤ 70°C		0.01	1.0	μA
current	inputs		$V_{CE2} \ge V_{CC} - 0.2 V$			Ta ≤ 85°C			3.0	•
	TTL inputs	I <sub>CC2</sub>	$V_{CE2} = V_{IL} \text{ or } V_{\overline{CE1}} =$	VIH, VI	<sub>N</sub> = 0 to	V <sub>CC</sub>			2.0	mA

Note \*: Reference values at  $V_{CC} = 5 V$ , Ta = 25°C

# AC Electrical Characteristics at Ta = –40 to +85°C, $V_{CC}$ = 4.5 to 5.5 V

Parameter	Conditions				
[AC Test Conditions]					
Input pulse voltage	V <sub>IH</sub> = 2.4 V, V <sub>IL</sub> = 0.6 V				
Input rise and fall times	5 ns				
Input and output timing level	1.5 V				
Output load	LC3564B, BS, BM, and BT-70: 30 pF + 1 TTL gate (Including the jig capacitance.)				
	LC3564B, BS, BM, and BT-10: 100 pF + 1 TTL gate (Including the jig capacitance.)				

# Read Cycle

Parameter	Symbol	-70		-1	0	Unit
		min	max	min	max	
Read cycle time	t <sub>RC</sub>	70		100		ns
Address access time	t <sub>AA</sub>		70		100	ns
CE1 access time	t <sub>CA1</sub>		70		100	ns
CE2 access time	t <sub>CA2</sub>		70		100	ns
OE access time	t <sub>OA</sub>		35		50	ns
Output hold time	t <sub>OH</sub>	10		10		ns
CE1 output enable time	t <sub>COE1</sub>	10		10		ns
CE2 output enable time	t <sub>COE2</sub>	10		10		ns
OE output enable time	t <sub>OOE</sub>	5		5		ns
CE1 output disable time	t <sub>COD1</sub>		30		35	ns
CE2 output disable time	t <sub>COD2</sub>		30		35	ns
OE output disable time	t <sub>OOD</sub>		25		25	ns

# Write Cycle

			LC3564B,	BS, BM, BT		
Parameter	Symbol	-7	0	-1	0	Unit
		min	max	min	max	
Write cycle time	t <sub>WC</sub>	70		100		ns
Address setup time	t <sub>AS</sub>	0		0		ns
Write pulse width	t <sub>WP</sub>	50		55		ns
CE1 setup time	t <sub>CW1</sub>	60		65		ns
CE2 setup time	t <sub>CW2</sub>	60		65		ns
Write recovery time	t <sub>WR</sub>	0		0		ns
CE1 write recovery time	t <sub>WR1</sub>	0		0		ns
CE2 write recovery time	t <sub>WR2</sub>	0		0		ns
Data setup time	t <sub>DS</sub>	35		40		ns
Data hold time	t <sub>DH</sub>	0		0		ns
CE1 data hold time	t <sub>DH1</sub>	0		0		ns
CE2 data hold time	t <sub>DH2</sub>	0		0		ns
WE output enable time	t <sub>WOE</sub>	5		5		ns
WE output disable time	t <sub>WOD</sub>		30		35	ns

# [3-V Operation]

# DC Allowable Operating Ranges at Ta = –40 to +85°C, $V_{CC}$ = 2.7 to 3.3 V

Parameter S		Conditions		Unit		
Falameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V <sub>CC</sub>		2.7	3.0	3.3	V
	V <sub>IH</sub>		V <sub>CC</sub> – 0.2		V <sub>CC</sub>	V
Input voltage	V <sub>IL</sub>		0		0.2	V

# DC Electrical Characteristics at Ta = -40 to +85°C, $V_{CC}$ = 2.7 to 3.3 V

Derem	atar	Qumbal	Con	ditiona				Ratings		Unit
Param	eter	Symbol	Con	Conditions				typ *	max	Unit
Input leakage current		ILI	$V_{IN} = 0$ to $V_{CC}$				-1.0		+1.0	μA
I/O leakage current		ILO	$V_{\overline{CE1}} = V_{IH} \text{ or } V_{CE2} = V_{IL} \text{ or } V_{\overline{OE}} = V_{IH} \text{ or}$ $V_{\overline{WE}} = V_{IL}, V_{I/O} = 0 \text{ to } V_{CC}$		-1.0		+1.0	μA		
Output high-level voltage		V <sub>OH</sub>	I <sub>OH</sub> = -0.5 mA				V <sub>CC</sub> – 0.2			V
Output low-level voltage		V <sub>OL</sub>	I <sub>OL</sub> = 1.0 mA						0.2	V
			$V_{CE1} \le V_{IL}, V_{CE2} \ge V_{IL}$ $I_{I/O} = 0 \text{ mA}, V_{IN} \le V_{II}$			Ta ≤ 70°C		0.01	0.8	μA
		I <sub>CCA1</sub>	$V_{IN} \ge V_{IH}$	_ 01		Ta ≤ 85°C			2.5	μΑ
Operation supply current			$V_{\overline{CE1}} \leq V_{IL},$	min	LC3564B	BS, BM, BT-70,			20	mA
	inputs	I <sub>CCA4</sub>	$V_{CE2} \ge V_{IH},$ $I_{I/O} = 0 \text{ mA},$	cycle	LC3564E	,BS,BM,BT-10			10	
			DUTY = 100%	1 µs c	ycle			3		mA
Standby mode supply	V <sub>CC</sub> – 0.2 V/0.2 V		$V_{CE2} \le 0.2 \text{ V or}$ $V_{CE1} \ge V_{IH}$			Ta≤70°C		0.01	0.8	μA
current	inputs	ICCS1	$V_{CE1} \ge V_{IH}$ $V_{CE2} \ge V_{IH}$			Ta ≤ 85°C			2.5	μ/

Note \*: Reference values at  $V_{CC} = 3 \text{ V}$ , Ta = 25°C

# AC Electrical Characteristics at Ta = –40 to +85°C, $V_{CC}$ = 2.7 to 3.3 V

Parameter	Conditions
[AC Test Conditions]	
Input pulse voltage	$V_{IH} = V_{CC} - 0.2 \text{ V}, V_{IL} = 0.2 \text{ V}$
Input rise and fall times	10 ns
Input and output timing level	1.5 V
Output load	LC3564B, BS, BM, BT-70 : 30pF (Including the jig capacitance.)
	LC3564B, BS, BM, BT-10 : 100pF (Including the jig capacitance.)

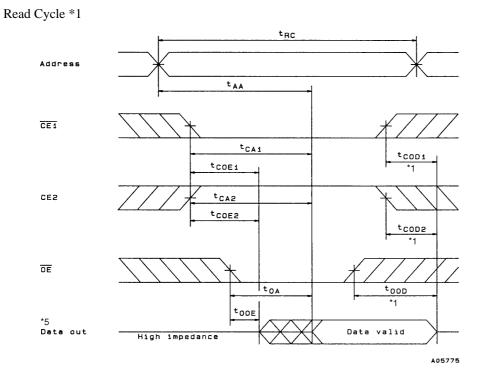
# **Read Cycle**

Parameter	Symbol					
		-70		-10		Unit
		min	max	min	max	
Read cycle time	t <sub>RC</sub>	200		500		ns
Address access time	t <sub>AA</sub>		200		500	ns
CE1 access time	t <sub>CA1</sub>		200		500	ns
CE2 access time	t <sub>CA2</sub>		200		500	ns
OE access time	t <sub>OA</sub>		100		250	ns
Output hold time	t <sub>OH</sub>	20		20		ns
CE1 output enable time	t <sub>COE1</sub>	20		20		ns
CE2 output enable time	t <sub>COE2</sub>	20		20		ns
OE output enable time	tOOE	10		10		ns
CE1 output disable time	t <sub>COD1</sub>		60		120	ns
CE2 output disable time	t <sub>COD2</sub>		60		120	ns
OE output disable time	tOOD		50		100	ns

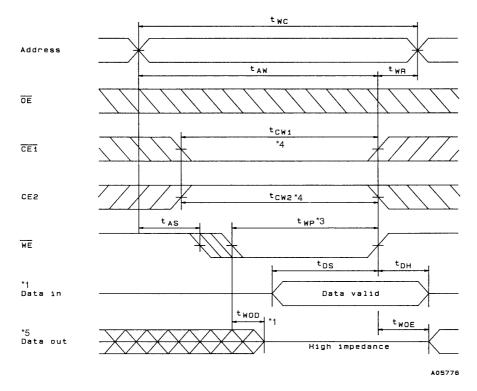
# Write Cycle

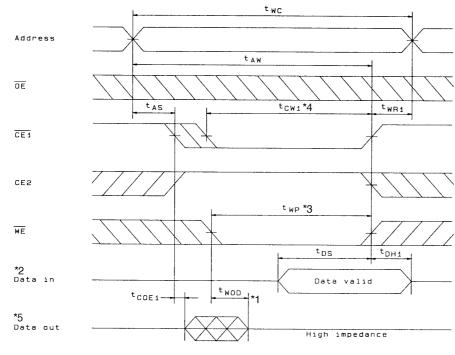
Parameter		LC3564B, BS, BM, BT				
	Symbol	-70		-10		Unit
		min	max	min	max	
Write cycle time	t <sub>WC</sub>	200		500		ns
Address setup time	t <sub>AS</sub>	0		0		ns
Write pulse width	t <sub>WP</sub>	140		200		ns
CE1 setup time	t <sub>CW1</sub>	150		250		ns
CE2 setup time	t <sub>CW2</sub>	0		250		ns
Write recovery time	t <sub>WR</sub>	0		0		ns
CE1 write recovery time	t <sub>WR1</sub>	0		0		ns
CE2 write recovery time	t <sub>WR2</sub>	130		0		ns
Data setup time	t <sub>DS</sub>	0		180		ns
Data hold time	t <sub>DH</sub>	0		0		ns
CE1 data hold time	t <sub>DH1</sub>	0		0		ns
CE2 data hold time	t <sub>DH2</sub>	10		0		ns
WE output enable time	t <sub>WOE</sub>			10		ns
WE output disable time	t <sub>WOD</sub>		60		120	ns

# **Timing Charts**



# Write Cycle (1): WE Write \*6

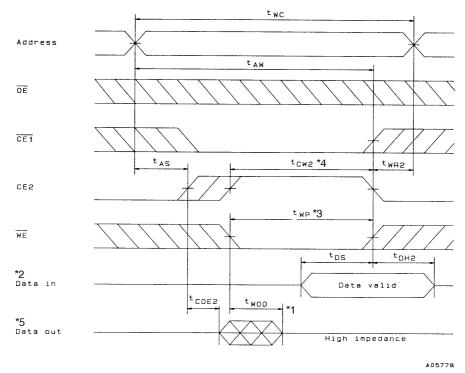




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## Write Cycle (3): CE2 Write \*6

Write Cycle (2):  $\overline{\text{CE1}}$  Write \*6



#### Notes: 1. Hold WE high during the read cycle.

- Applications must not apply reverse phase signals to the D<sub>OUT</sub> pins when those pins are in the output state.
   The time tWP is the period when CE1 and WE are low and CE2 is high, and is defined as the time from the fall of WE until either CE1 or WE rises, or CE2 falls, whichever occurs first.
- 4. The times t<sub>CW1</sub> and t<sub>CW2</sub> are periods when CE1 and WE are low and CE2 is high. They are defined as the times from the fall of CE1 or the rise of CE2 to the rise of CE1 and WE, or the fall of CE2, whichever occurs first.
- 5. The D<sub>OUT</sub> pins will be in the high-impedance state if either  $\overline{OE}$  is high,  $\overline{CE1}$  is high, CE2 is low, or  $\overline{WE}$  is low.
- 6.  $\overline{OE}$  must be held either at V<sub>IH</sub> or V<sub>IL</sub> during the write cycle.
- 7. The D<sub>OUT</sub> pins have the same phase as the write cycle write data.

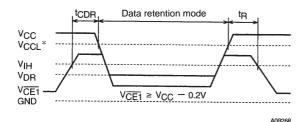
## LC3564B, BS, BM, BT-70/10

#### Data Retention Characteristics at Ta = -40 to $+85^{\circ}C$

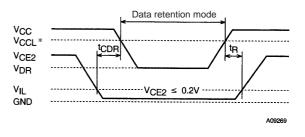
Parameter	Symbol	Conditions		Ratings			Unit
Farameter	Symbol			min	typ	max	
Data retention supply voltage	$V_{DR}$	$\label{eq:VCE2} \begin{split} V_{CE2} &\leq 0.2 \text{ V or} \\ V_{\overline{CE1}} &\geq V_{CC} - 0.2 \text{ V},  V_{CE2} &\geq V_{CC} - 0.2 \text{ V} \end{split}$		2.0		5.5	μΑ
Data retention supply current	I <sub>CCDR</sub>	$\label{eq:VCC} \begin{split} V_{CC} &= 3V, \ V_{CE2} \leq 0.2 \ V, \\ or \ V_{\overline{CE1}} \geq V_{CC} - 0.2 \ V, \\ V_{CE2} \geq V_{CC} - 0.2 \ V \end{split}$	Ta ≤ 70°C			0.8	
			Ta ≤ 85°C			2.5	μA
Chip enable setup time	t <sub>CDR</sub>			0			ns
Chip enable hold time	t <sub>R</sub>			t <sub>RC</sub> *			ns

Note \*: t<sub>RC</sub> is the read cycle time.

## Data Retention Waveforms (1): CE1 Control



## Data Retention Waveforms (2): CE2 Control



Note \*: In 5-V operation: 4.5 V In 3-V operation: 2.7 V

#### Notes on Circuit Design

When actually design a circuit using these devices, take the following points into consideration and design the circuit so that none of the maximum rating items are ever exceeded.

- Variations in the supply voltage
- Variations in the electrical characteristics of components such as semiconductor devices, resistors, and capacitors.
- Ambient temperature
- · Variations in input and clock signals
- Possible application of abnormal pulses
- Also, these devices must be operated within the ranges stipulated in the allowable operating ranges.

If CMOS IC input pins are left open, intermediate potential input voltages may occur leading to incorrect operation due to through currents or other phenomenon. Applications must handle unused input pins appropriately.

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