

ON Semiconductor

Is Now

onsemi™

To learn more about onsemi™, please visit our website at
www.onsemi.com

onsemi and **onsemi** and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi** product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner. Other names and brands may be claimed as the property of others.

NCS5650

2 Amp PLC Line Driver

The NCS5650 is a high efficiency, Class A/B, low distortion power line driver. Its design is optimized to accept a signal from a Power Line Carrier modem. The output stage is designed to drive up to 2 A peak into an isolation transformer or simple coil coupling to the mains. At output current of 1.5 A, the output voltage is guaranteed to swing within 1 V or less of either rail giving the user improved SNR. Power supply options are single-sided 6 V to 12 V and dual balanced ± 3.0 V to ± 6.0 V. The input stage contains an operational amplifier which can be configured as a unity gain follower buffer or used to provide the first stage of a 4-pole low pass filter. In addition the NCS5650 offers a current limit programmable with a single resistor, R_{Limit} , together with a current limit flag.

The device provides two independent thermal flags with hysteresis: a thermal warning flag to let the user know the internal junction temperature has reached a user programmable thermal warning threshold and a thermal error flag that indicates the internal junction temperature has exceeded 150°C. In shutdown mode the NCS5650 output goes into a high-impedance state. The NCS5650 comes in a 20 lead QFN package (4x4x1mm) with an exposed thermal pad for enhanced thermal reliability.

Features

- Rail-to-Rail Drop of Only ± 1 V with $I_{\text{out}} = 1.5$ A
- V_{CC} : Single-Sided (6 V to 12 V) or Dual-Balanced ± 6.0 V
- Flexible 4th-Order Filtering
- Current-Limit Set with One Resistor
- Diagnostic Flags Level Shifted to V_{uc} to Simplify Interface with External MCU
 - ◆ Thermal Warning Flag with Flexible Threshold Setting
 - ◆ Thermal Error flag and Shutdown
 - ◆ Overcurrent Flag
- Enable/Shutdown Control
- Extended Junction Temperature Range: -40°C to $+125^{\circ}\text{C}$
- Small Package: 20-pin 4x4x1mm QFN with Exposed Thermal Pad
- Optimized for Operation in the Cenelec A to D Frequency Band
- This is a Pb-Free Device

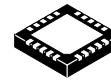
Typical Applications

- Power Line Communication Driver in AMM and AMR Metering Systems
- Valve, Actuator, and Motor Driver
- Audio



ON Semiconductor®

<http://onsemi.com>

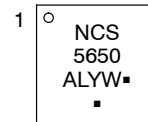


1 20

QFN20
CASE 485E

MARKING DIAGRAM

20



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

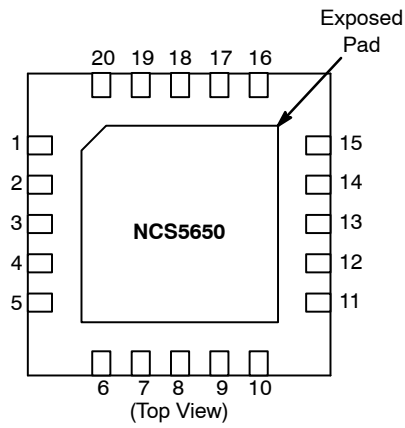
(*Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping
NCS5650MNTXG	QFN20 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part or orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCS5650



NOTE: The Exposed Pad (EP) on package bottom must be attached to a heat-sinking conduit. The Exposed Pad must be electrically connected to V_{EE} .

Figure 1. Pin Connections

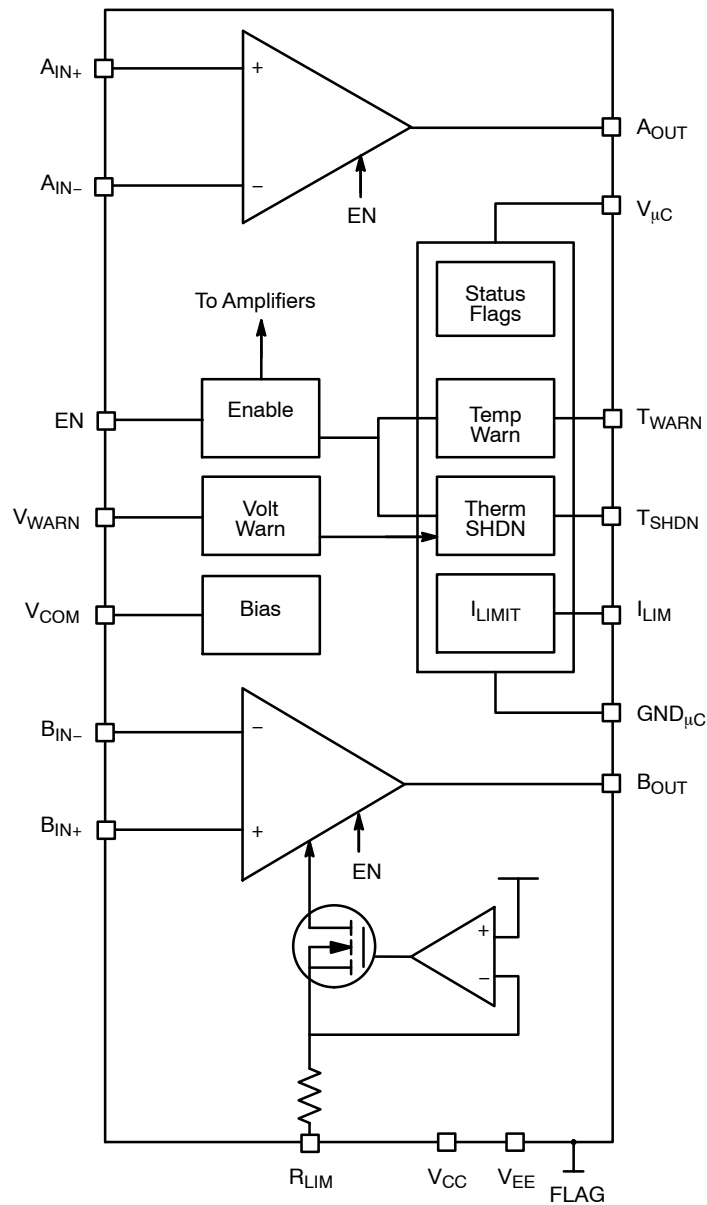


Figure 2. NCS5650 Block Diagram

NCS5650

PIN DESCRIPTION

Pin#	Symbol	Pin Function
1	Enable	Enable/ Shutdown Input (Low = Enable)
2	V _{com}	Virtual Common at (V _{CC} - V _{EE})/2; not to be used as a reference. (See Note 1 Below)
3	AIN+	Positive (+) Input of Op Amp A
4	AIN-	Negative (-) Input of Op Amp A
5	Amp A Out	Output of Op Amp A
6	V _{CC}	Positive supply for amplifiers
7	V _{CC}	Positive supply for amplifiers
8	Amp B Out	Output of Op Amp B
9	Amp B Out	Output of Op Amp B
10	V _{EE}	Negative supply for amplifiers
11	V _{EE}	Negative supply for amplifiers
12	BIN-	Negative (-) Input of Op Amp B
13	BIN+	Positive (+) Input of Op Amp B
14	V-Warn	Thermal Warning Temp is set by a voltage determined by the ratio of two resistors (see Figure 8).
15	R-Limit	Output B Current Limit Set Resistor (R-Limit) to Pin 10, V _{EE} + 1.92 V
16	I _{LIM} flag	Current Limit Flag (High indicates Output Current ≥ limit set by R-Limit)
17	TSD flag	Thermal Shutdown Flag (High indicates Junction Temperature ≥ 150°C)
18	TW flag	Thermal Warning Flag (High indicates Junction Temperature ≥ threshold set by V-Warn)
19	V _{μC}	Digital supply for logic flag thresholds
20	GND _{μC}	Digital ground for logic flag thresholds
21	Exposed Pad	The exposed pad should be connected to the lowest voltage potential in the circuit.

- The principal purpose of pin 2 is to facilitate the implementation of the 4th-order lowpass filter when operating on single-sided supply by providing a virtual common at mid-supply. When operating on dual balanced supplies, Pin 2 must be left floating and the external common of the dual supplies should be used for the filter implementation.

MAXIMUM RATINGS

Symbol	Rating	Value	Unit	
V _S	Supply Voltage (V _{CC} to V _{EE})	13.2	V	
V _{ICR}	Input Common Mode Voltage Range	(V _{EE} - 0.3 V, V _{CC} + 0.3 V) < V _S	V	
T _J	Maximum Junction Temperature (Operating Range -40°C to 125°C)	160	°C	
T _{stg}	Storage Temperature	-65 to 165	°C	
	Mounting Temperature (Infrared or Convection - 30 sec)	260		
MSL	Moisture Sensitivity Level	Level 1		
θ _{JA}	Thermal Resistance 20-Pin QFN with Exposed Thermal Pad (With exposed thermal pad soldered to 9 in ² of 2 oz Cu PCB area (62 mil thick board) using 14 vias each with an 18 mil diameter and 1.5 mils Cu walls. See Application Information.)	33	°C/W	
	Logic control pins	Enable, R _{LIMIT} , I _{LIM} , TSD, TW, V _{μC}	5.5	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NCS5650

ELECTRICAL CHARACTERISTICS $V_S = 12\text{ V}$ All limits apply over the temperature range, $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise noted. Total supply $V_S = V_{CC} - V_{EE}$.

Parameter	Symbol	Condition	NCS5650			Units
			Min	Typ	Max	
INPUT OPERATIONAL AMPLIFIER (Op Amp A)						
Offset Voltage						
Input Offset Voltage	V_{OS}	$V_{CC} = +12\text{ V}, V_{EE} = 0\text{ V}$		± 3	± 10	mV
Offset vs Power Supply	PSRR	$V_{CC} = +6\text{ V}, V_{EE} = -6\text{ V}$		25	150	$\mu\text{V/V}$
Input Bias Current (Note 2)	I_B				1	nA
Input Voltage Noise Density	e_n	$f = 1\text{ kHz}, V_{IN} = \text{GND},$ $\text{BW} = 131\text{ kHz}$		250		$\text{nV}/\sqrt{\text{Hz}}$
Input Voltage Range						
Common-Mode Voltage Range	V_{CM}		$V_{EE} - 0.1$		$V_{CC} - 3$	V
Common-Mode Rejection Ratio	CMRR	$V_{EE} - 0.1 \leq V_{CM} \leq V_{CC} - 3$	70	85		dB
Input Impedance						
Differential				0.2 1.5		$\text{G}\Omega$ pF
Common-Mode				0.2 3		$\text{G}\Omega$ pF
Open-Loop Gain (Note 2)		$R_L = 500\ \Omega$	80	100		dB
Frequency Response						
Gain Bandwidth Product	GBW			80		MHz
Full Power Bandwidth (Note 2)		$G = +5, V_{out} = 11\text{ V}_{PP}$	200	1.5		MHz
Slew Rate	SR			60		$\text{V}/\mu\text{s}$
Total Harmonic Distortion + Noise	THD+N	$G = +1, R_L = 500\ \Omega, V_O = 8\text{ V}_{PP}, f =$ $1\text{ kHz}, C_{in} = 220\ \mu\text{F}, C_{out} = 330\ \mu\text{F}$		0.015		%
		$G = +1, R_L = 50\ \Omega, V_O = 8\text{ V}_{PP}, f =$ $100\text{ kHz}, C_{in} = 220\ \mu\text{F}, C_{out} = 330\ \mu\text{F}$		0.023		
Output						
Voltage Output Swing from Rail		$V_{CC} = +12\text{ V}, V_{EE} = 0\text{ V}$				
From Positive Rail	V_{OH}	$R_L = 500\ \Omega$ to $V_{CC}/2$		0.3	1	V
From Negative Rail	V_{OL}	$R_L = 500\ \Omega$ to $V_{CC}/2$		0.3	1	V
Short-Circuit Current	I_{SC}			280		mA
Output Impedance	Z_O	Closed Loop $G = +4, f = 100\text{ kHz}$		0.25		Ω
Capacitive Load Drive	C_{LOAD}			100		pF

OUTPUT OPERATIONAL AMPLIFIER (Op Amp B)

Offset Voltage						
Input Offset Voltage	V_{OS}	$V_{CC} = +12\text{ V}, V_{EE} = 0\text{ V}$		± 3	± 10	mV
Offset vs Power Supply	PSRR	$V_{CC} = +12\text{ V}, V_{EE} = 0\text{ V}$		25	150	$\mu\text{V/V}$
Input Bias Current (Note 2)	I_B				1	nA
Input Voltage Noise Density	e_n	$f = 1\text{ kHz}, V_{IN} = \text{GND},$ $\text{BW} = 131\text{ kHz}$		125		$\text{nV}/\sqrt{\text{Hz}}$
Input Voltage Range						
Common-Mode Voltage Range	V_{CM}		$V_{EE} - 0.1$		$V_{CC} - 3$	V
Common-Mode Rejection Ratio	CMRR	$V_{EE} - 0.1 \leq V_{CM} \leq V_{CC} - 3$	70	85		dB

2. Guaranteed by characterization or design.
3. Formula accuracy requires a resistor with $\pm 1\%$ tolerance.

NCS5650

ELECTRICAL CHARACTERISTICS $V_S = 12\text{ V}$ All limits apply over the temperature range, $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise noted. Total supply $V_S = V_{CC} - V_{EE}$.

Parameter	Symbol	Condition	NCS5650			Units
			Min	Typ	Max	
OUTPUT OPERATIONAL AMPLIFIER (Op Amp B)						
Input Impedance						
Differential				0.2 11		$\text{G}\Omega$ pF
Common-Mode				0.2 22		$\text{G}\Omega$ pF
Open-Loop Gain (Note 2)		$R_L = 5\ \Omega$	80	100		dB
Frequency Response						
Gain Bandwidth Product	GBW			60		MHz
Full Power Bandwidth (Note 2)		$G = +2, V_{out} = 11\text{ V}_{PP}$	200	400		kHz
Slew Rate	SR			70		$\text{V}/\mu\text{s}$
Total Harmonic Distortion + Noise	THD+N	$G = +1, R_L = 50\ \Omega,$ $V_O = 8\text{ V}_{PP}, f = 1\text{ kHz}$		0.015		%
		$G = +1, R_L = 50\ \Omega,$ $V_O = 8\text{ V}_{PP}, f = 100\text{ kHz}$		0.067		
Output						
Voltage Output Swing from Rail		$V_{CC} = +12\text{ V}, V_{EE} = 0\text{ V}$				
From Positive Rail	V_{OH}	$I_{out} = 1.5\text{ A}$ to Mid-Supply		0.7	1	V
From Negative Rail	V_{OL}	$I_{out} = 1.5\text{ A}$ to Mid-Supply		0.4	1	V
Voltage Output Swing from Rail		$V_{CC} = +6\text{ V}, V_{EE} = -6\text{ V}$				
From Positive Rail	V_{OH}	$I_{out} = 1.5\text{ A}$ to GND		0.7	1	V
Negative Rail	V_{OL}	$I_{out} = 1.5\text{ A}$ to GND		0.4	1	V
Output Impedance	Z_O	Closed Loop $G = +1,$ $f = 100\text{ kHz}$		0.065		Ω
Enabled Mode				12		$\text{M}\Omega$
Shutdown Mode						
Capacitive Load Drive	C_{LOAD}			500		nF

BOTH AMPLIFIERS COMBINED

Junction Temperature	T_J					
At Shutdown (Note 2)			+150	+160		$^\circ\text{C}$
At Recovery from Shutdown				+135		$^\circ\text{C}$
Thermal Warning Tolerance		$T_{warning}$ is determined by the ratio of two resistors (see Figure 8) (Note 3)		± 10		$^\circ\text{C}$
Current Limit Tolerance		I-Limit is determined by a single resistor (see Figure 5 text) (Note 3)		± 50		mA
Power Supply						
Operating Voltage Range	V_S	Single-Supply Operation (V_{EE} Tied to System Common)		6 to 12	13.2	V
		Dual Balanced-Supply operation		± 3.0 to ± 6.0		
Quiescent Current	I_Q	$V_{CC} = +6\text{ V}, V_{EE} = -6\text{ V}$		20	40	mA
Enabled Mode				120	150	
Shutdown Mode						
V_{COM}		$V_{CC} = 12\text{ V}, V_{EE} = 0\text{ V}$ Internal resistor divider. Bypass purposes only.	5.8	6.0	6.2	V

2. Guaranteed by characterization or design.
3. Formula accuracy requires a resistor with $\pm 1\%$ tolerance.

NCS5650

ELECTRICAL CHARACTERISTICS $V_S = 12\text{ V}$ All limits apply over the temperature range, $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise noted. Total supply $V_S = V_{CC} - V_{EE}$.

Parameter	Symbol	Condition	NCS5650			Units
			Min	Typ	Max	
LOGIC INPUT/OUTPUT						
Logic/flag Supply Range	$V_{\mu c}$	Logic/flag supply for operation with external MCU	3.0		5.5	V
Reference Point for GND $_{\mu c}$	$V_{g\mu c}$	With Single-Sided Power Supply	V_{EE} (Pins 10 and 11) Connected to System Common			
		With Dual-Balanced Power Supply	Common of Dual Supply Connected to System Common			
Shutdown Input Mode						
Output Enabled	Ve/s LOW	E/S Pin Open or Forced LOW	$V_{g\mu c} - 0.4$		$V_{g\mu c} + 0.8$	V
Output Shutdown	Ve/s HIGH	E/S Pin Forced HIGH	$V_{g\mu c} + 2$		$V_{\mu c}$	V
Output Enabled	Ie/s LOW	E/S Pin LOW		0.1		μA
Output Shutdown	Ie/s HIGH	E/S Pin HIGH		10		μA
Output Shutdown Time				60		ns
Output Enable Time (Note 2)				5	10	μs
All Flag Outputs						
HIGH State			$V_{g\mu c} + 2$			V
LOW State					$V_{g\mu c} + 0.8$	V

2. Guaranteed by characterization or design.
3. Formula accuracy requires a resistor with $\pm 1\%$ tolerance.

APPLICATIONS INFORMATION

Exposed Thermal Pad

The NCS5650 is capable of delivering 1.5 A, into a reactive load. Output signal swing should be kept as high as possible to minimize internal heat generation to keep the internal junction temperature as low as possible. The NCS5650 can swing to within 1 V of either rail without adding distortion. An exposed thermal pad is provided on the bottom of the device to facilitate heat dissipation. Application Note AND8402/D provides considerable details for optimizing the soldering down of the exposed pad. A very good example of the exposed pad implementation is provided in the layout information included with the NCS5650 Demo Board. The demo board implements 14 vias, each with an 18 mil diameter and 1.5 mils Copper walls.

Multi-Feedback Filter (MFB)

CENELEC EN 50065-1 is a European standard for signaling on low-voltage electrical installations in the frequency range 3 kHz to 148.5 kHz. More specifically Part 1 of that specification deals with frequency bands and electromagnetic disturbances introduced into the electrical mains. A practical solution to meet this requirement is to place a 4th-order filter between the output of the modem and the isolation transformer connected to the mains. In this datasheet a MFB filter topology is proposed to help meet the requirements of the CENELEC standard. Four (4) pole filters require two op amps for implementation. The NCS5650 has an input pre-amplifier and an output power amplifier. Therefore only passive components (R's and C's) need to be added. In addition the NCS5650 has a mid-supply virtual common at pin 2 (V_{com}) to facilitate implementation of the filter topology when powered from a single-sided power supply.

Figure 3 below shows the frequency response for each stage and the overall filter.

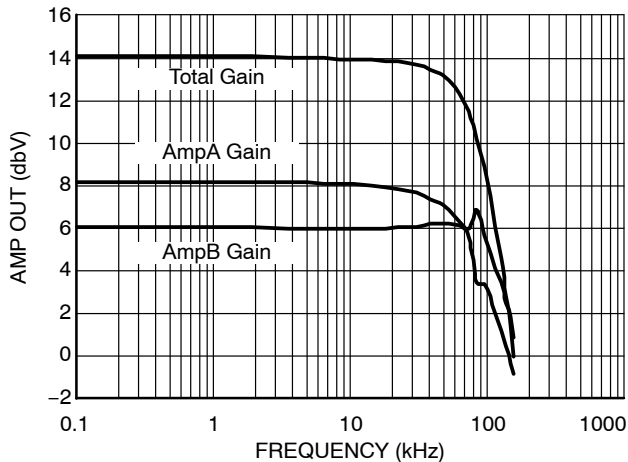


Figure 3. Amplifier Voltage vs. Frequency

Bypassing

Optimal stability and noise rejection will be implemented with power-supply bypassing placed as physically close to the device as possible. A parallel combination of 10 μF and 0.01 μF is recommended (ceramic and tantalum, respectively) for each sensitive point. For either single-supply operation or split supply operation, bypass should be placed directly across V_{CC} to V_{EE}. In addition add bypass from V_{μC} to GND_{μC}. Reference Figure 4.

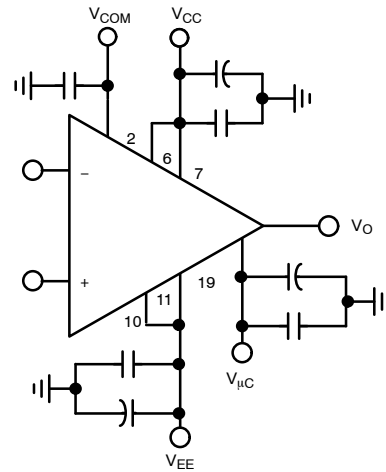


Figure 4.

Current Limit (R-Limit)

The 2 A output current of the NCS5650 can be programmed by the simple addition of a resistor (R_{Limit}) from pin 15 to the lowest potential in the circuit: V_{EE} for balanced supplies, and GND for single supplies (see Figure 5). If the load current tries to exceed the set current limit, the I_{LIM} flag will go logic High signaling the user to take any necessary action. When the current output recovers, the I_{LIM} flag will return to logic Low. The curve in Figure 5 is tolerance typically to ±50 mA. Unlike traditional power amplifiers the NCS5650 current limits functions both when sourcing and sinking current. To calculate the resistance required to program a desired current limit the following equation can be used:

$$I_{LIM} = \frac{1.215}{R_{CL}} \times 8197$$

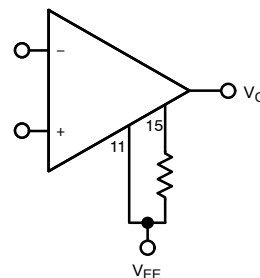


Figure 5.

Figure 6 graphically illustrates the required resistance in ohms to program the current limit.

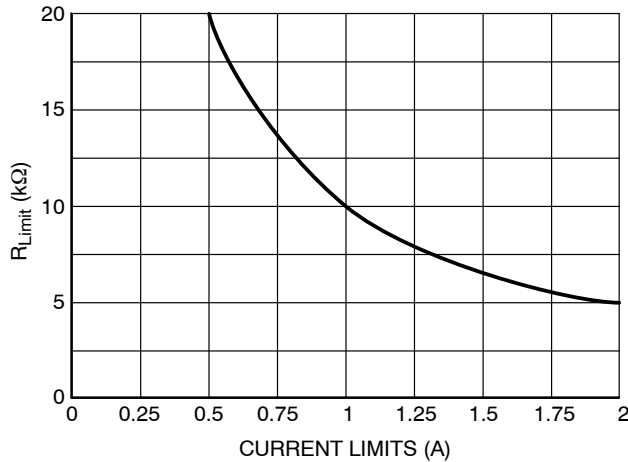


Figure 6.

Thermal Shutdown and Thermal Warning Flag

In the event load conditions cause internal over-heating the amplifier will go into shutdown to prevent damage. Under these conditions pin 17 the TSD flag (Thermal Shut Down) will go logic High. Thermal shutdown takes place at an internal junction temperature of approximately 160°C; the amplifier will recover to the Enabled mode when the junction temperature cools back down to approximately 135°C.

The user has the option to avoid entering into the TSD mode by monitoring the junction temperature via the Thermal Warning feature. Figure 8 shows how the user can select any junction temperature (T_{warn}) in the range 105°C to 145°C by applying the appropriate voltage to pin 14. A simple way to implement this feature is by setting the ratio of a voltage divider between V_{CC} (pins 6,7) and V_{EE} (the negative supply, pin 10 or 11). The voltage ratio required to program the thermal warning of the NCS5650 can be calculated using the following equation:

$$V_{TW} = 6.665 \times 10^{-3} (T_J) + 1.72$$

Figure 8 illustrates the linearity of the internal junction temperature to the required voltage on pin 14 (T_{warn}).

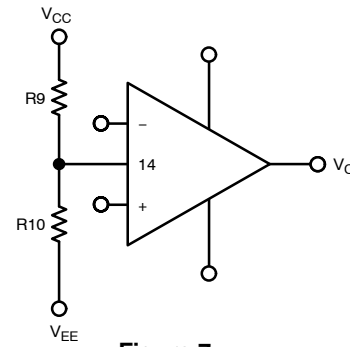


Figure 7.

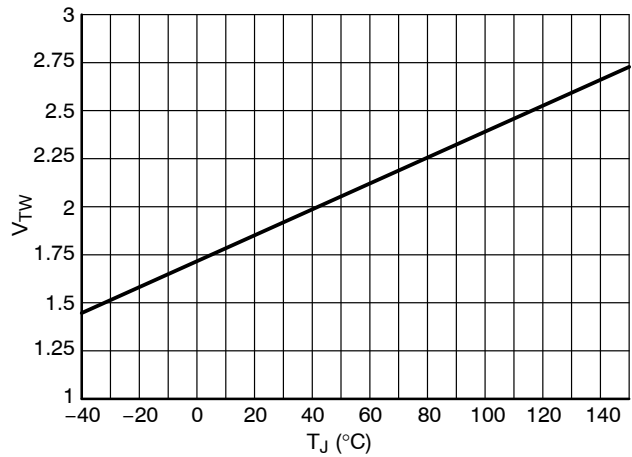


Figure 8.

Virtual Common (V_{com})

The principal purpose of V_{com} is to provide a convenient virtual common for implementing the 4th-order CENELEC filter when operating on single-sided power supply. When operating on balanced split supplies it is recommended to use the power supply common for the filter implementation and to leave V_{com} floating.

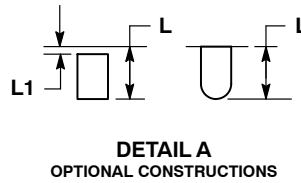
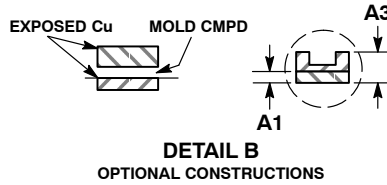
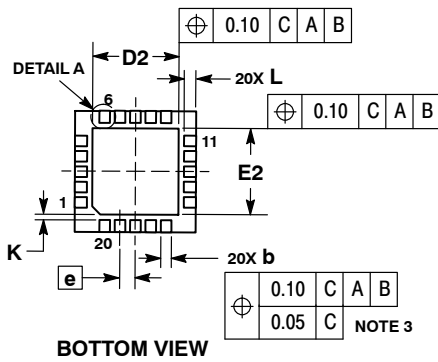
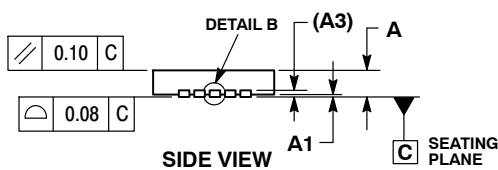
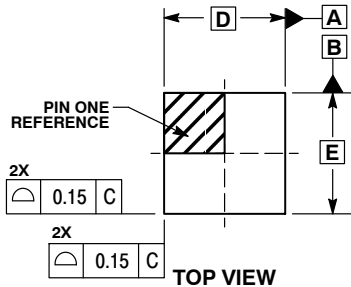
Digital Power Supply GND-Reference and Translators

In many mixed signal applications analog GND and digital GND are not always at the same potential. To minimize GND loop issues, the NCS5650 has a separate GND pin (pin 20) which should be used to reference the digital supply and the warning flags (pins 16, 17, and 18). In most applications this would be the same GND reference used for the PLC modem. Please note that at some point in the application digital GND and analog GND must be tied together.

NCS5650

PACKAGE DIMENSIONS

QFN20, 4x4, 0.5P
CASE 485E-01
ISSUE B

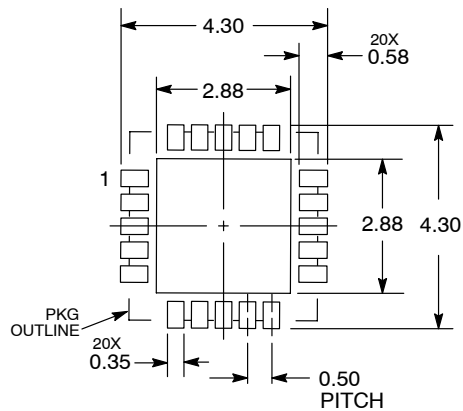


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20	REF
b	0.20	0.30
D	4.00	BSC
D2	2.60	2.90
E	4.00	BSC
E2	2.60	2.90
e	0.50	BSC
K	0.20	REF
L	0.35	0.45
L1	0.00	0.15

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative