HEF4040B

12-stage binary ripple counter

Rev. 10 — 7 December 2021 Product data sheet

1. General description

The HEF4040B is a 12-stage binary ripple counter with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve fully buffered outputs (Q0 to Q11). The counter advances on the HIGH-to-LOW transition of $\overline{CP}$. A HIGH on MR clears all counter stages and forces all outputs LOW, independent of $\overline{CP}$. Each counter stage is a static toggle flip-flop. Inputs are overvoltage tolerant to 15 V. This enables the device to be used in HIGH-to-LOW level shifting applications.

2. Features and benefits

- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Tolerant of slow clock rise and fall time
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Complies with JEDEC standard JESD 13-B
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-B exceeds 200 V
- Specified from -40 °C to +85 °C

3. Applications

- Frequency dividing circuits
- Time delay circuits
- Control counters

4. Ordering information

Table 1. Ordering information

Type number		Package		
	Temperature range	Name	Description	Version
HEF4040BT	-40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

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5. Functional diagram

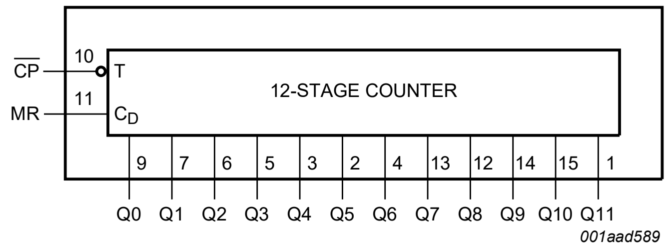


Fig. 1. Functional diagram

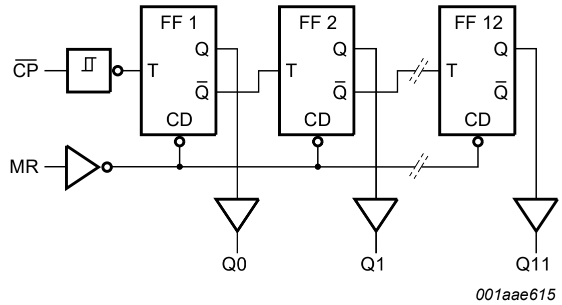


Fig. 2. Logic diagram

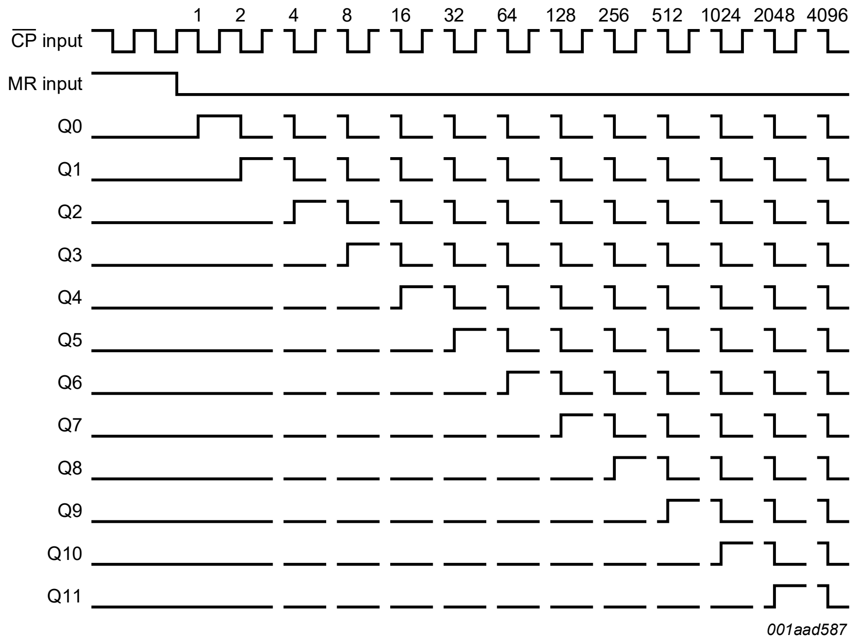


Fig. 3. Timing diagram

6. Pinning information

6.1. Pinning

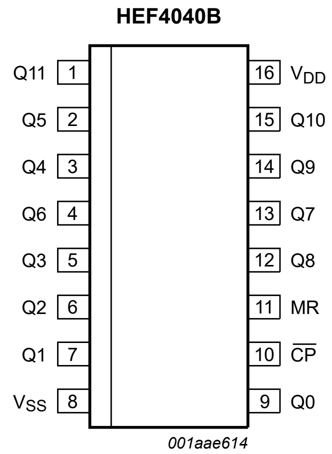


Fig. 4. Pin configuration SOT109-1 (SO16)

6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
V_{SS}	8	ground supply voltage
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q 8, Q9, Q10, Q11	9, 7, 6, 5, 3, 2, 4, 13, 12, 14, 15, 1	parallel output
$\overline{CP}$	10	clock input (HIGH-to-LOW edge-triggered)
MR	11	master reset input (active HIGH)
V_{DD}	16	supply voltage

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I_{IK}	input clamping current	V_I < -0.5 V or V_I > V_{DD} + 0.5 V	-	±10	mA
V_I	input voltage		-0.5	V_{DD} + 0.5	V
I_{OK}	output clamping current	V_O < -0.5 V or V_O > V_{DD} + 0.5 V	-	±10	mA
$I_{I/O}$	input/output current		-	±10	mA
I_{DD}	supply current		-	50	mA
T_{stg}	storage temperature		-65	+150	°C
T_{amb}	ambient temperature		-40	+85	°C
P_{tot}	total power dissipation		-	500	mW
P	power dissipation	per output	-	100	mW

8. Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	V_{DD} = 5 V	-	-	3.75	ms/V
		V_{DD} = 10 V	-	-	0.5	ms/V
		V_{DD} = 15 V	-	-	0.08	ms/V

9. Static characteristics

Table 5. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD}; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = -40 °C		T_{amb} = +25 °C		T_{amb} = +85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\lvert I_O \rvert$ < 1 μA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$\lvert I_O \rvert$ < 1 μA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$\lvert I_O \rvert$ < 1 μA	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$\lvert I_O \rvert$ < 1 μA	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	V_O = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		V_O = 4.6 V	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		V_O = 9.5 V	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		V_O = 13.5 V	15 V	-	-3.6	-	-3.0	-	-2.4	mA
I_{OL}	LOW-level output current	V_O = 0.4 V	5 V	0.52	-	0.44	-	0.36	-	mA
		V_O = 0.5 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V_O = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mA
I_{LI}	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	μA
I_{DD}	supply current	I_O = 0 A	5 V	-	20	-	20	-	150	μA
			10 V	-	40	-	40	-	300	μA
			15 V	-	80	-	80	-	600	μA
C_I	input capacitance		-	-	-	-	7.5	-	-	pF

10. Dynamic characteristics

Table 6. Dynamic characteristics

V_{SS} = 0 V; T_{amb} = 25 °C; unless otherwise specified; for test circuit see Fig. 6.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula [1]	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	$\overline{CP}$ → Q0; see Fig. 5	5 V	78 ns + (0.55 ns/pF)C_L	-	105	210	ns
			10 V	34 ns + (0.23 ns/pF)C_L	-	45	90	ns
			15 V	27 ns + (0.16 ns/pF)C_L	-	35	70	ns
		Qn → Qn + 1	5 V [2]	(0.55 ns/pF)C_L	-	35	70	ns
			10 V [2]	(0.23 ns/pF)C_L	-	15	30	ns
			15 V [2]	(0.16 ns/pF)C_L	-	10	20	ns
		MR → Qn; see Fig. 5	5 V	63 ns + (0.55 ns/pF)C_L	-	90	180	ns
			10 V	29 ns + (0.23 ns/pF)C_L	-	40	80	ns
			15 V	22 ns + (0.16 ns/pF)C_L	-	30	60	ns
t_{PLH}	LOW to HIGH propagation delay	$\overline{CP}$ → Q0; see Fig. 5	5 V	58 ns + (0.55 ns/pF)C_L	-	85	170	ns
			10 V	29 ns + (0.23 ns/pF)C_L	-	40	80	ns
			15 V	22 ns + (0.16 ns/pF)C_L	-	30	60	ns
		Qn → Qn + 1	5 V [2]	(0.55 ns/pF)C_L	-	35	70	ns
			10 V [2]	(0.23 ns/pF)C_L	-	15	30	ns
			15 V [2]	(0.16 ns/pF)C_L	-	10	20	ns
t_t	transition time	see Fig. 5	5 V [3]	10 ns + (1.00 ns/pF)C_L	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF)C_L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C_L	-	20	40	ns
t_W	pulse width	$\overline{CP}$ input HIGH; minimum width; see Fig. 5	5 V		50	25	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
		MR input HIGH; minimum width; see Fig. 5	5 V		40	20	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
t_{rec}	recovery time	MR input; see Fig. 5	5 V		40	20	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
f_{max}	maximum frequency	$\overline{CP}$ input; see Fig. 5	5 V		10	20	-	MHz
			10 V		15	30	-	MHz
			15 V		25	50	-	MHz

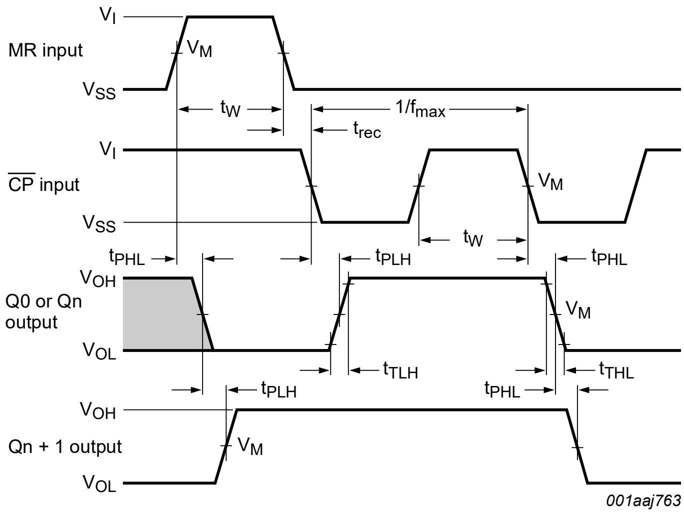
[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).
[2] For loads other than 50 pF at the n^{th} output, use the slope given.
[3] t_t is the same as t_{THL} and t_{TLH}.

Table 7. Dynamic power dissipation P_D

P_D can be calculated from the formulas shown. V_{SS} = 0 V; $t_r = t_f \leq 20$ ns; T_{amb} = 25 °C.

Symbol	Parameter	V_{DD}	Typical formula for P_D (μW)	where:
P_D	dynamic power dissipation	5 V	$P_D = 400 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}{}^2$	f_i = input frequency in MHz, f_o = output frequency in MHz, C_L = output load capacitance in pF, V_{DD} = supply voltage in V, $\Sigma(f_o \times C_L)$ = sum of the outputs.
		10 V	$P_D = 2000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}{}^2$	
		15 V	$P_D = 5200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}{}^2$	

10.1. Waveforms and test circuit

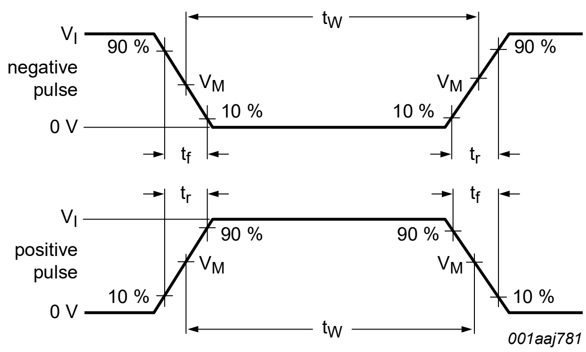


Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.
Measurement points are given in Table 8.

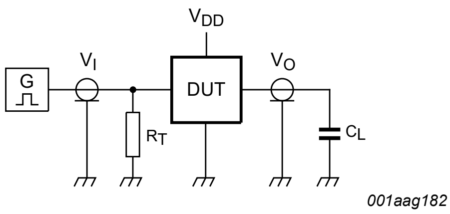
Fig. 5. Waveforms showing the propagation delays, pulse widths, recovery times, maximum clock frequency, and output transition times

Table 8. Measurement points

Supply voltage	Input		Output
V_{DD}	V_I	V_M	V_M
5 V to 15 V	V_{DD} or V_{SS}	$0.5V_{DD}$	$0.5V_{DD}$



a. Input waveforms



b. Test circuit

Test data is given in Table 9.
Definitions test circuit:
C_L = load capacitance, including the jig and probe capacitance;
R_L = load resistance, which should be equal to the output impedance of the pulse generator.

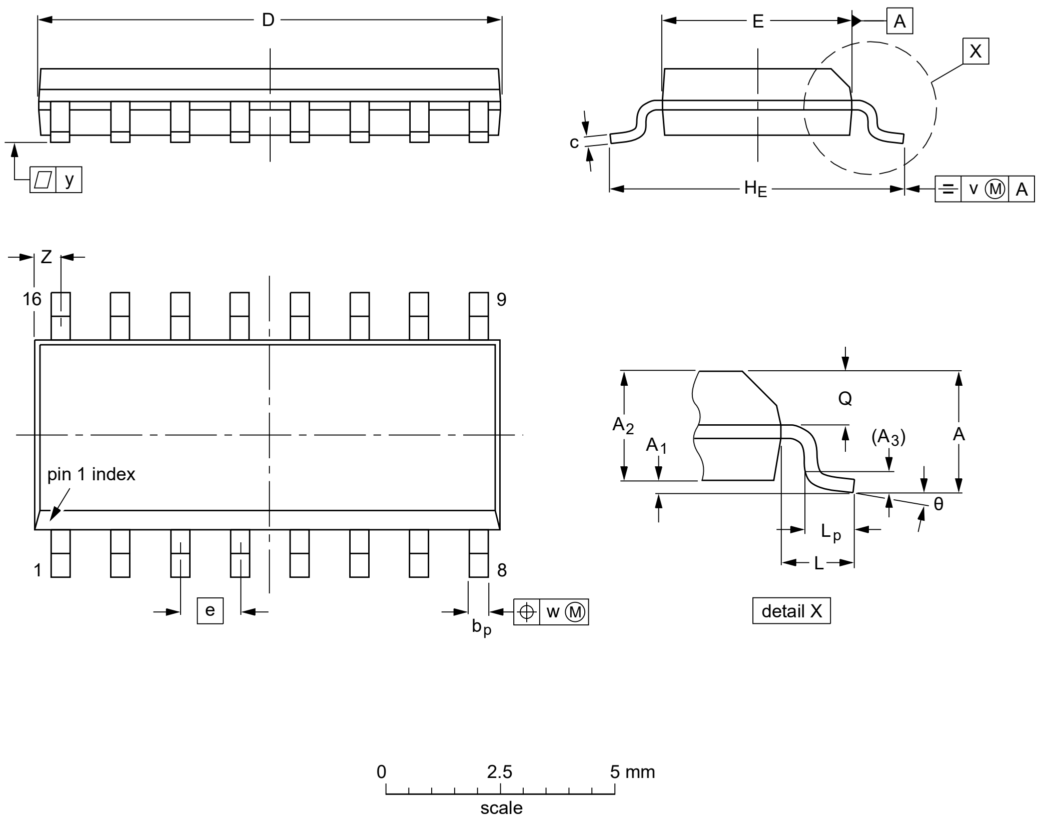
Fig. 6. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load
V_{DD}	V_I	t_r, t_f	C_L
5 V to 15 V	V_{SS} or V_{DD}	≤ 20 ns	50 pF

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

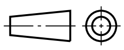
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig. 7. Package outline SOT109-1 (SO16)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4040B v.10	20211207	Product data sheet	-	HEF4040B v.9
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 and Section 2 updated. • Section 12 added.			
HEF4040B v.9	20160323	Product data sheet	-	HEF4040B v.8
Modifications:	• Type number HEF4040BP (SOT38-4) removed.			
HEF4040B v.8	20111117	Product data sheet	-	HEF4040B v.7
Modifications:	• Legal pages updated. • Changes in Section 1 and Section 2.			
HEF4040B v.7	20111010	Product data sheet	-	HEF4040B v.6
HEF4040B v.6	20091125	Product data sheet	-	HEF4040B v.5
HEF4040B v.5	20090709	Product data sheet	-	HEF4040B v.4
HEF4040B v.4	20090304	Product data sheet	-	HEF4040B_CNV v.3
HEF4040B_CNV v.3	19950101	Product specification	-	HEF4040B_CNV v.2
HEF4040B_CNV v.2	19950101	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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