# 74HC4520; 74HCT4520

## **Dual 4-bit synchronous binary counter**

Rev. 4 — 10 May 2016

**Product data sheet** 

### 1. General description

The 74HC4520; 74HCT4520 are dual 4-bit internally synchronous binary counters with two clock inputs (nCP0 and nCP1). They have buffered outputs from all 4 bit positions (nQ0 to nQ3) and an asynchronous master reset input (nMR). The counter advances on the LOW-to-HIGH transition of nCP0 when nCP1 is HIGH. It also advances on the HIGH-to-LOW transition of nCP1 when nCP0 is LOW. Either nCP0 or nCP1 may be used as the clock input to the counter. The other clock input may be used as a clock enable input. A HIGH on nMR, resets the counter (nQ0 to nQ3 = LOW) independent of nCP0 and nCP1. Inputs include clamp diodes. It enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

#### 2. Features and benefits

- Complies with JEDEC standard no. 7A
- Input levels:
  - ◆ For 74HC4520: CMOS level
  - ◆ For 74HCT4520: TTL level
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

## 3. Applications

- Multistage synchronous counting
- Multistage asynchronous counting
- Frequency dividers

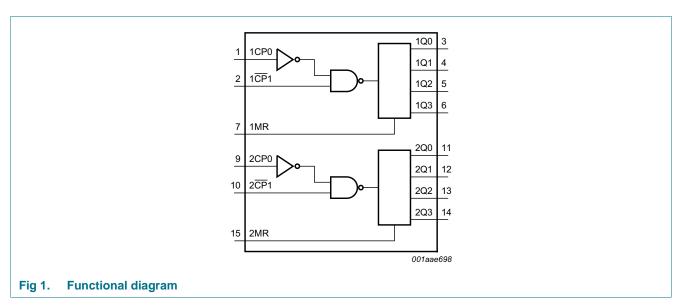


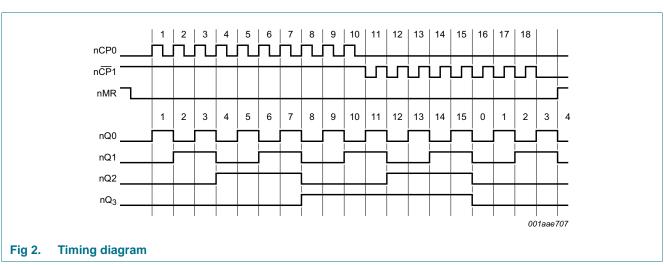
## 4. Ordering information

Table 1. Ordering information

Type number	Package								
	Temperature range	Name	Description	Version					
74HC4520D	-40 °C to +125 °C	SO16	process commercial processes,						
74HCT4520D			body width 3.9 mm						
74HC4520DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads;	SOT338-1					
74HCT4520DB			body width 5.3 mm						
74HC4520PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1					

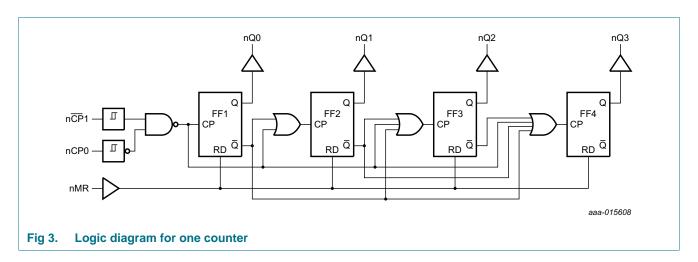
## 5. Functional diagram





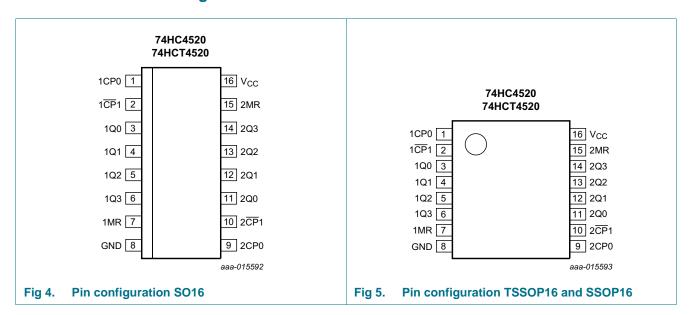
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## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1CP0, 2CP0	1, 9	clock input (LOW-to-HIGH edge-triggered)
1CP1, 2CP1	2, 10	clock input (HIGH-to-LOW edge-triggered)
1Q0 to 1Q3	3, 4, 5, 6	output
1MR, 2MR	7, 15	asynchronous master reset input (active HIGH)
GND	8	ground (0 V)
2Q0 to 2Q3	11, 12, 13, 14	output
V <sub>CC</sub>	16	supply voltage

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## 7. Functional description

Table 3. Function table[1]

nCP0	nCP1	nMR	Mode
<b>↑</b>	Н	L	counter advances
L	<b>\</b>	L	counter advances
$\downarrow$	X	L	no change
X	$\uparrow$	L	no change
$\uparrow$	L	L	no change
Н	<b>\</b>	L	no change
X	X	Н	nQ0 to nQ3 = LOW

<sup>[1]</sup> H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = positive-going transition; ↓ = negative-going transition.

### 8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC}$	supply voltage			-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{CC} + 0.5 \text{ V}$		-	±20	mA
I <sub>OK</sub>	output clamping current	$V_{O} < -0.5 \text{ V or } V_{O} > V_{CC} + 0.5 \text{ V}$		-	±20	mA
I <sub>O</sub>	output current	$V_O = -0.5 \text{ V to } V_{CC} + 0.5 \text{ V}$		-	±25	mA
I <sub>CC</sub>	supply current			-	50	mA
I <sub>GND</sub>	ground current			-50	-	mA
T <sub>stg</sub>	storage temperature			<b>−65</b>	+150	°C
P <sub>tot</sub>	total power dissipation	SO16 and (T)SSOP16 package	<u>[1]</u>	-	500	mW

<sup>[1]</sup> For SO16 package: above 70  $^{\circ}$ C the value of P<sub>tot</sub> derates linearly at 8 mW/K. For (T)SSOP16 packages: above 60  $^{\circ}$ C the value of P<sub>tot</sub> derates linearly at 5.5 mW/K.

## 9. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC4520		74	4HCT452	20	Unit	
			Min	Тур	Max	Min	Тур	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
$V_{I}$	input voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
Vo	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 2.0 V	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5 \text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0 \text{ V}$	-	-	83	-	-	-	ns/V

## 10. Static characteristics

#### Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		–40 °C t	o +85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HC452	20									
V <sub>IH</sub>	HIGH-level	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
	input voltage	V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
$V_{IL}$	LOW-level	V <sub>CC</sub> = 2.0 V	-	8.0	0.5	-	0.5	-	0.5	V
	input voltage	V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level	$V_I = V_{IH}$ or $V_{IL}$				1				1
	output voltage	$I_{O} = -20 \mu A; V_{CC} = 2.0 V$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -20 \mu A; V_{CC} = 4.5 V$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -20 \mu A; V_{CC} = 6.0 V$	5.9	6.0	-	5.9	-	5.9	-	V
		$I_{O} = -4.0$ ; $V_{CC} = 4.5 \text{ V}$	3.98	4.32	-	3.84	-	3.7	-	V
		$I_{O} = -5.2$ ; $V_{CC} = 6.0 \text{ V}$	5.48	5.81	-	5.34	-	5.2	-	V
V <sub>OL</sub>	LOW-level	$V_I = V_{IH}$ or $V_{IL}$								
	output voltage	$I_O = 20 \mu A; V_{CC} = 2.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 4.5 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 6.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
		$I_{O} = 5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	-	0.16	0.26	-	0.33	-	0.4	V
l <sub>l</sub>	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1.0	-	±1.0	μΑ
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	8.0	-	80.0	-	160.0	μΑ

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 Table 6.
 Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT4	520		1						1	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
$V_{IL}$	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub> HIGH-level		$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	I <sub>O</sub> = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		$I_{O} = -4.0 \text{ mA}$	3.98	4.32	-	3.84	-	3.7	-	V
$V_{OL}$	LOW-level	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	I <sub>O</sub> = 20 μA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
l <sub>l</sub>	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±0.1	-	±1.0	-	±1.0	μΑ
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	8.0	-	80.0	-	160.0	μА
$\Delta I_{CC}$	additional	per input pin; $V_I = V_{CC} - 2.1 \text{ V}$ ;	other in	puts at	V <sub>CC</sub> or	GND; V <sub>C</sub>	<sub>C</sub> = 4.5 V	to 5.5 V; I	O = 0 A	
	supply current	pin nCP0, nCP1	-	80	288	-	360	-	392	μΑ
		pin nMR	-	150	540	-	675	-	735	μΑ
Cı	input capacitance		-	3.5	-	-	-	-	-	pF

## 11. Dynamic characteristics

#### Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V);  $C_L = 50 \ pF$  unless otherwise specified; for test circuit, see <u>Figure 7</u>.

Symbol	Parameter	Conditions		25 °C		-40 °C to	+85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HC452	20									
t <sub>pd</sub>	propagation	nCP0 to nQn; see Figure 6	<u>1]</u>							
delay	V <sub>CC</sub> = 2.0 V	-	77	240	-	300	-	360	ns	
		V <sub>CC</sub> = 4.5 V	-	28	48	-	60	-	72	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	24	-	-	-	-	-	ns
		V <sub>CC</sub> = 6.0 V	-	22	41	-	51	-	61	ns
		nCP1 to nQn; see Figure 6	<u>1]</u>							
		V <sub>CC</sub> = 2.0 V	-	77	240	-	300	-	360	ns
		V <sub>CC</sub> = 4.5 V	-	28	48	-	60	-	72	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	24	-	-	-	-	-	ns
		V <sub>CC</sub> = 6.0 V	-	22	41	-	51	-	61	ns

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 Table 7.
 Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V);  $C_L = 50 \text{ pF}$  unless otherwise specified; for test circuit, see Figure 7.

Symbol	Parameter	Conditions		25 °C		-40 °C to	+85 °C	–40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
t <sub>PHL</sub>	HIGH to LOW	nMR to nQn; see Figure 6								1
	propagation	V <sub>CC</sub> = 2.0 V	-	44	150	-	190	-	225	ns
	delay	V <sub>CC</sub> = 4.5 V	-	16	30	-	38	-	45	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	13	-	-	-	-	-	ns
		V <sub>CC</sub> = 6.0 V	-	13	26	-	33	-	38	ns
t <sub>t</sub>	transition	nQn; see Figure 6 [2]								
	time	V <sub>CC</sub> = 2.0 V	-	19	75	-	95	-	110	ns
		V <sub>CC</sub> = 4.5 V	-	7	15	-	19	-	22	ns
		V <sub>CC</sub> = 6.0 V	-	6	13	-	16	-	19	ns
$t_W$	pulse width	nCP0, nCP1 HIGH or LOW; see Fi	gure 6	<u> </u>						
		V <sub>CC</sub> = 2.0 V	80	22	-	100	-	120	-	ns
		V <sub>CC</sub> = 4.5 V	16	8	-	20	-	24	-	ns
		V <sub>CC</sub> = 6.0 V	14	6	-	17	-	20	-	ns
		nMR HIGH; see Figure 6								
		V <sub>CC</sub> = 2.0 V	120	39	-	150	-	180	-	ns
		V <sub>CC</sub> = 4.5 V	24	14	-	30	-	36	-	ns
		V <sub>CC</sub> = 6.0 V	20	11	-	26	-	31	-	ns
t <sub>rec</sub>	recovery time	nMR to nCP0, nCP1; see Figure 6								
		V <sub>CC</sub> = 2.0 V	0	-28	-	0	-	0	-	ns
		V <sub>CC</sub> = 4.5 V	0	-10	-	0	-	0	-	ns
		V <sub>CC</sub> = 6.0 V	0	-8	-	0	-	0	-	ns
t <sub>su</sub>	set-up time	nCP0 to nCP1; nCP1 to nCP0; see	Figu	<u>e 6</u>						
		V <sub>CC</sub> = 2.0 V	80	14	-	100	-	120	-	ns
		V <sub>CC</sub> = 4.5 V	16	5	-	20	-	24	-	ns
		V <sub>CC</sub> = 6.0 V	14	4	-	17	-	20	-	ns
f <sub>max</sub>	maximum	nCP0, nCP1; see Figure 6								
	frequency	V <sub>CC</sub> = 2.0 V	6	19	-	4.8	-	4	-	MHz
		V <sub>CC</sub> = 4.5 V	30	58	-	24	-	20	-	MHz
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	68	-	-	-	-	-	MHz
		V <sub>CC</sub> = 6.0 V	35	69	-	28	-	24	-	MHz
C <sub>PD</sub>	power dissipation capacitance	$V_I = GND \text{ to } V_{CC}; V_{CC} = 5 \text{ V};$ [3] $f_i = 1 \text{ MHz}$	-	29	-	-	-	-	-	pF

 Table 7.
 Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V);  $C_L = 50 \text{ pF}$  unless otherwise specified; for test circuit, see Figure 7.

Symbol	Parameter	Conditions		25 °C		-40 °C to	+85 °C	–40 °C to	+125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HCT4	520									
t <sub>pd</sub>	propagation	nCP0 to nQn; see Figure 6 [1]								
	delay	V <sub>CC</sub> = 4.5 V	-	28	53	-	66	-	80	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	24	-	-	-	-	-	ns
		nCP1 to nQn; see Figure 6								-
		V <sub>CC</sub> = 4.5 V	-	25	53	-	66	-	80	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	24	-	-	-	-	-	ns
t <sub>PHL</sub>	HIGH to LOW	nMR to nQn; see Figure 6							1	ı
	propagation	V <sub>CC</sub> = 4.5 V	-	16	35	-	44	-	53	ns
delay		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	13	-	-	-	-	-	ns
t <sub>t</sub> transition time		nQn; see Figure 6 [2]								
		V <sub>CC</sub> = 4.5 V	-	7	15	-	19	-	22	ns
t <sub>W</sub>	pulse width	nCP0, nCP1 HIGH or LOW; see Figure 6								
		V <sub>CC</sub> = 4.5 V	20	10	-	25	-	30	-	ns
		nMR HIGH; see Figure 6								
		V <sub>CC</sub> = 4.5 V	20	12	-	25	-	30	-	ns
t <sub>rec</sub>	recovery time	nMR to nCP0, nCP1; see Figure 6			•					
		V <sub>CC</sub> = 4.5 V	0	-8	-	0	-	0	-	ns
t <sub>su</sub>	set-up time	nCP0 to nCP1; nCP1 to nCP0; see	Figu	re 6	•					
		V <sub>CC</sub> = 4.5 V	16	6	-	20	-	24	-	ns
f <sub>max</sub>	maximum	nCP0, nCP1; see Figure 6			•					
	frequency	V <sub>CC</sub> = 4.5 V	30	58	-	24	-	20	-	MHz
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	64	-	-	-	-	-	MHz
C <sub>PD</sub>	power dissipation capacitance	$V_I = GND \text{ to } V_{CC} - 1.5 \text{ V};$ $V_{CC} = 5 \text{ V}; f_i = 1 \text{ MHz}$	-	24	-	-	-	-	-	pF

<sup>[1]</sup>  $t_{pd}$  is the same as  $t_{PHL}$  and  $t_{PLH}$ .

[3]  $C_{PD}$  is used to determine the dynamic power dissipation (P<sub>D</sub> in  $\mu$ W):

 $P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \sum (C_L \times V_{CC}{}^2 \times f_o)$  where:

 $f_i$  = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

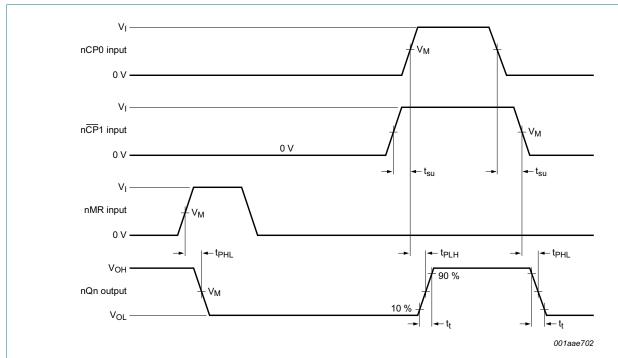
V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

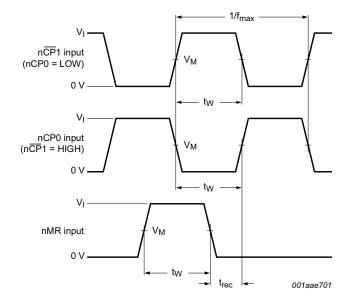
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

<sup>[2]</sup>  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .

### 12. Waveforms



a. nCP0 and nCP1 set-up times, propagation delays and output transition times



b. nMR recovery time, minimum nCP0, nCP1, nMR pulse widths and maximum frequency Measurement points are given in <u>Table 8</u>.
 The logic levels V<sub>OH</sub> and V<sub>OL</sub> are typical output voltage levels that occur with the output load.

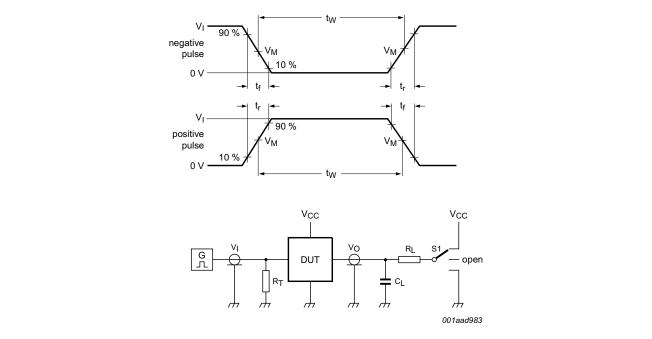
Fig 6. Waveforms showing measurements for switching times

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Table 8. Measurement points

Туре	Input	Output	
	V <sub>M</sub>	V <sub>I</sub>	V <sub>M</sub>
74HC4520	$0.5 \times V_{CC}$	GND to V <sub>CC</sub>	$0.5 \times V_{CC}$
74HCT4520	1.3 V	GND to 3 V	1.3 V



Test data is given in Table 9.

Test circuit definitions:

 $R_T$  = Termination resistance should be equal to output impedance  $Z_0$  of the pulse generator

C<sub>L</sub> = Load capacitance including jig and probe capacitance

 $R_L$  = Load resistance.

S1 = Test selection switch

Fig 7. Test circuit for measuring switching times

Table 9. Test data

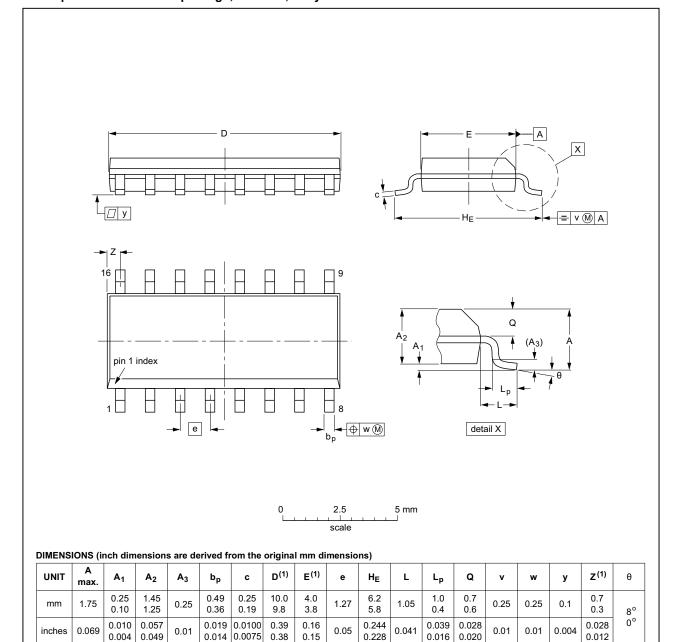
Туре	Input		_oad		S1 position
	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	CL	R <sub>L</sub>	t <sub>PHL</sub> , t <sub>PLH</sub>
74HC4520	GND to V <sub>CC</sub>	6 ns	15 pF, 50 pF	1 kΩ	open
74HCT4520	GND to 3 V	6 ns	15 pF, 50 pF	1 kΩ	open

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## 13. Package outline

#### SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



#### Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

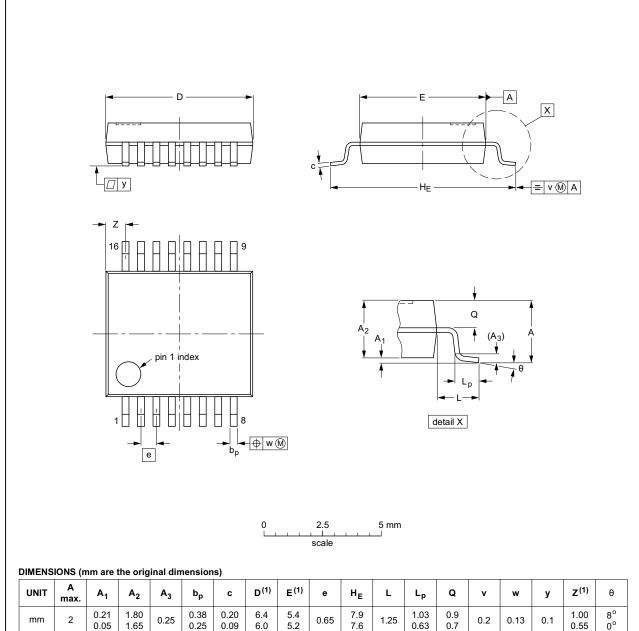
OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT109-1	076E07	MS-012			<del>99-12-27</del> 03-02-19

Fig 8. Package outline SOT109-1 (SO16)

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SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	<b>A</b> <sub>3</sub>	b <sub>p</sub>	C	D <sup>(1)</sup>	E <sup>(1)</sup>	е	HE	L	Lp	Q	v	w	у	Z <sup>(1)</sup>	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

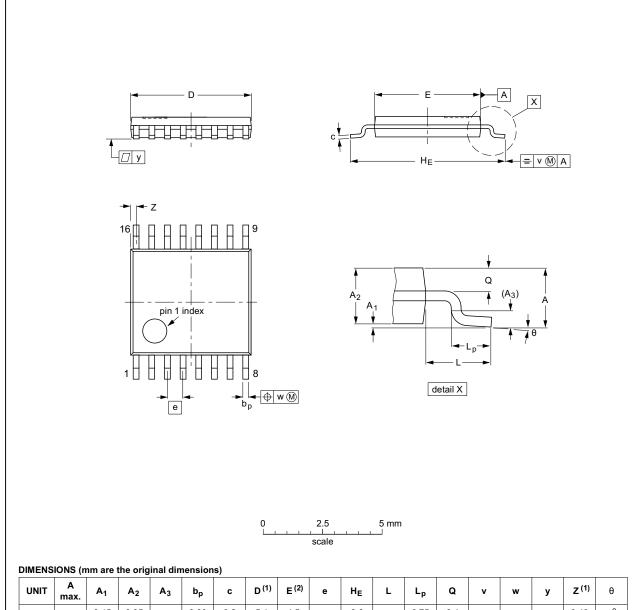
OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT338-1		MO-150			<del>99-12-27</del> 03-02-19

Package outline SOT338-1 (SSOP16)

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TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



_							-,												
	UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	bp	С	D (1)	E (2)	е	HE	L	Lp	Q	v	w	у	Z <sup>(1)</sup>	θ
	mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

#### Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT403-1		MO-153				<del>99-12-27</del> 03-02-18	

Fig 10. Package outline SOT403-1 (TSSOP16)

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## 14. Abbreviations

#### Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model
TTL	Transistor-Transistor Logic

## 15. Revision history

### Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes				
74HC_HCT4520 v.4	20160510	Product data sheet	-	74HC_HCT4520 v.3				
Modifications:	Type numbers 74HC4520N and 74HCT4520N (SOT38-4) removed.							
74HC_HCT4520 v.3	20141204	Product data sheet	-	74HC_HCT4520_CNV v.2				
Modifications:		<ul> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> </ul>						
	<ul> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>							
74HC_HCT4520_CNV v.2	19930927	Product specification	-	-				

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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## 74HC4520; 74HCT4520

#### **Dual 4-bit synchronous binary counter**

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## 74HC4520; 74HCT4520

## **Nexperia**

**Dual 4-bit synchronous binary counter** 

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