

# 74HC590

## 8-bit binary counter with output register; 3-state

Rev. 4 — 14 March 2022

Product data sheet

### 1. General description

The 74HC590 is an 8-bit binary counter with a storage register and 3-state outputs. The storage register has parallel (Q0 to Q7) outputs. The binary counter features master reset counter ( $\overline{MRC}$ ) and count enable ( $\overline{CE}$ ) inputs. The counter and storage register have separate positive edge triggered clock (CPC and CPR) inputs. If both clocks are connected together, the counter state is always one count ahead of the register. Internal circuitry prevents clocking from the clock enable. A ripple carry output ( $\overline{RCO}$ ) is provided for cascading. Cascading is accomplished by connecting  $\overline{RCO}$  of the first stage to  $\overline{CE}$  of the second stage. Cascading for larger count chains can be accomplished by connecting  $\overline{RCO}$  of each stage to the counter clock (CPC) input of the following stage. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

### 2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- CMOS input levels
- Counter and register have independent clock inputs
- Counter has master reset
- Multiple package options
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101C exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

### 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC590D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC590PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC590BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

### 4. Functional diagram

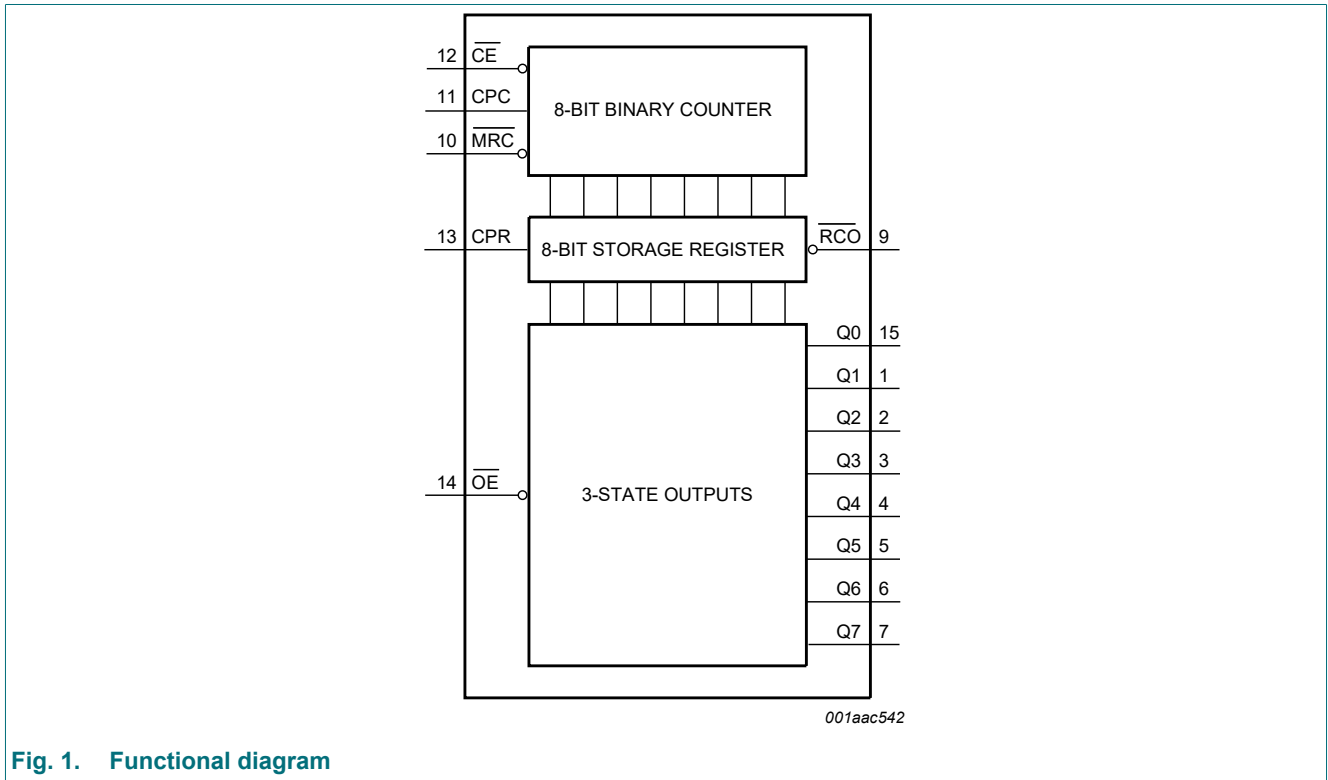


Fig. 1. Functional diagram

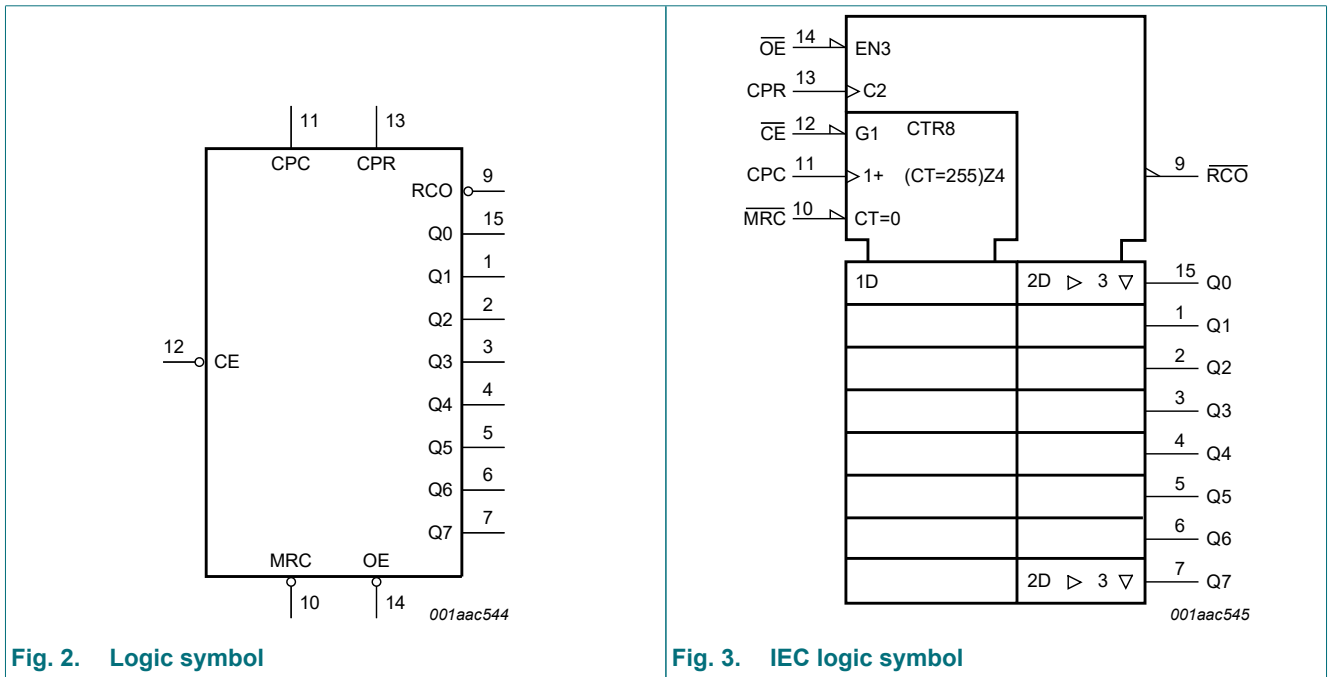


Fig. 2. Logic symbol

Fig. 3. IEC logic symbol

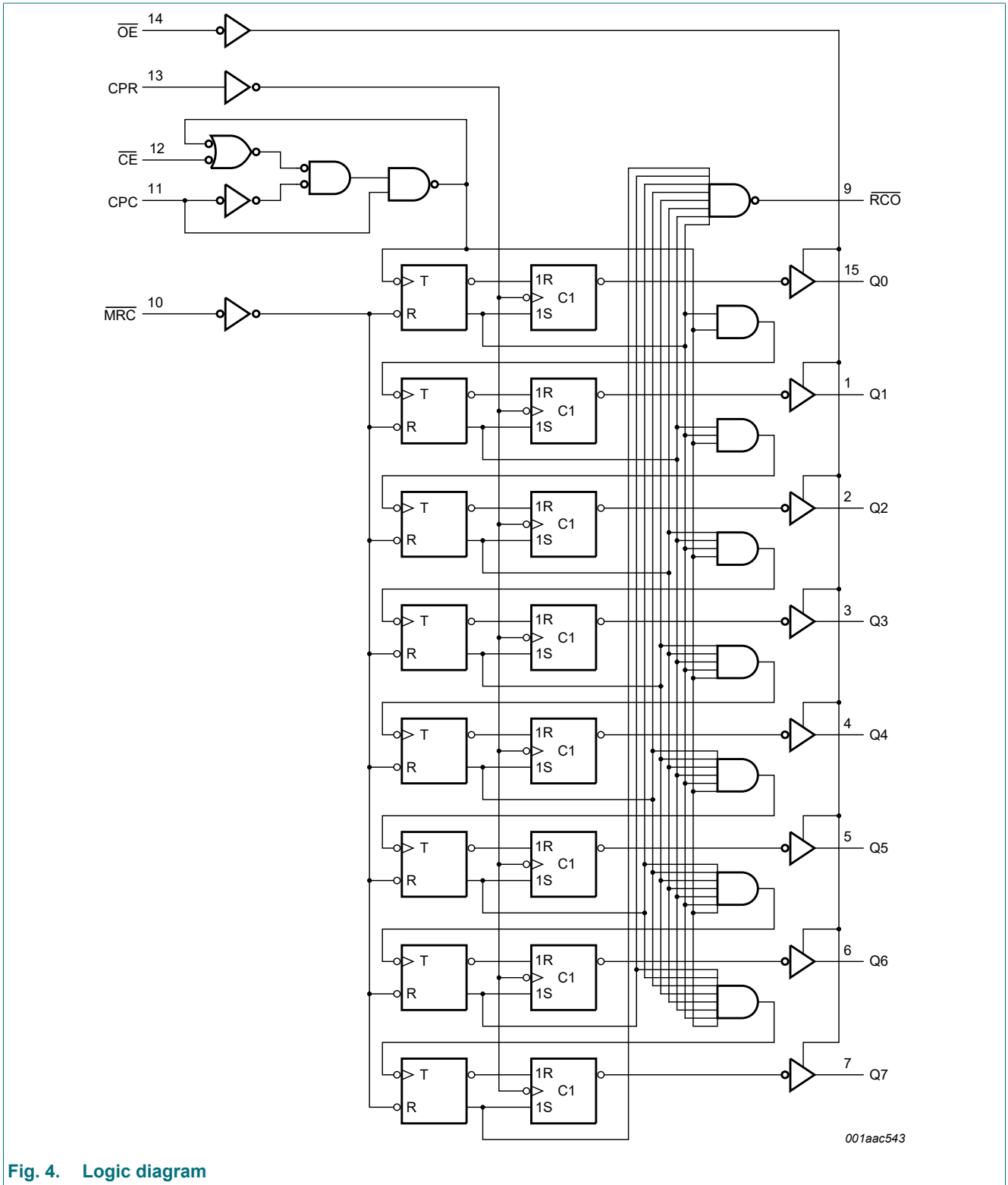
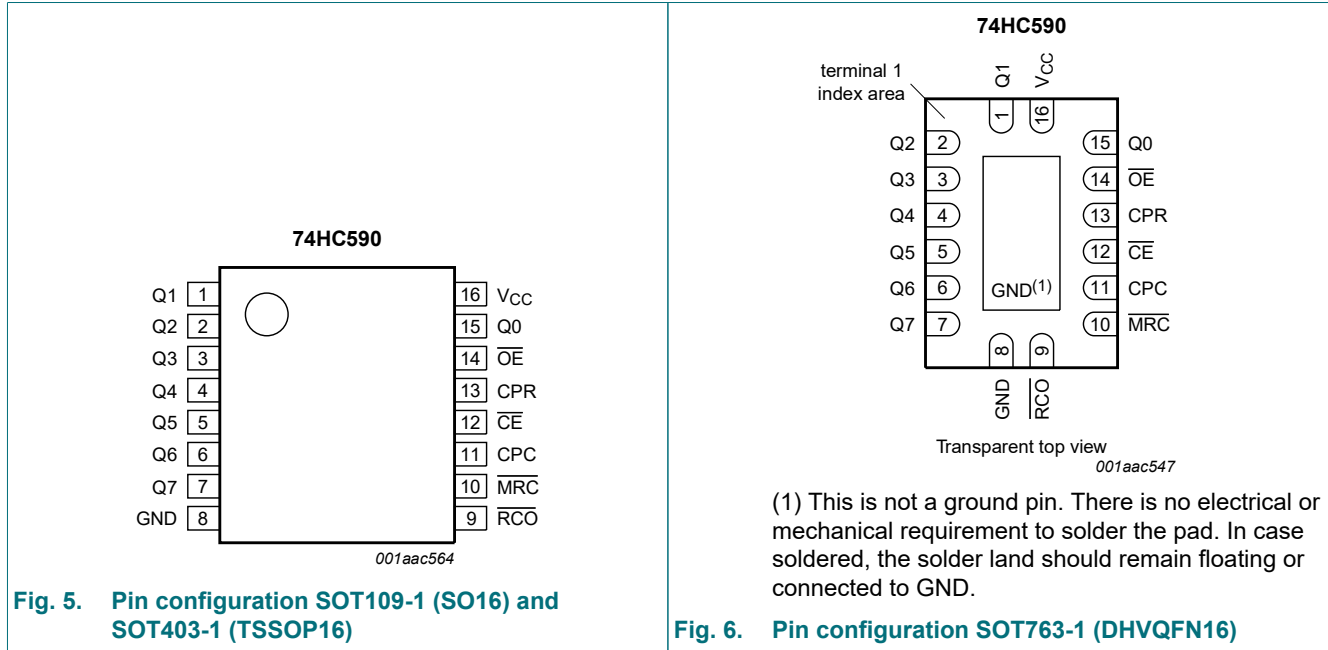


Fig. 4. Logic diagram

## 5. Pinning information

### 5.1. Pinning



### 5.2. Pin description

Table 2. Pin description

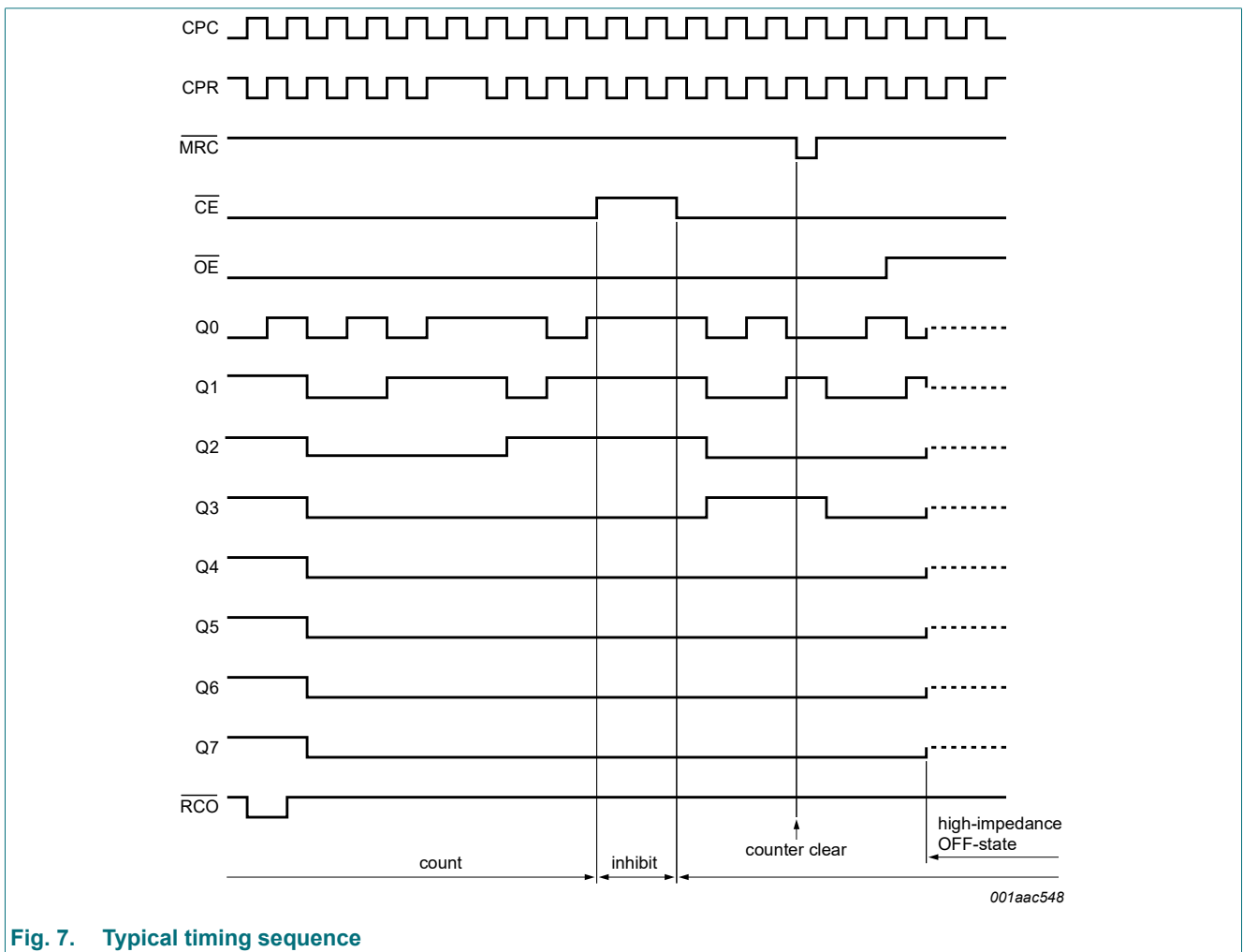
Symbol	Pin	Description
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	15, 1, 2, 3, 4, 5, 6, 7	parallel data output
GND	8	ground (0 V)
$\overline{\text{RCO}}$	9	ripple carry output (active LOW)
$\overline{\text{MRC}}$	10	master reset counter input (active LOW)
CPC	11	counter clock input (active HIGH)
$\overline{\text{CE}}$	12	count enable input (active LOW)
CPR	13	register clock input (active HIGH)
$\overline{\text{OE}}$	14	output enable input (active LOW)
V <sub>CC</sub>	16	supply voltage

## 6. Functional description

**Table 3. Function table**

H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH transition; ↓ = HIGH-to-LOW transition.  
 $RCO = \overline{Q0} \cdot Q1' \cdot Q2' \cdot Q3' \cdot Q4' \cdot Q5' \cdot Q6' \cdot Q7'$  ( $Q0'$  to  $Q7'$  are internal outputs of the counter).

Inputs					Description
OE	CPR	MRC	CE	CPC	
H	X	X	X	X	Q outputs disable
L	X	X	X	X	Q outputs enable
X	↑	X	X	X	counter data stored into register
X	↓	X	X	X	register stage is not changed
X	X	L	X	X	counter clear
X	X	H	L	↑	advance one count
X	X	H	L	↓	no count
X	X	H	H	X	no count



**Fig. 7. Typical timing sequence**

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ [1]	-	$\pm 20$	mA
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ [1]	-	$\pm 20$	mA
$I_O$	output current	$V_O = -0.5\text{ V}$ to $V_{CC} + 0.5\text{ V}$			
		RCO standard output	-	$\pm 25$	mA
		Qn bus driver output	-	$\pm 35$	mA
$I_{CC}$	supply current		-	70	mA
$I_{GND}$	ground current		-70	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT109-1 (SO16) package:  $P_{tot}$  derates linearly with 12.4 mW/K above 110 °C.

For SOT403-1 (TSSOP16) package:  $P_{tot}$  derates linearly with 8.5 mW/K above 91 °C.

For SOT763-1 (DHVQFN16) package:  $P_{tot}$  derates linearly with 11.2 mW/K above 106 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		2.0	5.0	6.0	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	ns/V
$T_{amb}$	ambient temperature		-40	-	+125	°C

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> all outputs								
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		$\overline{RCO}$ standard output								
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 4.5 V	4.18	4.31	-	4.13	-	4.1	-	V
		I <sub>O</sub> = -5.2 mA; V <sub>CC</sub> = 6.0 V	5.68	5.80	-	5.63	-	5.6	-	V
		Qn bus driver output								
		I <sub>O</sub> = -6.0 mA; V <sub>CC</sub> = 4.5 V	4.18	4.31	-	4.13	-	4.1	-	V
I <sub>O</sub> = -7.8 mA; V <sub>CC</sub> = 6.0 V	5.68	5.80	-	5.63	-	5.6	-	V		
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> all outputs								
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		$\overline{RCO}$ standard output								
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 4.5 V	-	0.17	0.26	-	0.33	-	0.4	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	0.18	0.26	-	0.33	-	0.4	V
		Qn bus driver output								
		I <sub>O</sub> = 6.0 mA; V <sub>CC</sub> = 4.5 V	-	0.17	0.26	-	0.33	-	0.4	V
I <sub>O</sub> = 7.8 mA; V <sub>CC</sub> = 6.0 V	-	0.18	0.26	-	0.33	-	0.4	V		
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.5	-	±5.0	-	±10	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	4.0	-	40	-	80	μA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

GND (ground = 0 V); for test circuit see Fig. 14.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$t_{pd}$	propagation delay	CPC to $\overline{RCO}$ ; see Fig. 8 [1]								
		$V_{CC} = 2.0\text{ V}$	-	52	150	-	190	-	230	ns
		$V_{CC} = 4.5\text{ V}$	-	19	30	-	38	-	45	ns
		$V_{CC} = 6.0\text{ V}$	-	15	26	-	33	-	40	ns
		CPR to Qn; see Fig. 9								
		$V_{CC} = 2.0\text{ V}$	-	50	140	-	175	-	210	ns
		$V_{CC} = 4.5\text{ V}$	-	17	28	-	35	-	42	ns
		$V_{CC} = 6.0\text{ V}$	-	14	24	-	30	-	36	ns
$t_{PLH}$	LOW to HIGH propagation delay	$\overline{MRC}$ to $\overline{RCO}$ ; see Fig. 10								
		$V_{CC} = 2.0\text{ V}$	-	53	130	-	165	-	200	ns
		$V_{CC} = 4.5\text{ V}$	-	18	26	-	33	-	40	ns
		$V_{CC} = 6.0\text{ V}$	-	14	22	-	28	-	34	ns
$t_{en}$	enable time	$\overline{OE}$ to Qn; see Fig. 11 [2]								
		$V_{CC} = 2.0\text{ V}$	-	28	105	-	130	-	160	ns
		$V_{CC} = 4.5\text{ V}$	-	13	21	-	26	-	32	ns
		$V_{CC} = 6.0\text{ V}$	-	11	18	-	22	-	27	ns
$t_{dis}$	disable time	$\overline{OE}$ to Qn; see Fig. 11 [3]								
		$V_{CC} = 2.0\text{ V}$	-	28	105	-	130	-	160	ns
		$V_{CC} = 4.5\text{ V}$	-	13	21	-	26	-	32	ns
		$V_{CC} = 6.0\text{ V}$	-	11	18	-	22	-	27	ns
$t_W$	pulse width	CPC and CPR; HIGH or LOW; see Fig. 8 and Fig. 9								
		$V_{CC} = 2.0\text{ V}$	100	24	-	125	-	145	-	ns
		$V_{CC} = 4.5\text{ V}$	20	9	-	25	-	29	-	ns
		$V_{CC} = 6.0\text{ V}$	17	8	-	21	-	25	-	ns
		$\overline{MRC}$ ; LOW; see Fig. 10								
		$V_{CC} = 2.0\text{ V}$	75	28	-	95	-	110	-	ns
		$V_{CC} = 4.5\text{ V}$	15	8	-	19	-	22	-	ns
		$V_{CC} = 6.0\text{ V}$	13	6	-	16	-	19	-	ns
$t_{su}$	set-up time	CPC to CPR; see Fig. 13								
		$V_{CC} = 2.0\text{ V}$	100	46	-	125	-	150	-	ns
		$V_{CC} = 4.5\text{ V}$	20	14	-	25	-	30	-	ns
		$V_{CC} = 6.0\text{ V}$	17	10	-	21	-	26	-	ns
		$\overline{CE}$ to CPC; see Fig. 12								
		$V_{CC} = 2.0\text{ V}$	100	44	-	125	-	150	-	ns
		$V_{CC} = 4.5\text{ V}$	20	11	-	25	-	30	-	ns
		$V_{CC} = 6.0\text{ V}$	17	9	-	21	-	26	-	ns



## 8-bit binary counter with output register; 3-state

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t <sub>h</sub>	hold time	CE to CPC; see Fig. 12								
		V <sub>CC</sub> = 2.0 V	0	-	-	0	-	0	-	ns
		V <sub>CC</sub> = 4.5 V	0	-	-	0	-	0	-	ns
		V <sub>CC</sub> = 6.0 V	0	-	-	0	-	0	-	ns
t <sub>rec</sub>	recovery time	MRC to CPC; see Fig. 10								
		V <sub>CC</sub> = 2.0 V	75	28	-	95	-	110	-	ns
		V <sub>CC</sub> = 4.5 V	15	7	-	19	-	22	-	ns
		V <sub>CC</sub> = 6.0 V	13	6	-	16	-	19	-	ns
f <sub>max</sub>	maximum frequency	CPC or CPR; see Fig. 8 and Fig. 9								
		V <sub>CC</sub> = 2.0 V	6.6	16	-	5.2	-	4.4	-	MHz
		V <sub>CC</sub> = 4.5 V	33	52	-	26	-	22	-	MHz
		V <sub>CC</sub> = 6.0 V	39	61	-	31	-	26	-	MHz
C <sub>PD</sub>	power dissipation capacitance	V <sub>I</sub> = GND to V <sub>CC</sub> [4]	-	44	-	-	-	-	-	pF

[1] t<sub>pd</sub> is the same as t<sub>PHL</sub> and t<sub>PLH</sub>.

[2] t<sub>en</sub> is the same as t<sub>PZH</sub> and t<sub>PZL</sub>.

[3] t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.

[4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs.

10.1. Waveforms and test circuit

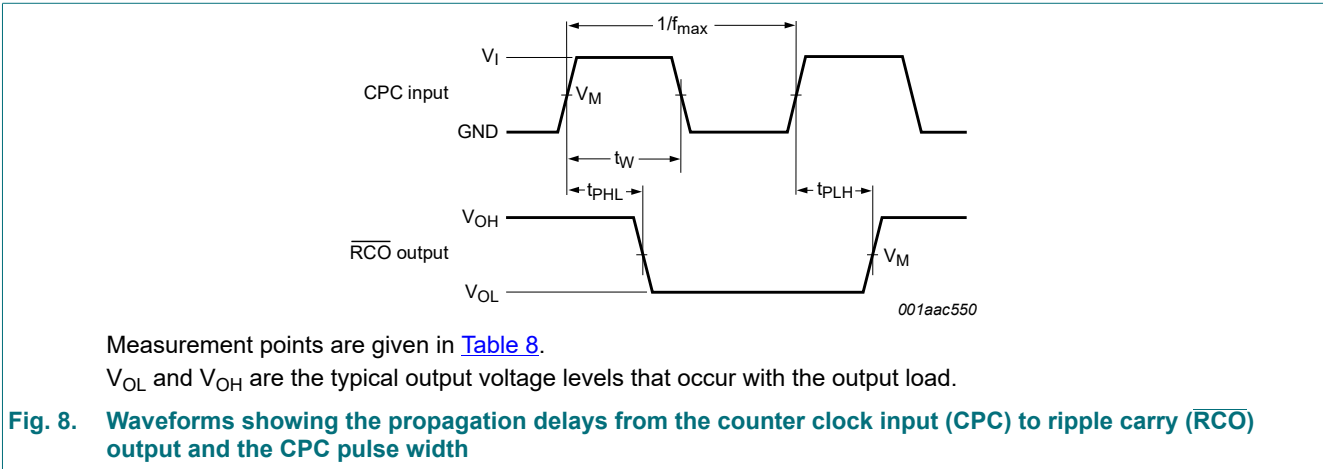
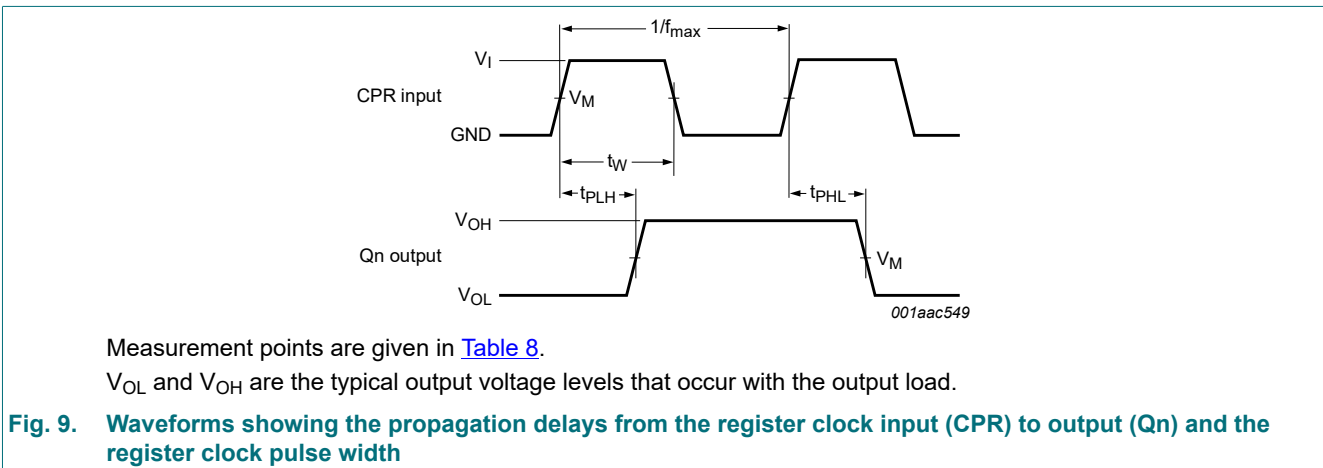
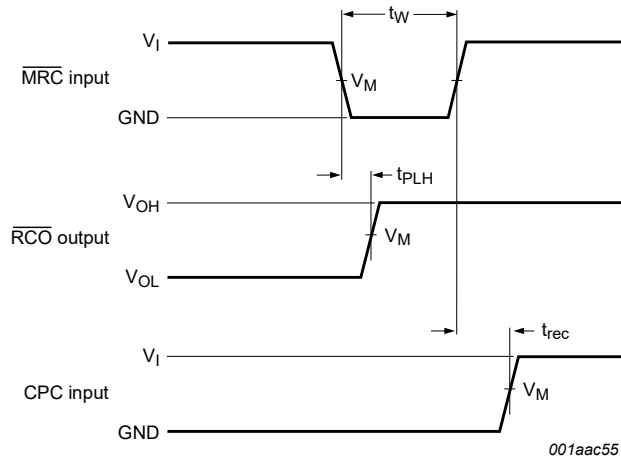


Table 8. Measurement points

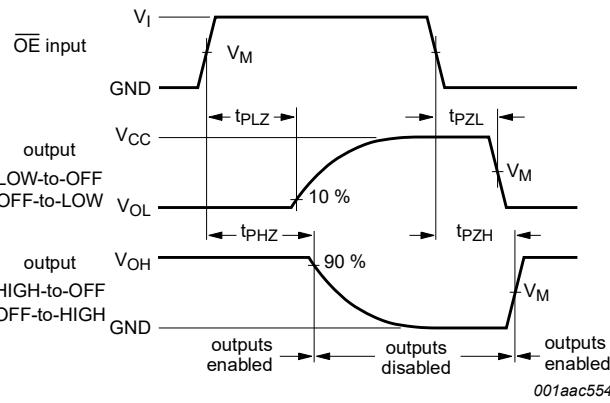
Input		Output
$V_I$	$V_M$	$V_M$
$V_{CC}$	$0.5V_{CC}$	$0.5V_{CC}$





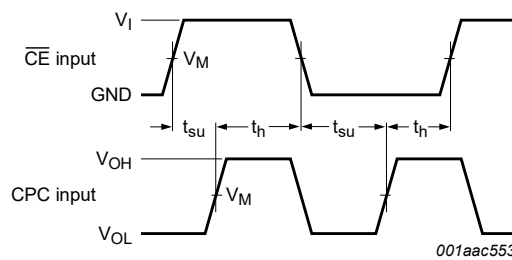
Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage levels that occur with the output load.

**Fig. 10. Waveforms showing the propagation delays from the master reset counter input ( $\overline{MRC}$ ) to output ( $\overline{RCO}$ ), the  $\overline{MRC}$  pulse width and recovery time**



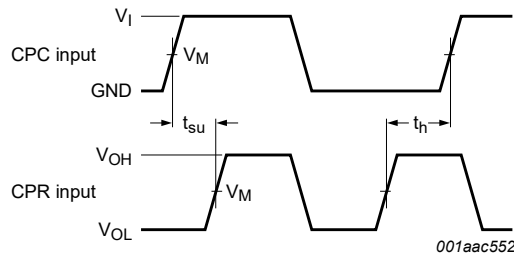
Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage levels that occur with the output load.

**Fig. 11. Waveforms showing the 3-state enable and disable times**



Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage levels that occur with the output load.

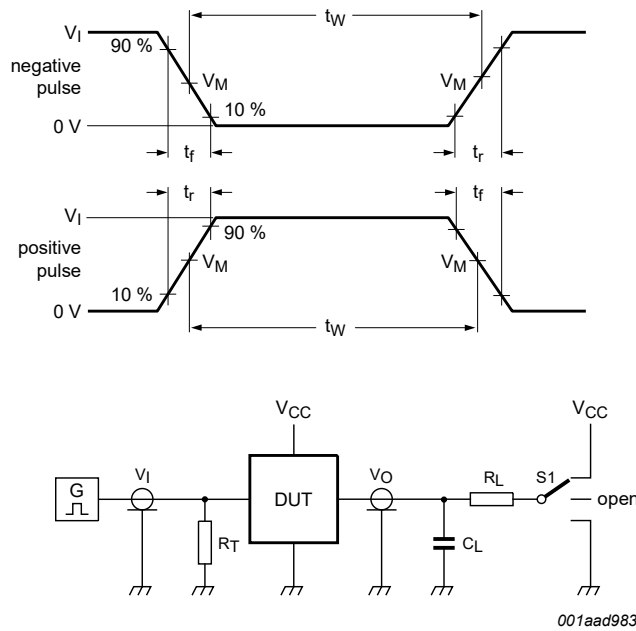
**Fig. 12. Waveforms showing the set-up and hold times for the count enable input ( $\overline{CE}$ ) to the counter clock input (CPC)**



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are the typical output voltage levels that occur with the output load.

**Fig. 13. Waveforms showing the set-up and hold times for the counter clock input (CPC) to the register clock input (CPR)**



Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator;

$C_L$  = Load capacitance including jig and probe capacitance;

$R_L$  = Load resistance;

S1 = Test selection switch.

**Fig. 14. Test circuit for measuring switching times**

**Table 9. Test data**

Supply voltage	Input		Load		Switch position		
$V_{CC}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
2.0 V to 6.0 V	$V_{CC}$	6 ns	50 pF	1 kΩ	open	GND	$V_{CC}$

### 11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

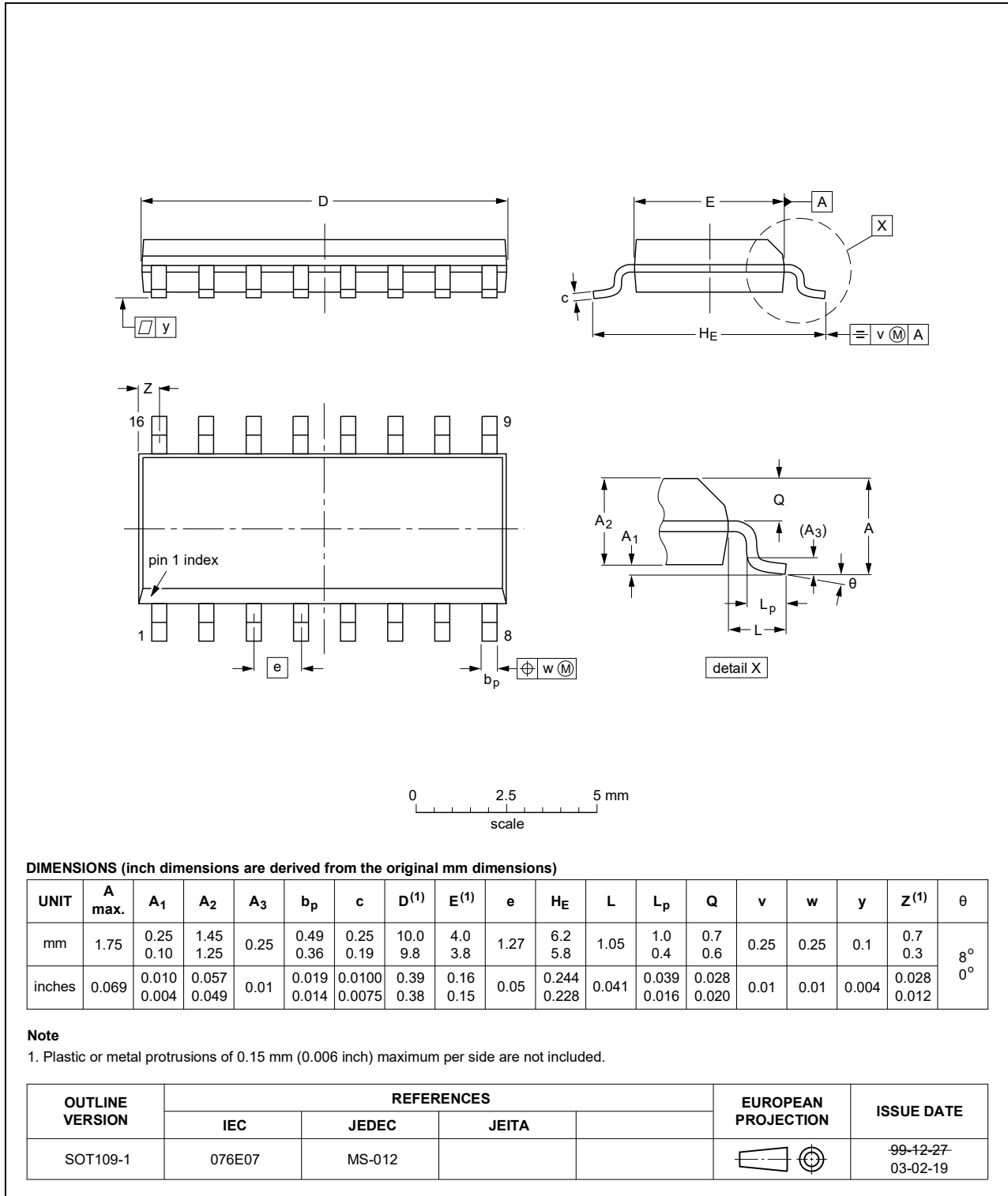


Fig. 15. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

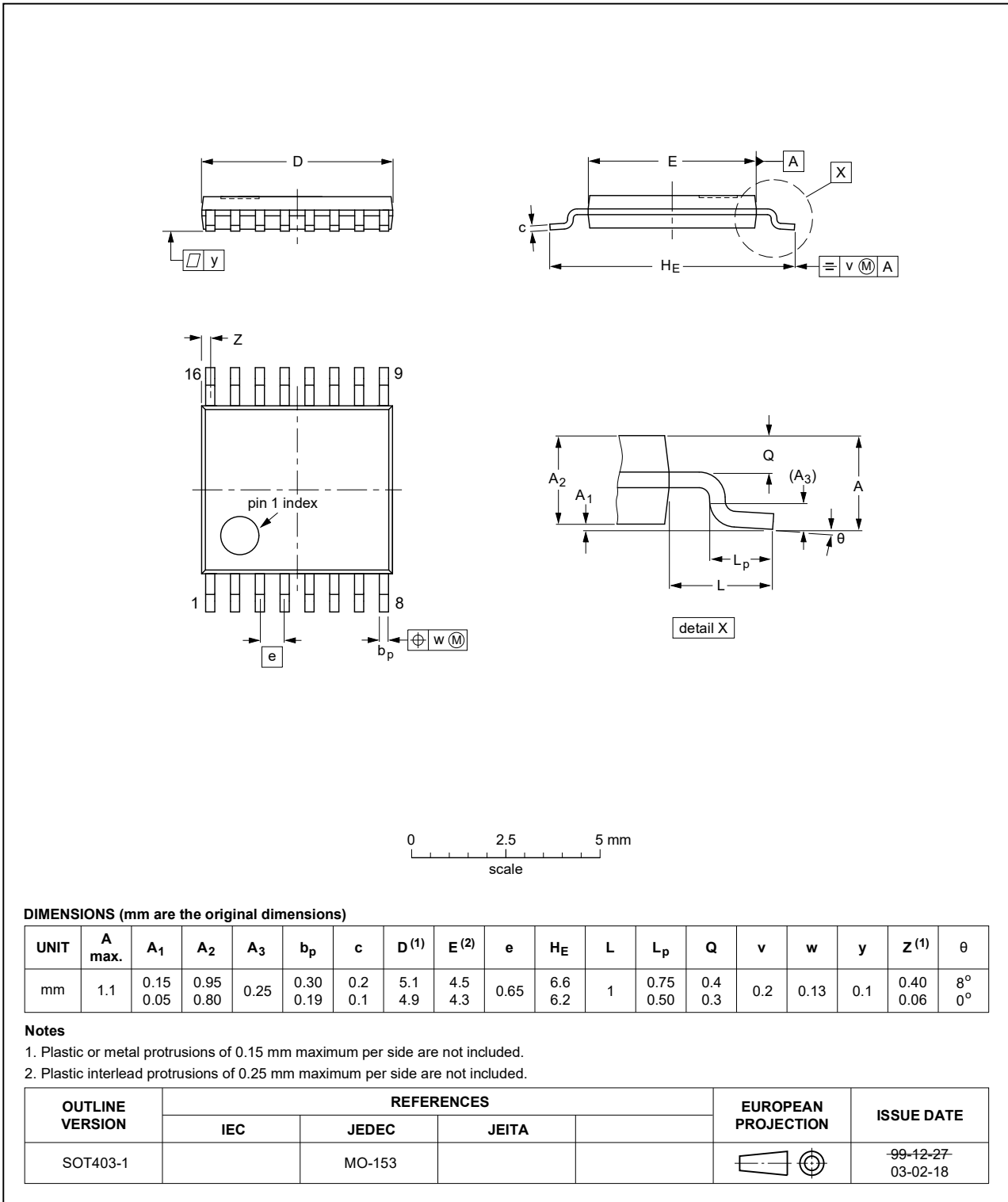


Fig. 16. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

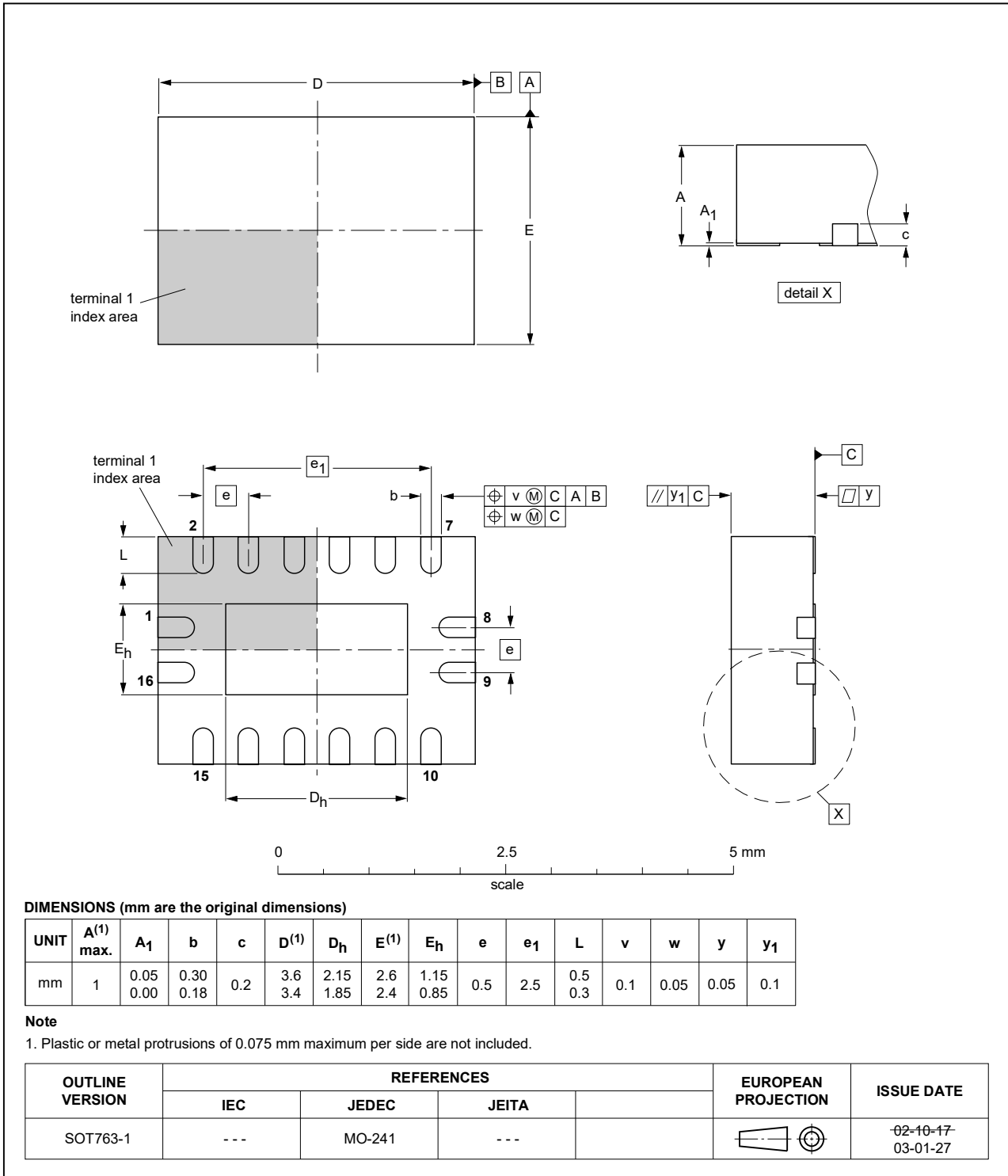


Fig. 17. Package outline SOT763-1 (DHVQFN16)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC590 v.4	20220314	Product data sheet	-	74HC590 v.3
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 2</a> updated.</li> <li>ESD CDM value changed from 2000 V to 1000 V (errata).</li> <li><a href="#">Section 7</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> </ul>			
74HC590 v.3	20160224	Product data sheet	-	74HC590 v.2
Modifications:	<ul style="list-style-type: none"> <li>Type number 74HC590N (SOT38-4) removed.</li> </ul>			
74HC590 v.2	20090428	Product data sheet	-	74HC590 v.1
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Quick reference data incorporated in to <a href="#">Section 9</a> and <a href="#">Section 10</a>.</li> <li>Added type number 74HC590N (DIP16 package)</li> </ul>			
74HC590 v.1	20050330	Product data sheet	-	-



## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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