Hex inverter

Rev. 10 — 28 August 2020

Product data sheet

1. General description

The 74LVC04A is a hex inverter. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

2. Features and benefits

- · Overvoltage tolerant inputs to 5.5 V
- Wide supply voltage range from 1.2 V to 3.6 V
- · CMOS low power consumption
- · Direct interface with TTL levels
- Complies with JEDEC standard:
 - JESD8-7A (1.65 V to 1.95 V)
 - JESD8-5A (2.3 V to 2.7 V)
 - JESD8-C/JESD36 (2.7 V to 3.6 V)
- · ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-B exceeds 200 V
 - CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

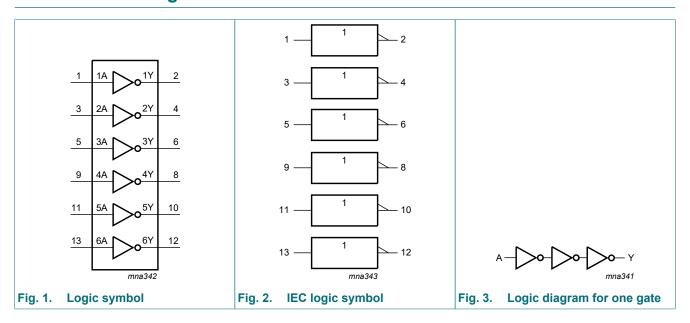
Table 1. Ordering information

Type number	Package								
	Temperature range	Name	Description	Version					
74LVC04AD	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1					
74LVC04ADB	-40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1					
74LVC04APW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1					
74LVC04ABQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1					



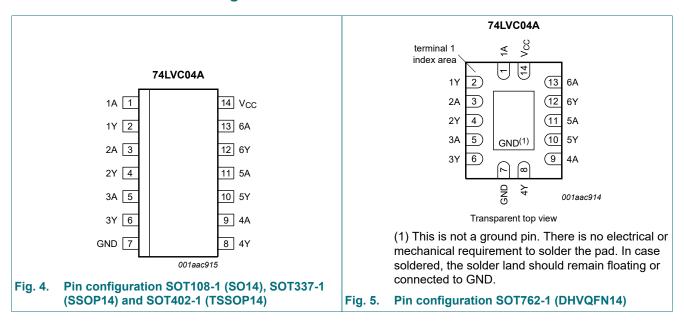
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4. Functional diagram



5. Pinning information

5.1. Pinning



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5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level

Input nA	Output nY
L	Н
Н	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0		-50	-	mA
VI	input voltage		[1]	-0.5	+6.5	V
I _{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$		-	±50	mA
Vo	output voltage		[2]	-0.5	V _{CC} + 0.5	V
Io	output current	$V_O = 0 V \text{ to } V_{CC}$		-	±50	mA
I _{CC}	supply current			-	100	mA
I_{GND}	ground current			-100	-	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[3]	-	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

- [2] The output voltage ratings may be exceeded if the output current ratings are observed.
- [3] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C. For SOT337-1 (SSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C. For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

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8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
VI	input voltage		0	-	5.5	V
Vo	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
		V _{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40	°C to +85	°C	-40 °C to	Unit	
			Min	Typ [1]	Max	Min	Max	
V _{IH}	HIGH-level input	V _{CC} = 1.2 V	1.08	-	-	1.08	-	V
	voltage	V _{CC} = 1.65 V to 1.95 V	0.65V _{CC}	-	-	0.65V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input	V _{CC} = 1.2 V	-	-	0.12	-	0.12	V
	voltage	V _{CC} = 1.65 V to 1.95 V	-	-	0.35V _{CC}	-	0.35V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level	V _I = V _{IH} or V _{IL}						
	output voltage	I _O = -100 μA; V _{CC} = 1.65 V to 3.6 V	V _{CC} - 0.2	-	-	V _{CC} - 0.3	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	1.2	-	-	1.05	-	V
		$I_O = -8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.8	-	-	1.65	-	V
		$I_O = -12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	2.2	-	-	2.05	-	V
		$I_O = -18 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.4	-	-	2.25	-	V
		$I_O = -24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.2	-	-	2.0	-	V
V _{OL}	LOW-level output	V _I = V _{IH} or V _{IL}						
	voltage	I _O = 100 μA; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I_{O} = 24 mA; V_{CC} = 3.0 V	-	-	0.55	-	0.8	V

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Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to	Unit	
			Min	Typ [1]	Max	Min	Max	
l _l	input leakage current	V _{CC} = 3.6 V; V _I = 5.5 V or GND	-	±0.1	±5	-	±20	μΑ
I _{CC}	supply current	$V_{CC} = 3.6 \text{ V}; V_{I} = V_{CC} \text{ or GND};$ $I_{O} = 0 \text{ A}$	-	0.1	10	-	40	μΑ
ΔI _{CC}	additional supply current	per input pin; $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V};$ $V_{I} = V_{CC} - 0.6 \text{ V};$ $I_{O} = 0 \text{ A}$	-	5	500	-	5000	μA
Cı	input capacitance	$V_{CC} = 0 \text{ V to } 3.6 \text{ V};$ $V_I = \text{GND to } V_{CC}$	-	4.0	-	-	-	pF

^[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 7.

Symbol	Parameter	Conditions		-40 °C to +85 °C			-40 °C to	+125 °C	Unit
				Min	Typ [1]	Max	Min	Max	
t _{pd}	propagation delay	nA to nY; see Fig. 6	[2]						
		V _{CC} = 1.2 V		-	14	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V		0.3	3.7	8.8	0.3	10.2	ns
		V _{CC} = 2.3 V to 2.7 V		0.5	2.2	5.0	0.5	5.8	ns
		V _{CC} = 2.7 V		1.0	2.1	5.5	1.0	7.0	ns
		V _{CC} = 3.0 V to 3.6 V		1.0	2.0	4.5	1.0	6.0	ns
t _{sk(o)}	output skew time	V _{CC} = 3.0 V to 3.6 V	[3]	-	-	1.0	-	1.5	ns
C _{PD}	power dissipation	per buffer; V_I = GND to V_{CC}	[4]						
	capacitance	V _{CC} = 1.65 V to 1.95 V		-	3.9	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V		-	7.1	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V		-	9.9	-	-	-	pF

- [1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.
- t_{pd} is the same as t_{PLH} and t_{PHL}.

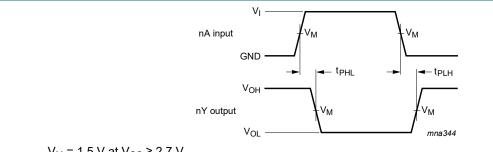
 Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
- [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W). $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

 - f_i = input frequency in MHz; f_o = output frequency in MHz
 - C_L = output load capacitance in pF
 - V_{CC} = supply voltage in Volts
 - N = number of inputs switching
 - $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

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10.1. Waveforms and test circuit

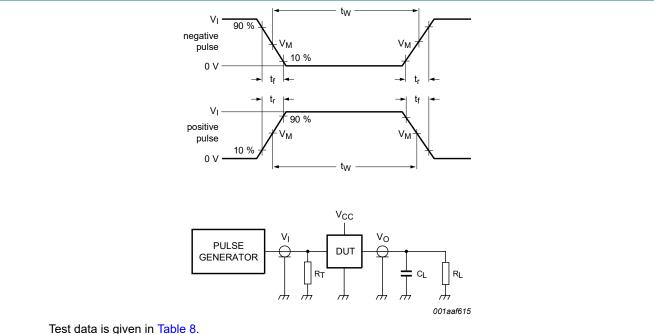


 $V_M = 1.5 \text{ V at } V_{CC} \ge 2.7 \text{ V}$

 $V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7 \text{ V}$

 $\ensuremath{V_{\text{OL}}}$ and $\ensuremath{V_{\text{OH}}}$ are typical output voltage levels that occur with the output load.

The input (nA) to output (nY) propagation delays Fig. 6.



Definitions for test circuit:

R_L = Load resistance

 C_L = Load capacitance including jig and probe capacitance

 R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator.

Fig. 7. Test circuit for measuring switching times

Table 8. Test data

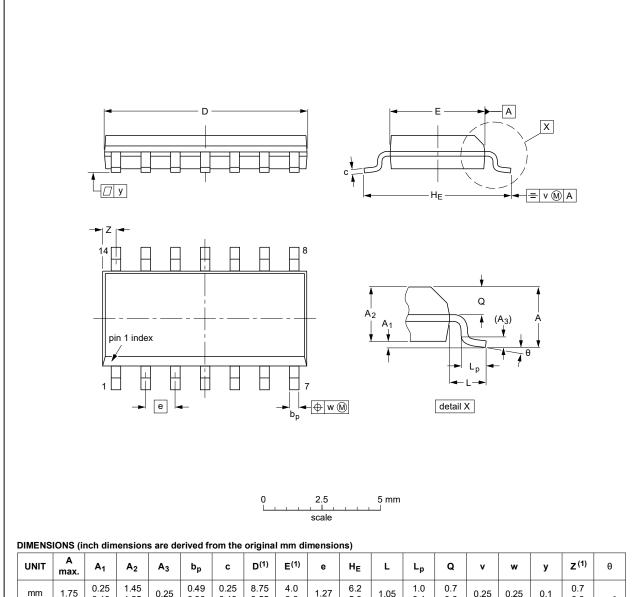
Supply voltage	Input		Load	Load		
	VI	t _r , t _f	CL	R _L		
1.2 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ		
1.65 V to 1.95 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ		
2.3 V to 2.7 V	V _{CC}	≤ 2 ns	30 pF	500 Ω		
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω		
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω		

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11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



	UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
	mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
ir	nches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	0°

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	EUROPEAN ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT108-1	076E06	MS-012				99-12-27 03-02-19

Fig. 8. Package outline SOT108-1 (SO14)

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SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

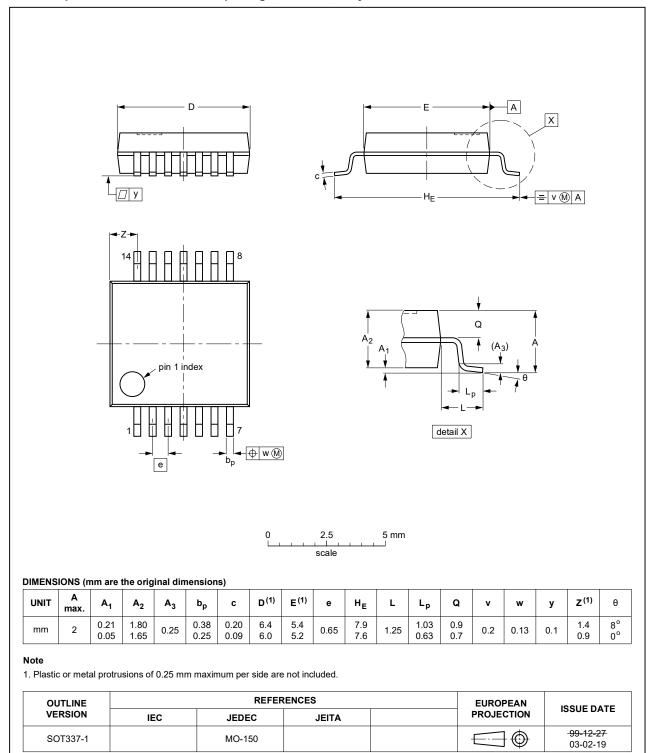


Fig. 9. Package outline SOT337-1 (SSOP14)

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

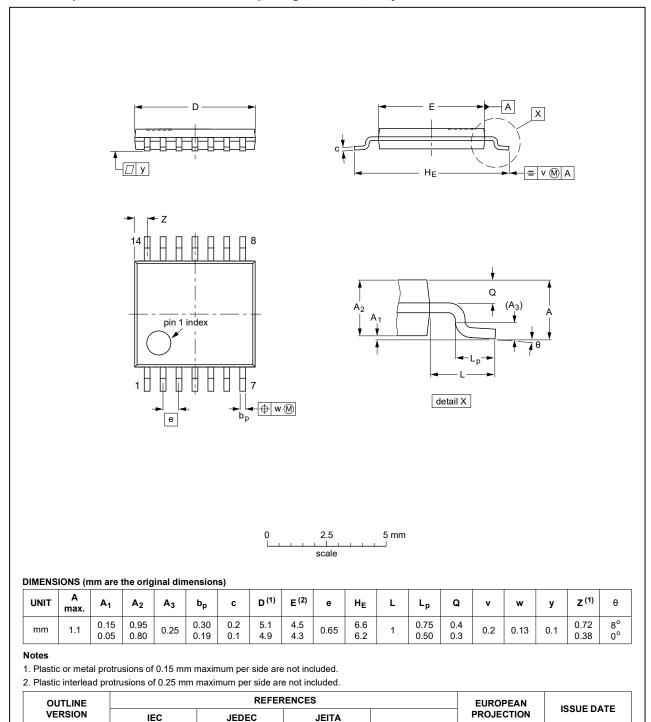


Fig. 10. Package outline SOT402-1 (TSSOP14)

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SOT402-1

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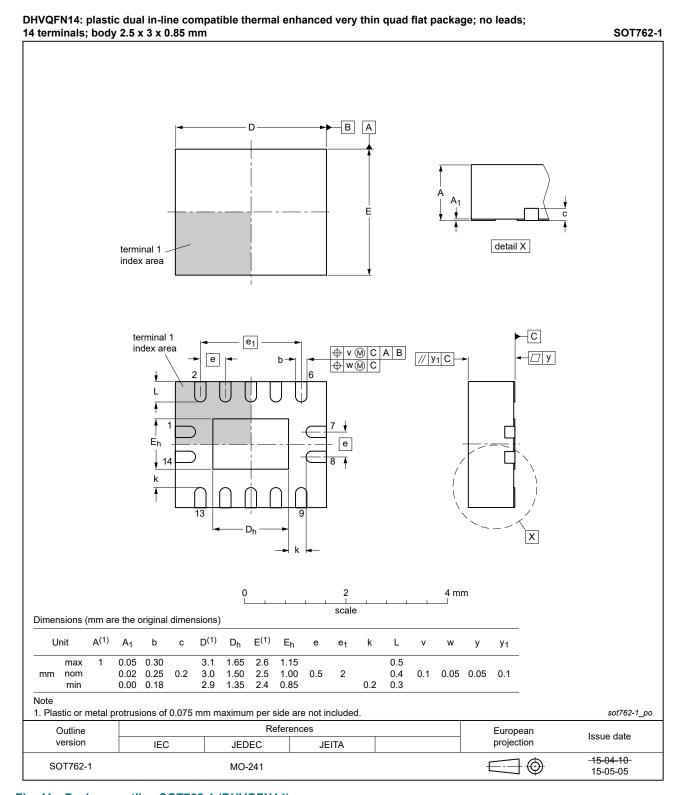


Fig. 11. Package outline SOT762-1 (DHVQFN14)

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12. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74LVC04A v.10	20200828	Product data sheet	-	74LVC04A v.9	
Modifications:	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 1 and Section 2 updated. Table 4: Derating values for P_{tot} total power dissipation updated. Fig. 11: Package outline drawing SOT762-1 (DHVQFN14) updated. 				
74LVC04A v.9	20111117	Product data sheet	-	74LVC04A v.8	
Modifications:	 Legal pages updated. Table 6, bodyrow ΔI_{CC}: condition V_{CC} changed. 				
74LVC04A v.8	20110926	Product data sheet	-	74LVC04A v.7	
74LVC04A v.7	20110201	Product data sheet	-	74LVC04A v.6	
74LVC04A v.6	20030904	Product specification	-	74LVC04A v.5	
74LVC04A v.5	20030224	Product specification	-	74LVC04A v.4	
74LVC04A v.4	20020308	Product specification	-	74LVC04A v.3	
74LVC04A v.3	19970630	Product specification	-	74LVC04A v.2	
74LVC04A v.2	19970630	Product specification	-	74LVC04A v.1	
74LVC04A v.1	19970203	Product specification	-	-	

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14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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