

74HC597; 74HCT597

8-bit shift register with input flip-flops

Rev. 5 — 26 October 2021

Product data sheet

1. General description

The 74HC597; 74HCT597 is an 8-bit shift register with input flip-flops. It consists of an 8-bit storage register feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and the shift register have positive edge-triggered clocks. The shift register also has direct load (from storage) and clear inputs. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Input levels:
 - For 74HC597: CMOS level
 - For 74HCT597: TTL level
- 8-bit parallel storage register inputs
- Shift register has direct overriding load and clear
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- ESD protection:
 - HBM EIA/JESD22-A114F exceeds 2000 V
 - MM EIA/JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC597D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT597D				
74HCT597DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC597PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT597PW				

4. Functional diagram

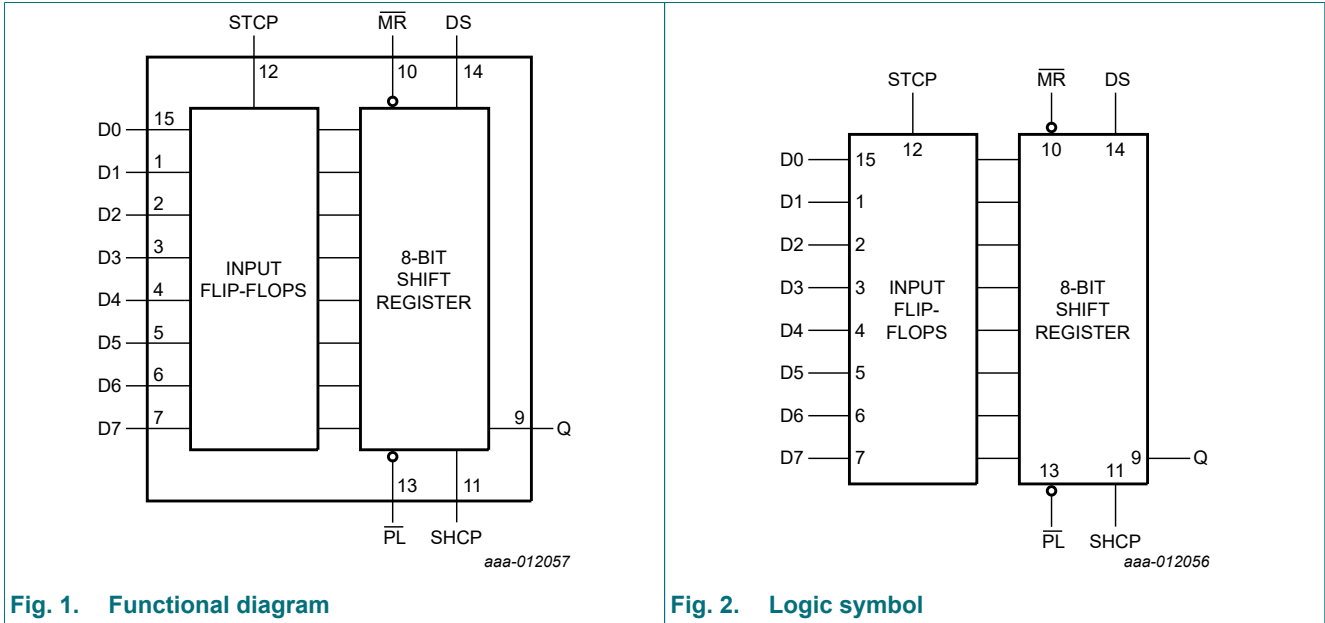


Fig. 1. Functional diagram

Fig. 2. Logic symbol

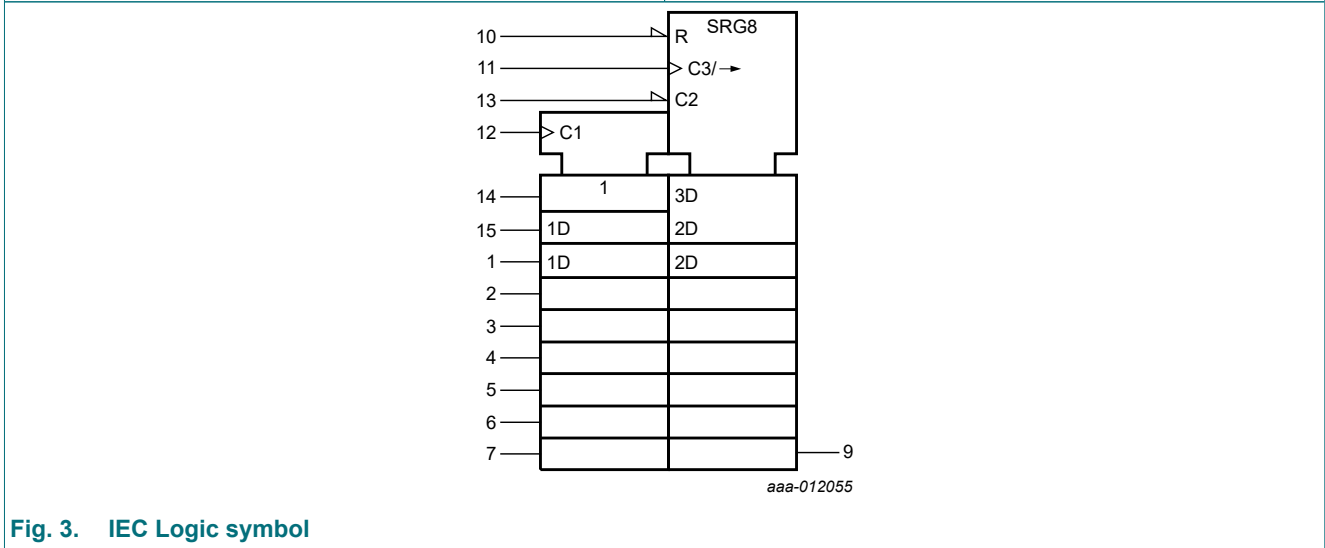


Fig. 3. IEC Logic symbol

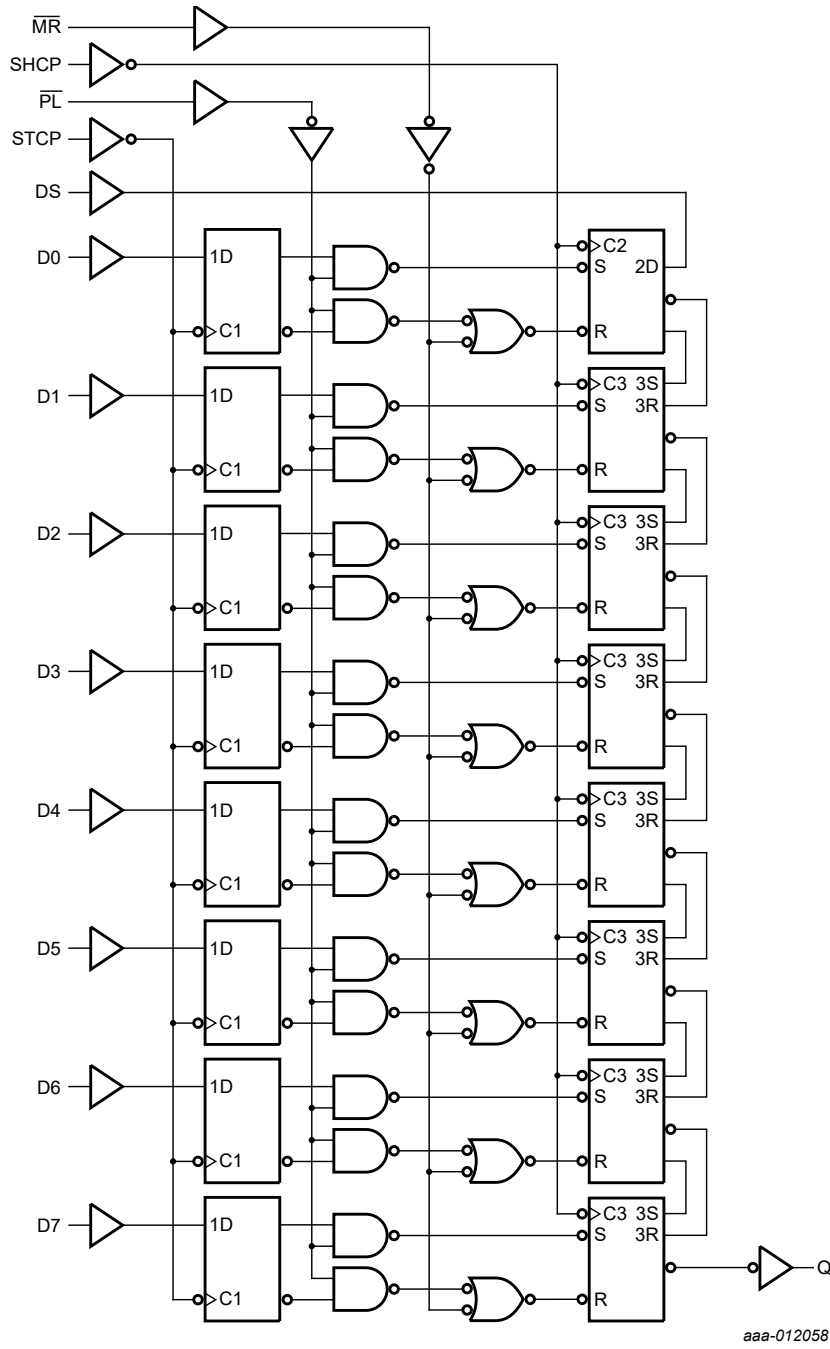
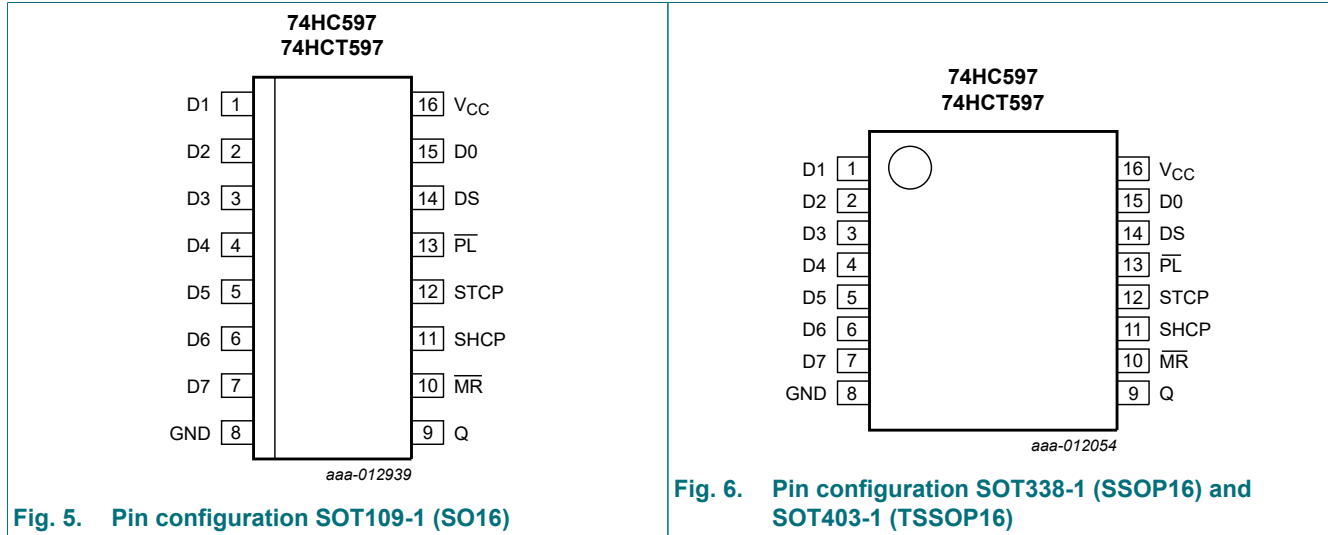


Fig. 4. Logic diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
GND	8	ground (0 V)
Q	9	serial data output
\overline{MR}	10	asynchronous master reset input (active LOW)
SHCP	11	shift register clock input (LOW-to-HIGH, edge-triggered)
STCP	12	storage register clock input (LOW-to-HIGH, edge-triggered)
\overline{PL}	13	parallel load input (active LOW)
DS	14	serial data input
D0, D1, D2, D3, D4, D5, D6, D7	15, 1, 2, 3, 4, 5, 6, 7	parallel data inputs
V _{CC}	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = positive-going transition.

Inputs				Function
STCP	SHCP	PL	MR	
↑	X	X	X	data loaded to input latches
↑	X	L	H	data loaded from inputs to shift register
no clock edge	X	L	H	data transferred from input flip-flops to shift register
X	X	L	L	invalid logic, state of shift register is indeterminate when signals removed
X	X	H	L	shift register cleared
X	↑	H	H	shift register clocked Q _n = Q _{n-1} , Q ₀ = DS

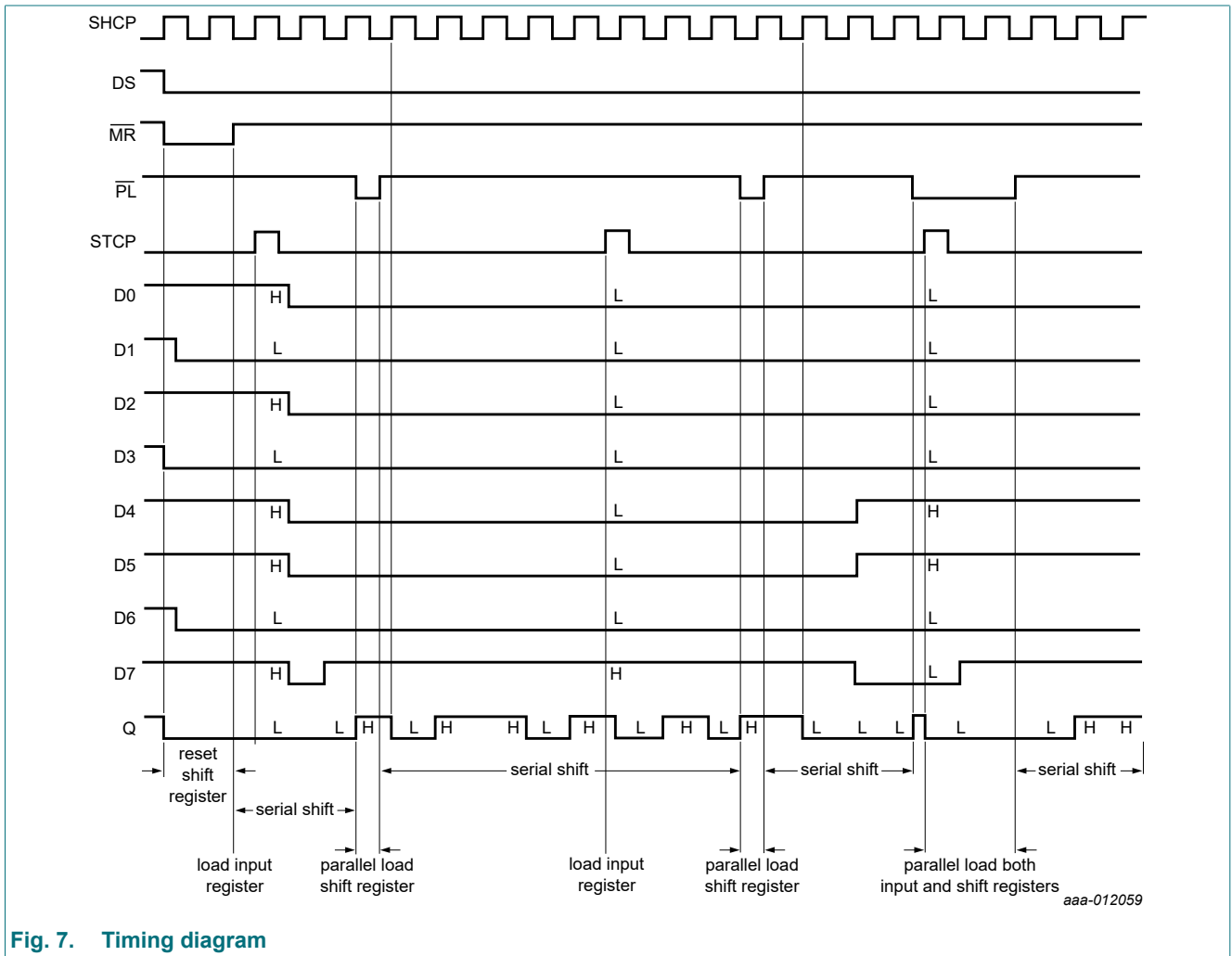


Fig. 7. Timing diagram

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_O	output current	$V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$	-	± 25	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	[1]	-	500	mW

- [1] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
 For SOT338-1 (SSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
 For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC597			74HCT597			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC597										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
		V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80.0	-	160.0	μA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT597										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	8.0	-	80.0	-	160.0	µA
ΔI _{CC}	additional supply current	V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; I _O = 0 A								
		per input pin; DS input	-	25	90	-	112.5	-	122.5	µA
		per input pin; Dn inputs	-	30	108	-	135	-	147	µA
		per input pin; PL, MR inputs	-	150	540	-	675	-	735	µA
		per input pin; STCP, SHCP inputs	-	150	540	-	675	-	735	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see Fig. 14.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC597										
t_{pd}	propagation delay	SHCP to Q; see Fig. 8 [1]								
		$V_{CC} = 2.0$ V	-	55	175	-	220	-	265	ns
		$V_{CC} = 4.5$ V	-	20	35	-	44	-	53	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	17	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	16	30	-	37	-	45	ns
		MR to Q; see Fig. 9 [1]								
		$V_{CC} = 2.0$ V	-	58	175	-	220	-	265	ns
		$V_{CC} = 4.5$ V	-	21	35	-	44	-	53	ns
		$V_{CC} = 6.0$ V	-	17	30	-	37	-	45	ns
		STCP to Q; see Fig. 8 [1]								
		$V_{CC} = 2.0$ V	-	80	250	-	315	-	375	ns
		$V_{CC} = 4.5$ V	-	29	50	-	63	-	75	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	25	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	23	43	-	54	-	64	ns
		PL to Q; see Fig. 10 [1]								
		$V_{CC} = 2.0$ V	-	69	215	-	270	-	325	ns
$V_{CC} = 4.5$ V	-	25	43	-	54	-	65	ns		
$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	21	-	-	-	-	-	ns		
$V_{CC} = 6.0$ V	-	20	37	-	46	-	55	ns		
t_t	transition time	Q; see Fig. 10 [2]								
		$V_{CC} = 2.0$ V	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0$ V	-	6	13	-	16	-	19	ns

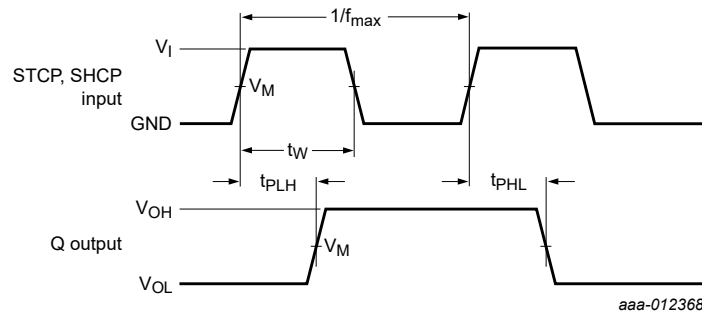
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _w	pulse width	STCP HIGH or LOW; see Fig. 8								
		V _{CC} = 2.0 V	80	11	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	4	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	3	-	17	-	20	-	ns
		SHCP HIGH or LOW; see Fig. 8								
		V _{CC} = 2.0 V	80	14	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	5	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	4	-	17	-	20	-	ns
		$\overline{\text{MR}}$ LOW; see Fig. 9								
		V _{CC} = 2.0 V	80	22	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	6	-	17	-	20	-	ns
		PL LOW; see Fig. 10								
V _{CC} = 2.0 V	80	22	-	100	-	120	-	ns		
V _{CC} = 4.5 V	16	8	-	20	-	24	-	ns		
V _{CC} = 6.0 V	14	6	-	17	-	20	-	ns		
t _{rec}	recovery time	MR to SHCP; see Fig. 11								
		V _{CC} = 2.0 V	60	-3	-	75	-	90	-	ns
		V _{CC} = 4.5 V	12	-1	-	15	-	18	-	ns
		V _{CC} = 6.0 V	10	-1	-	13	-	15	-	ns
t _{su}	set-up time	Dn to STCP; see Fig. 12								
		V _{CC} = 2.0 V	60	8	-	75	-	90	-	ns
		V _{CC} = 4.5 V	12	3	-	15	-	18	-	ns
		V _{CC} = 6.0 V	10	2	-	13	-	15	-	ns
		DS to SHCP; see Fig. 12								
		V _{CC} = 2.0 V	60	11	-	75	-	90	-	ns
		V _{CC} = 4.5 V	12	4	-	15	-	18	-	ns
		V _{CC} = 6.0 V	10	3	-	13	-	15	-	ns
		$\overline{\text{PL}}$ to SHCP; see Fig. 13								
		V _{CC} = 2.0 V	60	11	-	75	-	90	-	ns
		V _{CC} = 4.5 V	12	4	-	15	-	18	-	ns
		V _{CC} = 6.0 V	10	3	-	13	-	15	-	ns
t _h	hold time	Dn to STCP; see Fig. 12								
		V _{CC} = 2.0 V	5	-3	-	5	-	5	-	ns
		V _{CC} = 4.5 V	5	-1	-	5	-	5	-	ns
		V _{CC} = 6.0 V	5	-1	-	5	-	5	-	ns
		$\overline{\text{PL}}$, DS to SHCP; see Fig. 12								
		V _{CC} = 2.0 V	5	-6	-	5	-	5	-	ns
		V _{CC} = 4.5 V	5	-2	-	5	-	5	-	ns
V _{CC} = 6.0 V	5	-2	-	5	-	5	-	ns		

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
f _{max}	maximum frequency	SHCP; see Fig. 8								
		V _{CC} = 2.0 V	6.0	29	-	4.8	-	4.0	-	MHz
		V _{CC} = 4.5 V	30	87	-	24	-	20	-	MHz
		V _{CC} = 5.0 V; C _L = 15 pF	-	96	-	-	-	-	-	MHz
		V _{CC} = 6.0 V	35	104	-	28	-	24	-	MHz
C _{PD}	power dissipation capacitance	C _L = 50 pF; f = 1 MHz; V _I = GND to V _{CC} [3]	-	29	-	-	-	-	-	pF
74HCT597										
t _{pd}	propagation delay	SHCP to Q; see Fig. 8 [1]								
		V _{CC} = 4.5 V	-	23	40	-	50	-	60	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	20	-	-	-	-	-	ns
		MR to Q; see Fig. 9 [1]								
		V _{CC} = 4.5 V	-	28	49	-	61	-	74	ns
		STCP to Q; see Fig. 8 [1]								
		V _{CC} = 4.5 V	-	33	57	-	71	-	86	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	29	-	-	-	-	-	ns
		PL to Q; see Fig. 10 [1]								
		V _{CC} = 4.5 V	-	30	52	-	65	-	78	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	26	-	-	-	-	-	ns
t _t	transition time	Q; see Fig. 10 [2]								
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
t _w	pulse width	STCP HIGH or LOW; see Fig. 8								
		V _{CC} = 4.5 V	16	6	-	20	-	24	-	ns
		SHCP HIGH or LOW; see Fig. 8								
		V _{CC} = 4.5 V	16	7	-	20	-	24	-	ns
		MR LOW; see Fig. 9								
		V _{CC} = 4.5 V	25	14	-	31	-	38	-	ns
		PL LOW; see Fig. 10								
		V _{CC} = 4.5 V	20	10	-	25	-	30	-	ns
t _{rec}	recovery time	MR to SHCP; see Fig. 11								
		V _{CC} = 4.5 V	12	-2	-	15	-	18	-	ns
t _{su}	set-up time	Dn to STCP; see Fig. 12								
		V _{CC} = 4.5 V	12	5	-	15	-	18	-	ns
		DS to SHCP; see Fig. 12								
		V _{CC} = 4.5 V	12	2	-	15	-	18	-	ns
		PL to SHCP; see Fig. 13								
		V _{CC} = 4.5 V	12	4	-	15	-	18	-	ns
t _h	hold time	Dn to STCP; see Fig. 12								
		V _{CC} = 4.5 V	5	-1	-	5	-	5	-	ns
		PL, DS to SHCP; see Fig. 12								
		V _{CC} = 4.5 V	5	-2	-	5	-	5	-	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
f _{max}	maximum frequency	SHCP; see Fig. 8								
		V _{CC} = 4.5 V	30	75	-	24	-	20	-	MHz
		V _{CC} = 5.0 V; C _L = 15 pF	-	83	-	-	-	-	-	MHz
C _{PD}	power dissipation capacitance	C _L = 50 pF; f = 1 MHz; V _I = GND to V _{CC} - 1.5 V [3]	-	32	-	-	-	-	-	pF

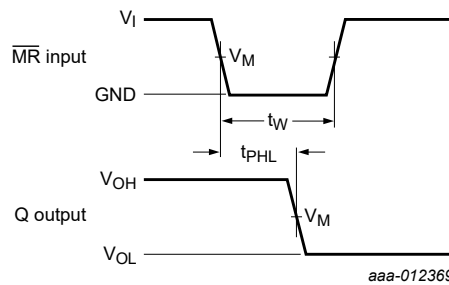
- [1] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [2] t_i is the same as t_{THL} and t_{TLH}.
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit



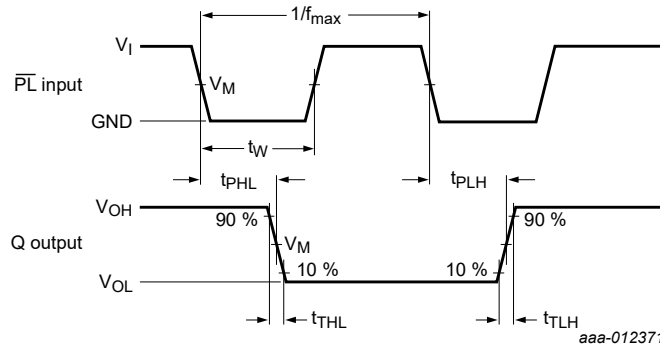
Measurement points are given in Table 8.
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 8. SHCP and STCP clock inputs to Q output propagation delays, pulse width and maximum clock frequency



Measurement points are given in Table 8.
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

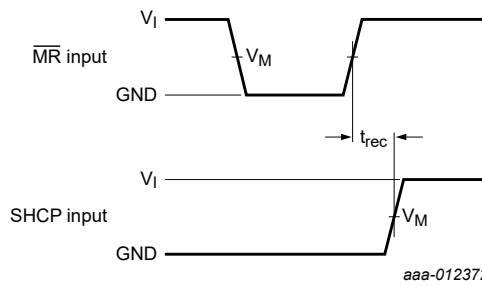
Fig. 9. Input MR to Q output propagation delays and MR pulse width



Measurement points are given in [Table 8](#).

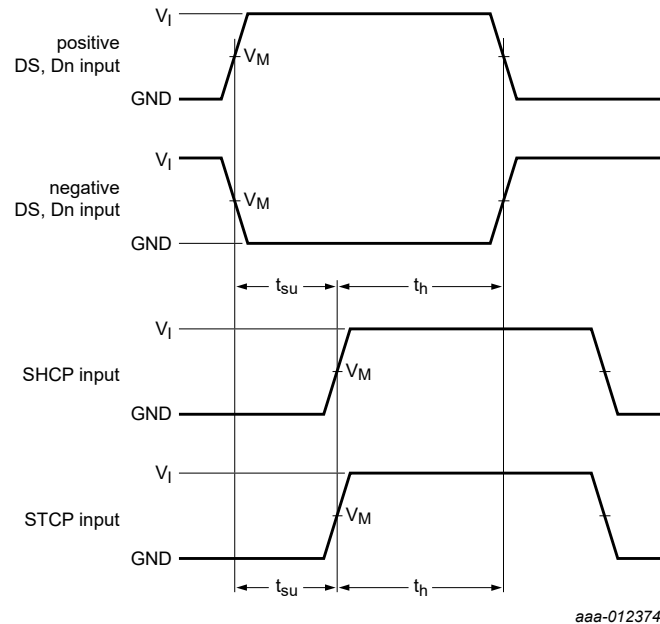
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 10. Input \overline{PL} to Q output propagation delays, \overline{PL} pulse width and output transition times



Measurement points are given in [Table 8](#).

Fig. 11. Input \overline{MR} to shift clock SHCP and storage clock STCP recovery times



Measurement points are given in [Table 8](#).

Fig. 12. Set-up and hold times for DS, Dn inputs to SHCP, STCP inputs

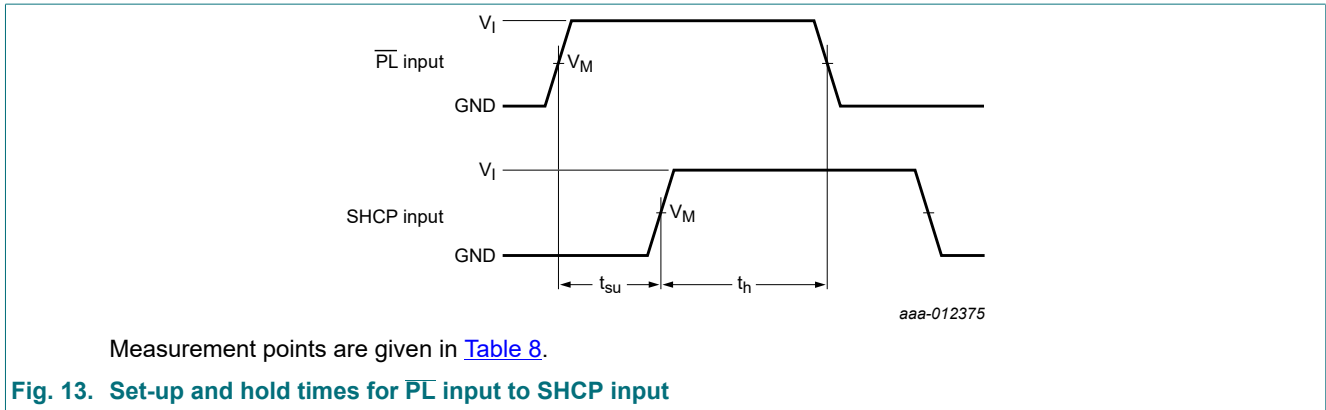


Table 8. Measurement points

Type	Input		Output
	V_M	V_I	V_M
74HC597	$0.5 \times V_{CC}$	GND to V_{CC}	$0.5 \times V_{CC}$
74HCT597	1.3 V	GND to 3 V	1.3 V

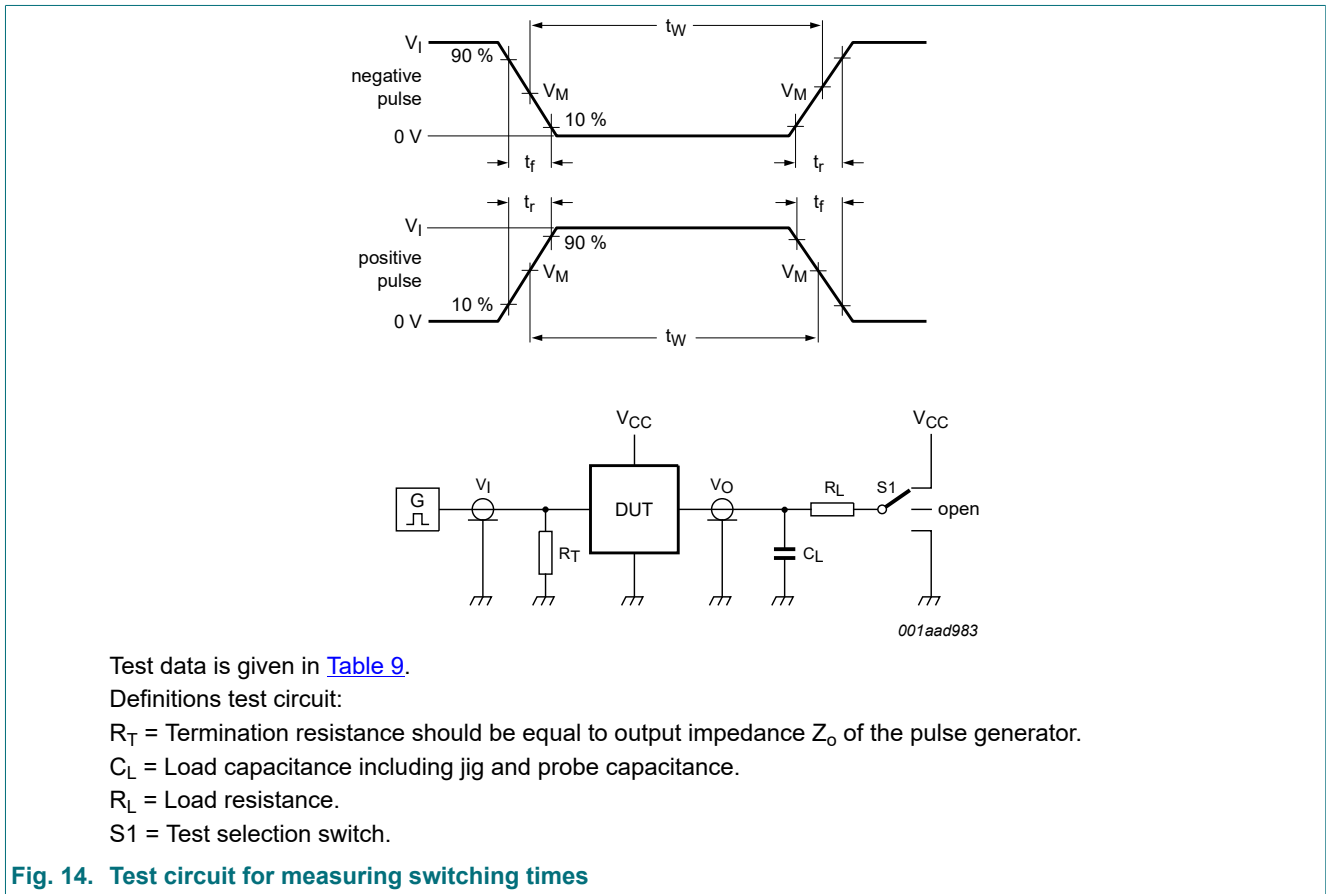


Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC597	V_{CC}	6 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}
74HCT597	3 V	6 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

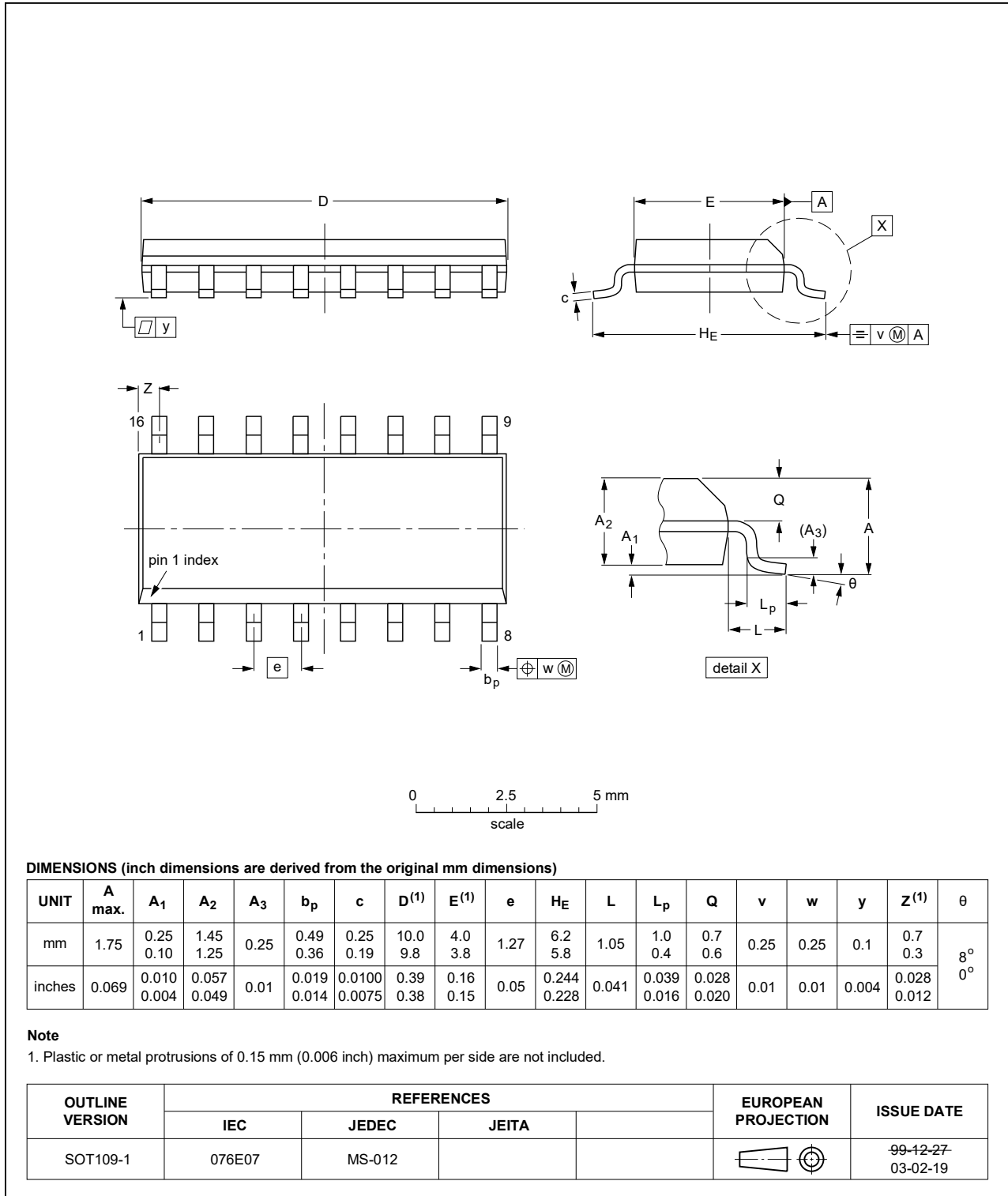


Fig. 15. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

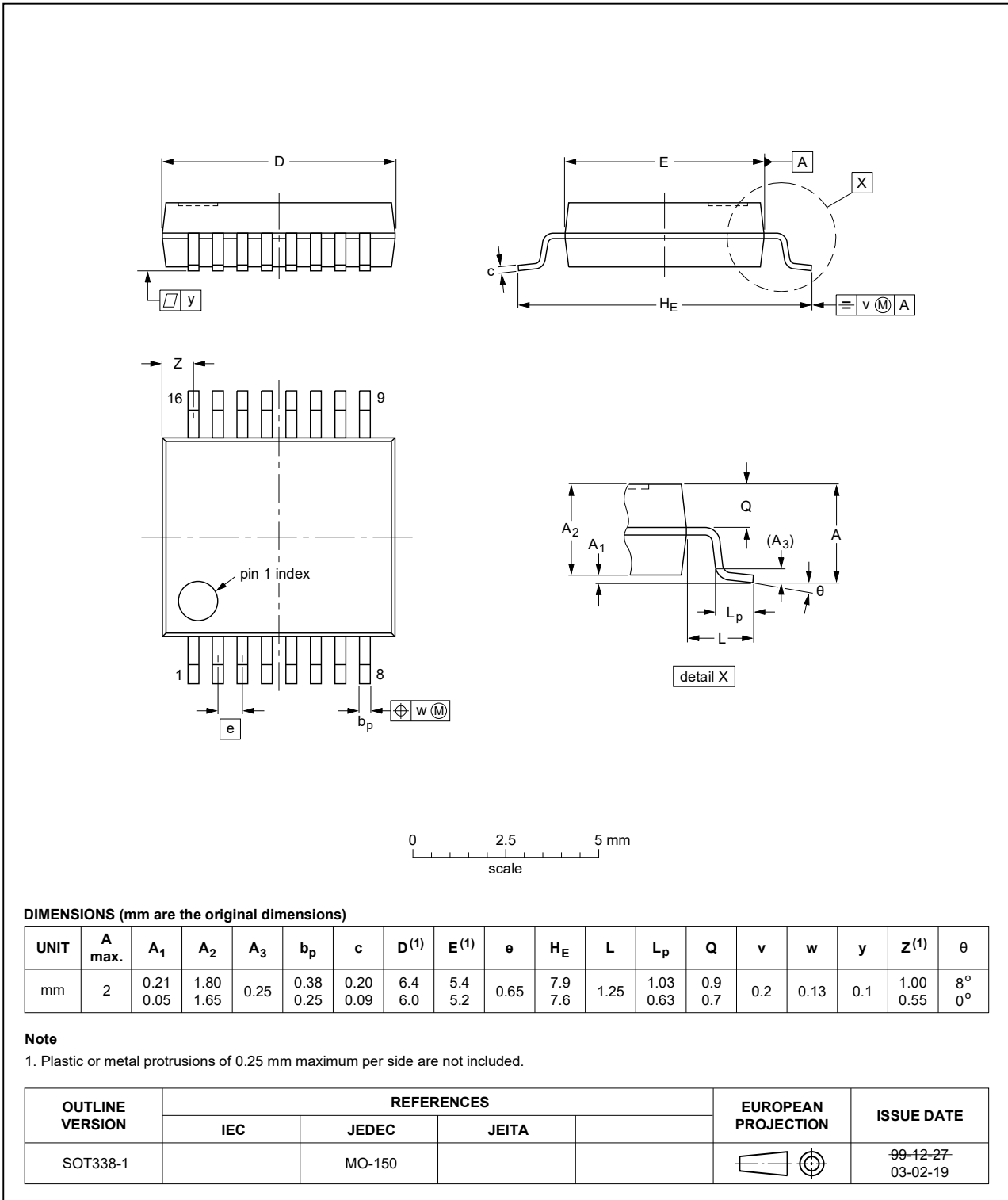


Fig. 16. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

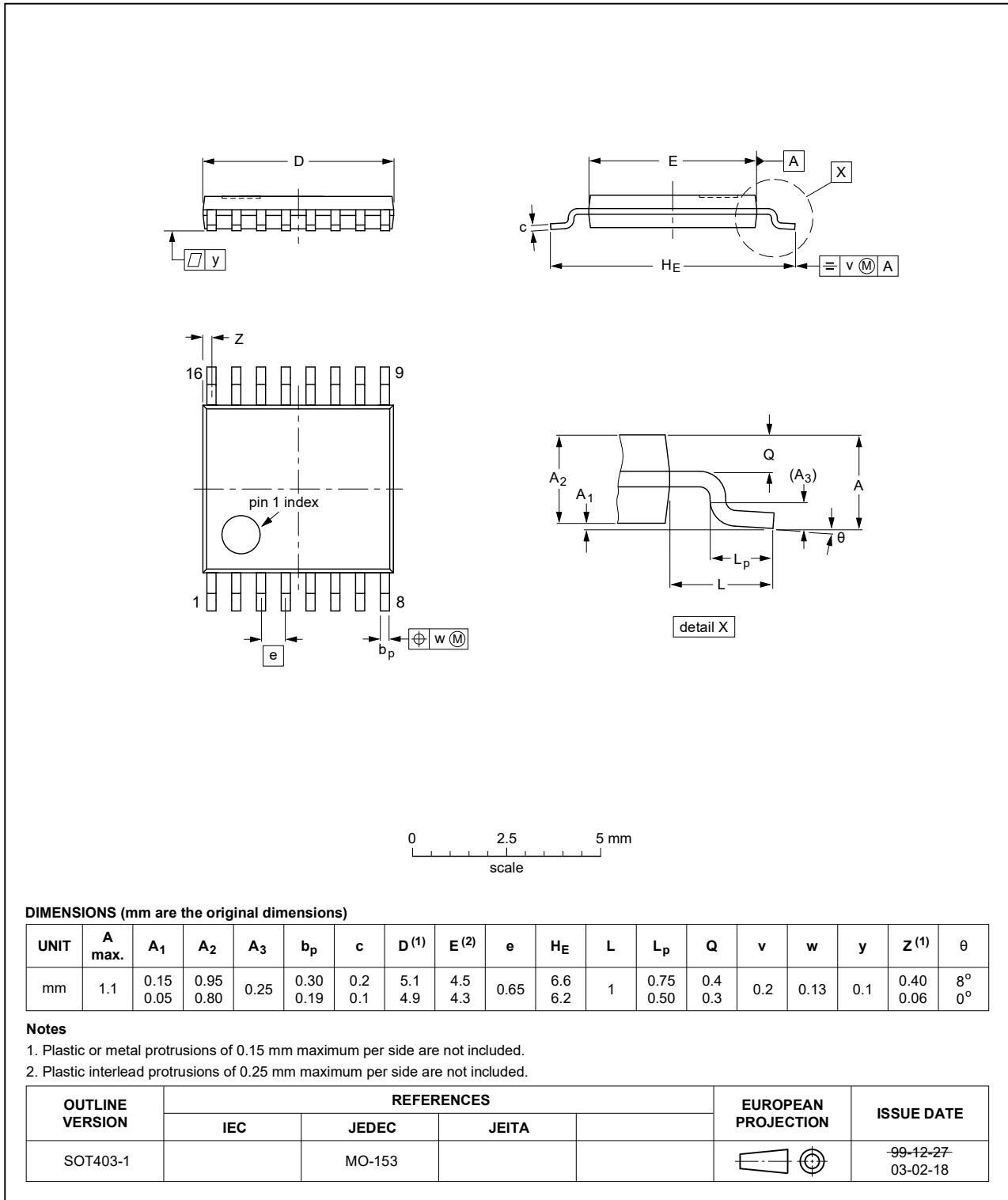


Fig. 17. Package outline SOT403-1 (TSSOP16)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT597 v.5	20211026	Product data sheet	-	74HC_HCT597 v.4
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type number 74HC597DB (SOT338-1/SSOP16) removed. Type number 74HCT597PW (SOT403-1/TSSOP16) added. Section 2 updated. Table 4: Derating values for P_{tot} total power dissipation updated. 			
74HC_HCT597 v.4	20160225	Product data sheet	-	74HC_HCT597 v.3
Modifications:	<ul style="list-style-type: none"> Type numbers 74HC597N and 74HCT597N (SOT38-4) removed. 			
74HC_HCT597 v.3	20140415	Product data sheet	-	74HC_HCT597_CNV v.2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. 			
74HC_HCT597_CNV v.2	19901201	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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Contents

1. General description	1
2. Features and benefits	1
3. Ordering information	1
4. Functional diagram	2
5. Pinning information	4
5.1. Pinning.....	4
5.2. Pin description.....	4
6. Functional description	5
7. Limiting values	6
8. Recommended operating conditions	6
9. Static characteristics	7
10. Dynamic characteristics	9
10.1. Waveforms and test circuit.....	12
11. Package outline	15
12. Abbreviations	18
13. Revision history	18
14. Legal information	19

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