PH2925U

N-channel TrenchMOS ultra low level FET

Rev. 04 — 24 February 2009 Product data sheet

1. Product profile

1.1 General description

Ultra low level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Higher operating power due to low thermal resistance
- Interfaces directly with low voltage gate drivers
- Low conduction losses due to low on-state resistance

1.3 Applications

- DC-to-DC convertors
- Notebook computers
- Portable equipment
- Switched-mode power supplies

1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C	-	-	25	V
I_D	drain current	$T_{mb} = 25$ °C; $V_{GS} = 4.5$ V; see Figure 1; see Figure 3	-	-	100	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2	-	-	62.5	W
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 4.5$ V; $I_D = 50$ A; $V_{DS} = 10$ V; $T_j = 25$ °C; see Figure 10; see Figure 11	-	20.2	-	nC
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5$ V; $I_D = 25$ A; $T_j = 25$ °C; see Figure 8; see Figure 9	-	2.3	3	mΩ

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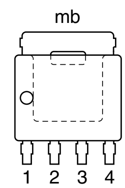
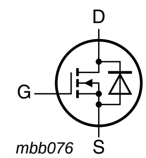
2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 **SOT669 (LFPAK)**	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

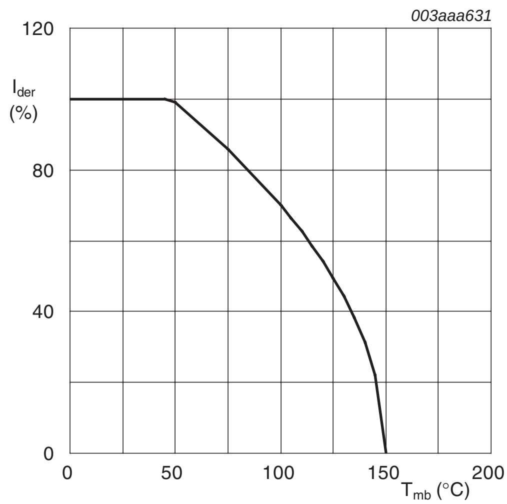
Type number	Package		
	Name	Description	Version
PH2925U	LFPAK	plastic single-ended surface-mounted package (LFPAK); 4 leads	SOT669

4. Limiting values

Table 4. Limiting values

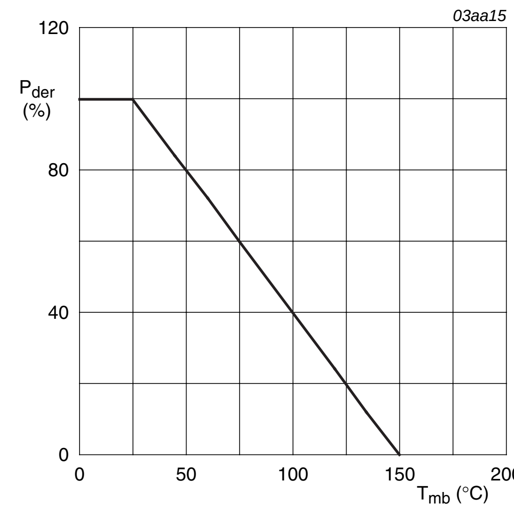
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C	-	25	V
V_{DGR}	drain-gate voltage	$T_j \leq 150$ °C; $T_j \geq 25$ °C; R_{GS} = 20 kΩ	-	25	V
V_{GS}	gate-source voltage		-10	10	V
I_D	drain current	V_{GS} = 4.5 V; T_{mb} = 100 °C; see Figure 1	-	70	A
		V_{GS} = 4.5 V; T_{mb} = 25 °C; see Figure 1; see Figure 3	-	100	A
I_{DM}	peak drain current	$t_p \leq 10$ µs; pulsed; T_{mb} = 25 °C; see Figure 3	-	300	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 2	-	62.5	W
T_{stg}	storage temperature		-55	150	°C
T_j	junction temperature		-55	150	°C
Source-drain diode					
I_S	source current	T_{mb} = 25 °C	-	52	A
I_{SM}	peak source current	$t_p \leq 10$ µs; pulsed; T_{mb} = 25 °C	-	150	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 70.7 A; $V_{sup} \leq 25$ V; unclamped; t_p = 0.22 ms; R_{GS} = 50 Ω	-	250	mJ



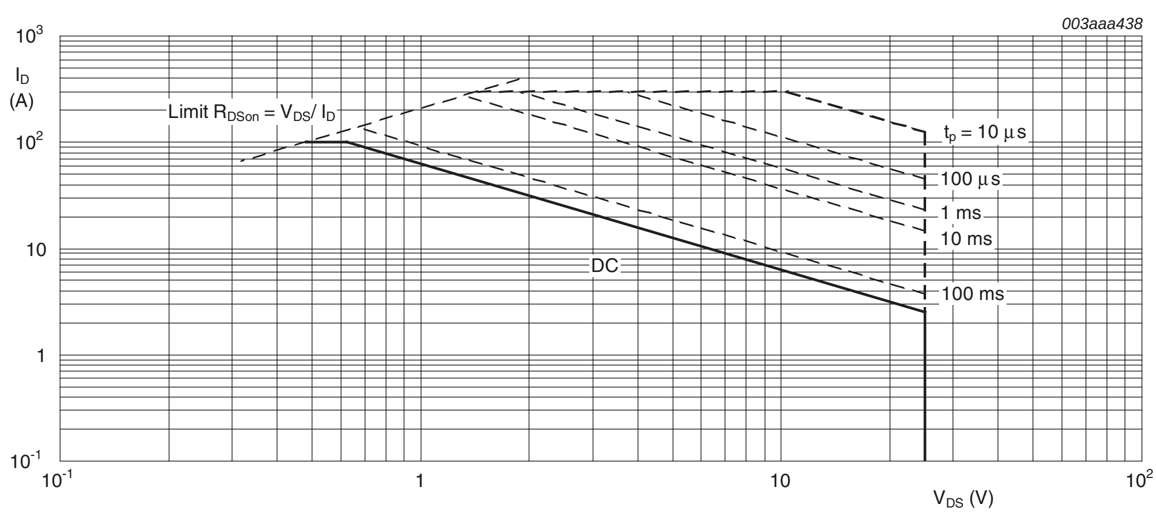
$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\,\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$$T_{mb} = 25°C; I_{DM} \text{ is single pulse}$$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	2	K/W

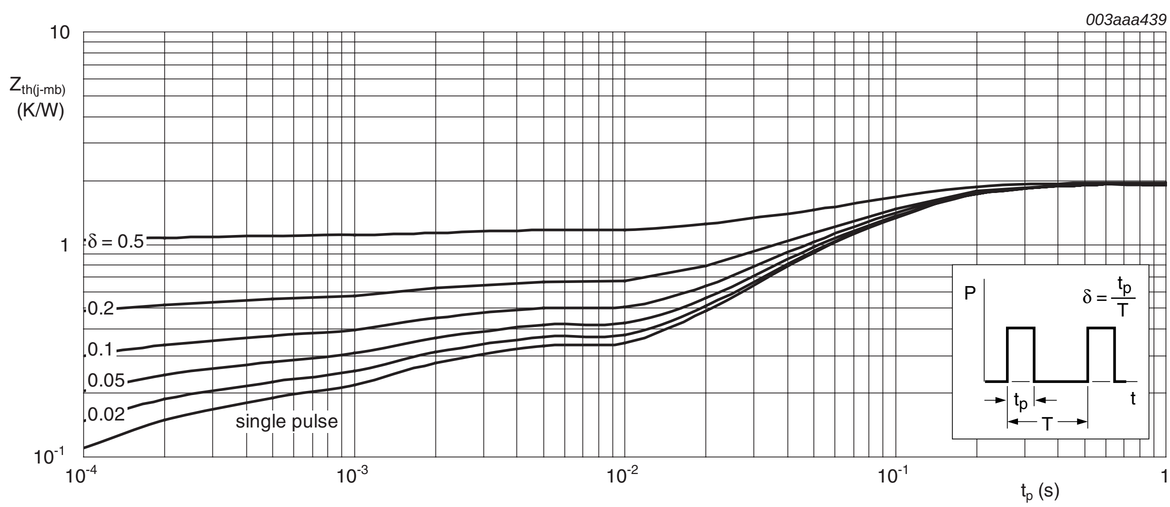
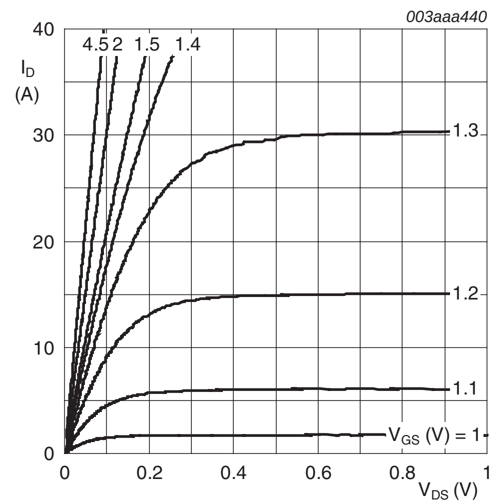


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

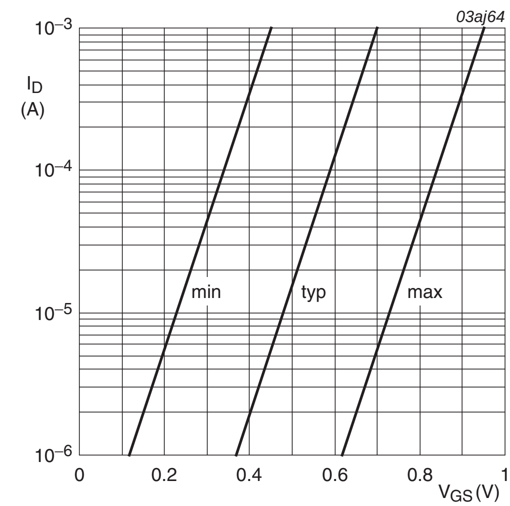
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	22.5	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	25	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 6; see Figure 7	-	-	1.2	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 150 °C; see Figure 6; see Figure 7	0.25	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 7; see Figure 6	0.45	0.7	0.95	V
I_{DSS}	drain leakage current	V_{DS} = 25 V; V_{GS} = 0 V; T_j = 150 °C	-	-	500	µA
		V_{DS} = 25 V; V_{GS} = 0 V; T_j = 25 °C	-	0.06	1	µA
I_{GSS}	gate leakage current	V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 °C	-	20	100	nA
		V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 °C	-	20	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 25 A; T_j = 150 °C; see Figure 8; see Figure 9	-	3.6	4.8	mΩ
		V_{GS} = 2.5 V; I_D = 25 A; T_j = 25 °C	-	3.2	4.2	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C; see Figure 8; see Figure 9	-	2.3	3	mΩ
R_G	internal gate resistance (AC)	f = 1 MHz; T_j = 25 °C	-	1.55	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 50 A; V_{DS} = 10 V; V_{GS} = 4.5 V; T_j = 25 °C; see Figure 10; see Figure 11	-	92	-	nC
Q_{GS}	gate-source charge		-	12	-	nC
Q_{GD}	gate-drain charge		-	20.2	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 50 A; V_{DS} = 10 V; T_j = 25 °C; see Figure 10; see Figure 11	-	1.6	-	V
C_{iss}	input capacitance	V_{DS} = 10 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; see Figure 12	-	6150	-	pF
C_{oss}	output capacitance		-	1170	-	pF
C_{rss}	reverse transfer capacitance		-	814	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 10 V; R_L = 1 Ω; V_{GS} = 4.5 V; $R_{G(ext)}$ = 4.7 Ω; T_j = 25 °C	-	30	-	ns
t_r	rise time		-	80	-	ns
$t_{d(off)}$	turn-off delay time		-	258	-	ns
t_f	fall time		-	114	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 13	-	0.72	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 25 V	-	60	-	ns



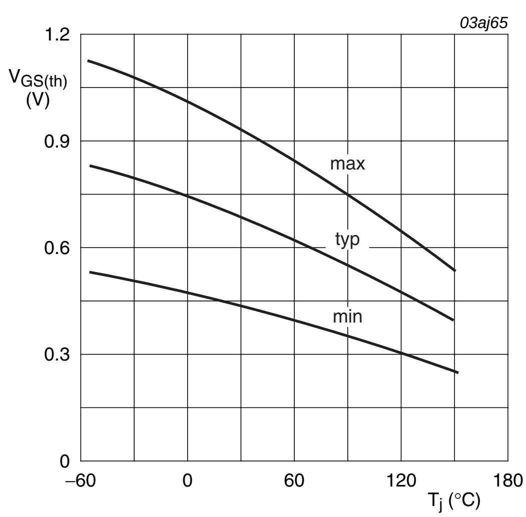
$T_j = 25°C$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



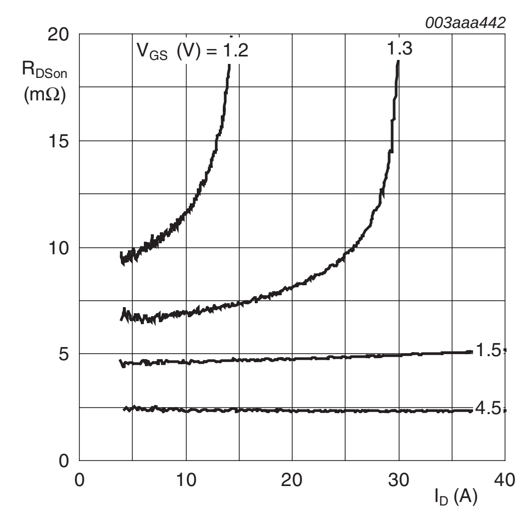
$T_j = 25°C; V_{DS} = 5V$

Fig 6. Sub-threshold drain current as a function of gate-source voltage



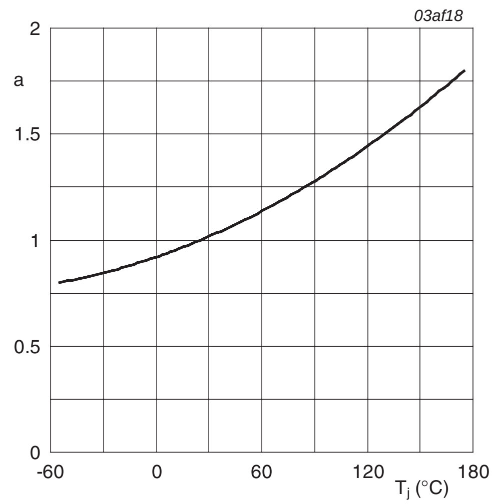
$I_D = 1mA; V_{DS} = V_{GS}$

Fig 7. Gate-source threshold voltage as a function of junction temperature



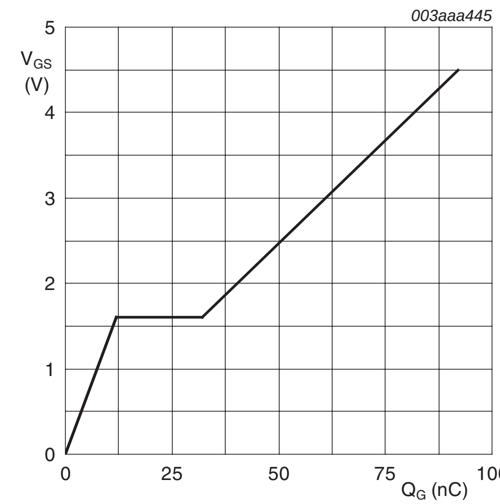
$T_j = 25°C$

Fig 8. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature



$$I_D = 50A; V_{DS} = 10V$$

Fig 10. Gate-source voltage as a function of gate charge; typical values

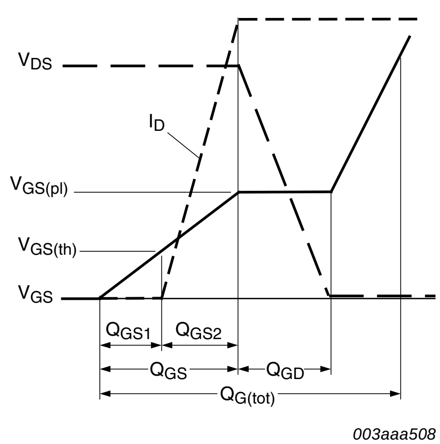
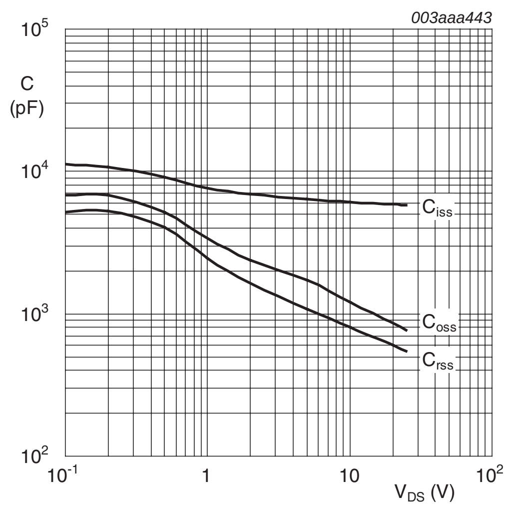
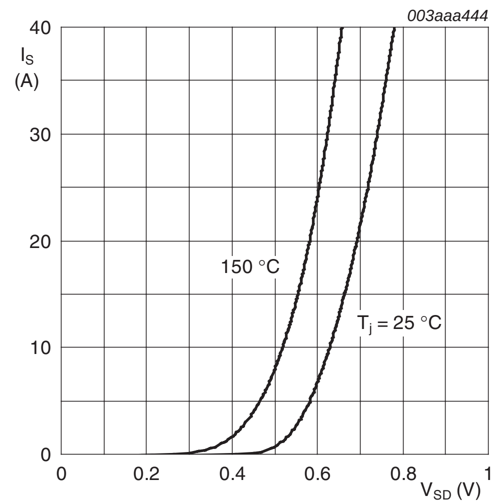


Fig 11. Gate charge waveform definitions



$$V_{GS} = 0V; f = 1MHz$$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

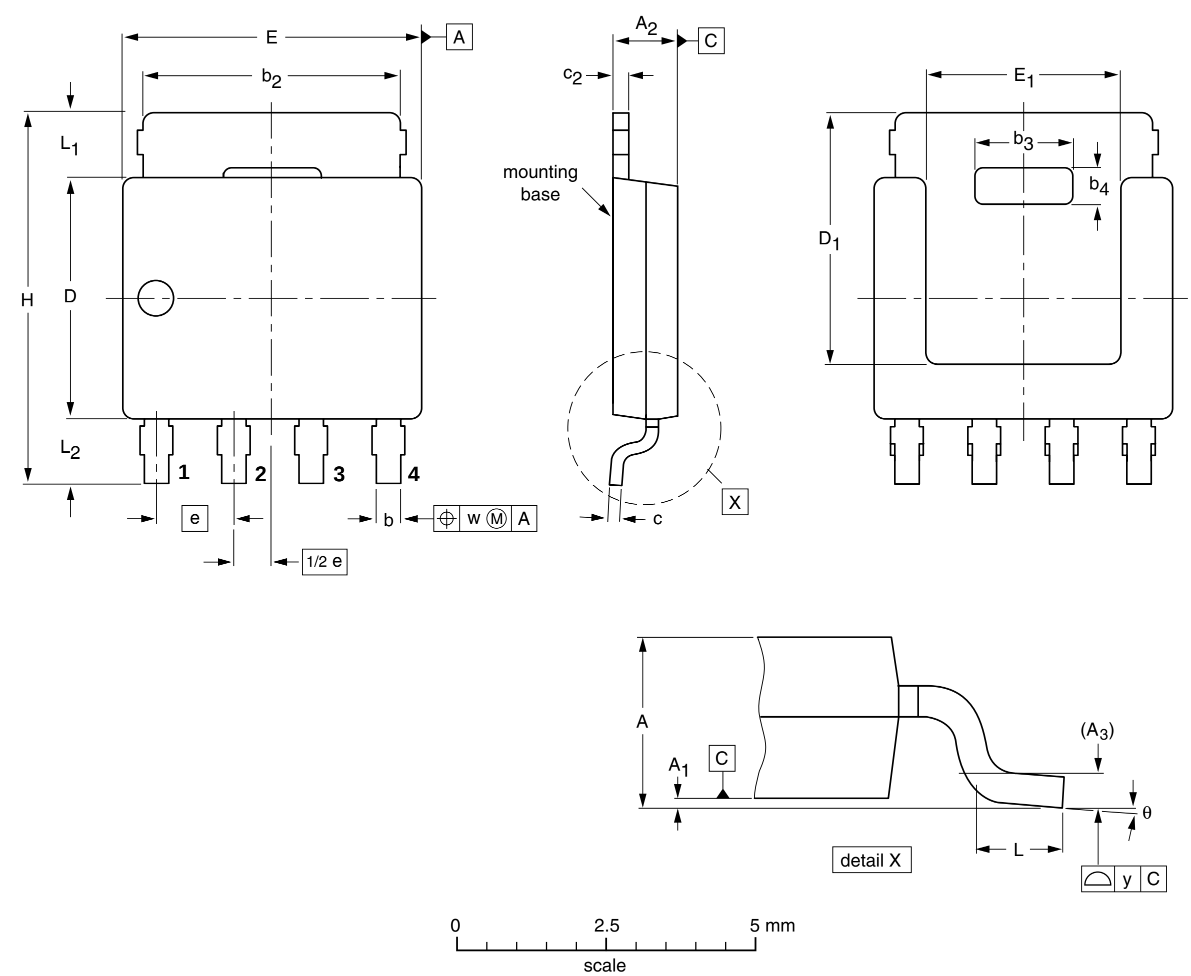


$T_j = 25°C$ and $150°C; V_{GS} = 0V$

Fig 13. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LFPAK); 4 leads **SOT669**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	A_2	A_3	b	b_2	b_3	b_4	c	c_2	D(1)	D_1(1) max	E(1)	E_1(1)	e	H	L	L_1	L_2	w	y	θ
mm	1.20 1.01	0.15 0.00	1.10 0.95	0.25	0.50 0.35	4.41 3.62	2.2 2.0	0.9 0.7	0.25 0.19	0.30 0.24	4.10 3.80	4.20	5.0 4.8	3.3 3.1	1.27	6.2 5.8	0.85 0.40	1.3 0.8	1.3 0.8	0.25	0.1	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

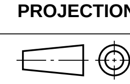
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT669		MO-235				~~04-10-13~~ 06-03-16

Fig 14. Package outline SOT669 (LFPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PH2925U_4	20090224	Product data sheet	-	PH2925U_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
PH2925U_3	20051129	Product data sheet	-	PH2925U-02
PH2925U-02 (9397 750 13064)	20040408	Product data	-	PH2925U-01
PH2925U-01 (9397 750 11407)	20030502	Product data	-	-

9. Legal information

9.1 Data sheet status

Document status [1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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11. Contents

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