74LVT14

3.3 V hex inverter Schmitt trigger

Rev. 4 — 28 July 2021

Product data sheet

1. General description

The 74LVT14 is a hex inverter with Schmitt-trigger inputs. Bus hold data inputs eliminate the need for external pull-up resistors to define unused inputs. This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- · Different positive and negative going input threshold voltages
- · Tolerant of slow input transitions
- Wide supply voltage range from 2.7 to 3.6 V
- Overvoltage tolerant inputs to 5.5 V
- · BiCMOS high speed and output drive
- Output capability: +32 mA/-20 mA
- High noise immunity
- · Direct interface with TTL levels
- · No bus current loading when output is tied to 5 V bus
- · Power-up 3-state
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up protection exceeds 500 mA per JESD78 class II level A
- Complies with JEDEC standard JESD8C (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114E exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C

3. Ordering information

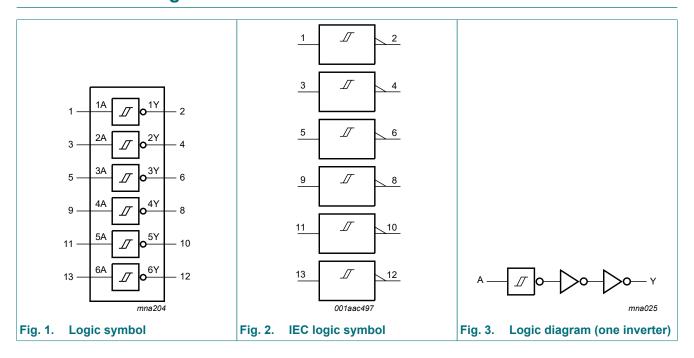
Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVT14D	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVT14PW	-40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVT14BQ	-40 °C to +85 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1



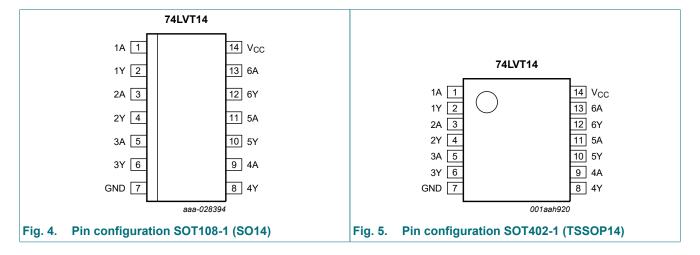
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4. Functional diagram



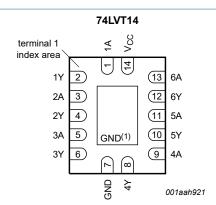
5. Pinning information

5.1. Pinning



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Transparent top view

(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

Fig. 6. Pin configuration SOT762-1 (DHVQFN14)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V _{CC}	14	positive supply voltage

6. Functional description

Table 3. Function selection

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level.$

Inputs	Output
nA	nY
L	Н
Н	L

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7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
VI	input voltage	[1]	-0.5	+7.0	V
Vo	output voltage	output in OFF or HIGH state [1]	-0.5	+7.0	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
Io	output current	output in LOW state	-	64	mA
		output in HIGH state	-32	-	mA
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature	[2]	-	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +85 ^{\circ}\text{C}$ [3]	-	500	mW

^[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{CC}	supply voltage		2.7	-	3.6	V
VI	input voltage		0	-	5.5	V
I _{OH}	HIGH-level output current		-20	-	-	mA
I _{OL}	LOW-level output current		-	-	32	mA
T _{amb}	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	output enabled	0	-	10	ns/V

^[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

^[3] For SOT402-1 (TSSOP14) package: Ptot derates linearly with 7.3 mW/K above 81 °C.

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9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40	°C to +85	°C	Unit
			Min	Typ[1]	Max	
V _{T+}	positive-going threshold voltage	V _{CC} = 3.3 V; see <u>Fig. 7</u>	1.5	1.7	2.0	V
V _{T-}	negative-going threshold voltage	V _{CC} = 3.3 V; see <u>Fig. 7</u>	0.9	1.1	1.3	V
V _H	hysteresis voltage	V _{CC} = 3.3 V; see <u>Fig. 7</u>	0.4	0.6	-	V
V_{IK}	input clamping voltage	V _{CC} = 2.7 V; I _{IK} = -18 mA	-1.2	-	-	V
V _{OH}	HIGH-level output voltage	V _{CC} = 2.7 V to 3.6 V; I _{OH} = -100 μA	V _{CC} - 0.2	-	-	V
		V _{CC} = 2.7 V; I _{OH} = -6 mA	2.4	-	-	V
		V _{CC} = 3.0 V; I _{OH} = -20 mA	2.0	-	-	V
V _{OL}	LOW-level output voltage	V _{CC} = 2.7 V; I _{OL} = 100 μA	-	-	0.2	V
		V _{CC} = 2.7 V; I _{OL} = 24 mA	-	-	0.5	V
		V _{CC} = 3.0 V; I _{OL} = 32 mA	-	-	0.5	V
I _I	input leakage current	V _{CC} = 0 V or 3.6 V; V _I = 5.5 V	-	-	10	μΑ
		$V_{CC} = 3.6 \text{ V}; V_I = V_{CC} \text{ or GND}$	-	-	±1	μΑ
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O = 0 V to 4.5 V	-	-	±100	μΑ
I _{CC}	supply current	$V_{CC} = 3.6 \text{ V}; V_{I} = \text{GND or } V_{CC}; I_{O} = 0 \text{ A}$				
		outputs HIGH	-	-	0.02	mA
		outputs LOW	-	1.5	3	mA
Δl _{CC}	additional supply current	per input pin; V_{CC} = 3.0 V to 3.6 V; one input = V_{CC} - 0.6 V and other inputs at V_{CC} or GND	-	-	0.2	mA
Cı	input capacitance	V _I = 0 V or 3.0 V	-	3	-	pF

^[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 9.

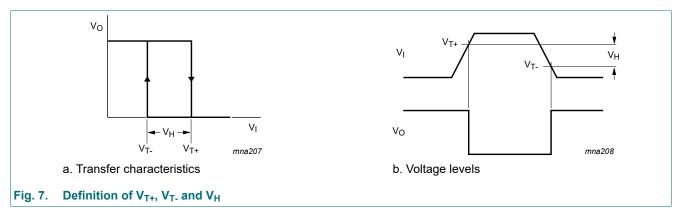
Symbol	Parameter	Conditions	-40 °C to +85 °C			
			Min	Typ [1]	Max	
t_{PLH}	LOW to HIGH propagation delay	nA to nY; see Fig. 8				
		V _{CC} = 2.7 V	-	-	6.9	ns
		V _{CC} = 3.3 V + 0.3 V	1.0	3.8	5.7	ns
t _{PHL}	HIGH to LOW propagation delay	nA to nY; see Fig. 8				
		V _{CC} = 2.7 V	-	-	4.1	ns
		$V_{CC} = 3.3 \text{ V} + 0.3 \text{ V}$	1.0	3.2	4.5	ns

^[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 3.3 V.

^[2] This is the increase in the supply current for each input at the specified voltage level other than V_{CC} or GND.

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10.1. Waveforms and test circuit



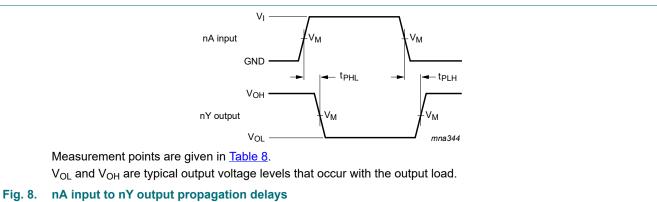
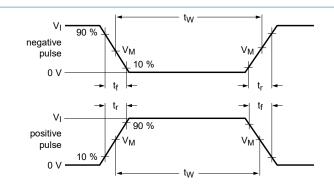
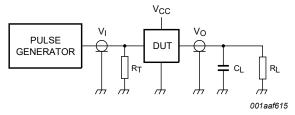


Table 8. Measurement points

V _{CC}	Input	Output
	V _M	V _M
2.7 V to 3.6 V	1.5 V	1.5 V

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Test data is given in given in Table 9.

Definitions for test circuit:

R_L = Load resistance;

 C_L = Load capacitance including jig and probe capacitance;

 R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator.

Fig. 9. Test circuit for measuring switching times

Table 9. Test data

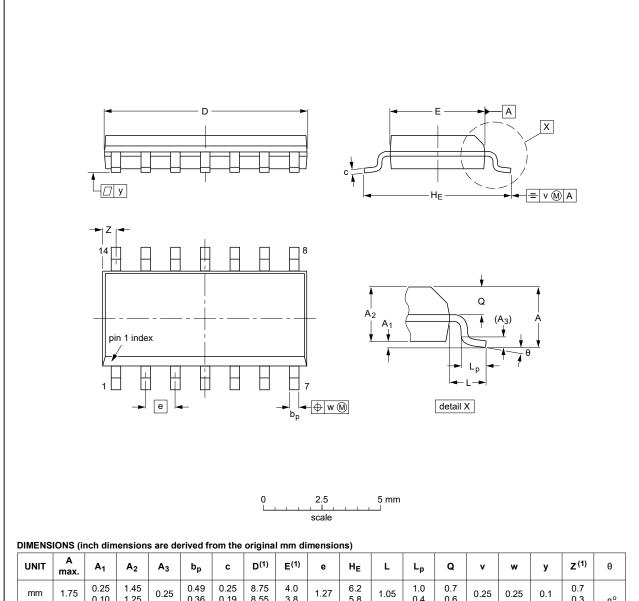
Supply	Input Load			nput L					
V _{CC}	V _I	f _i	t _W	t _r , t _f	R _L	CL			
2.7 V to 3.3 V	2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	500 Ω	50 pF			

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11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	0°

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

	OUTLINE		REFER	EUROPEAN	ISSUE DATE		
'	VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
	SOT108-1	076E06	MS-012				99-12-27 03-02-19

Fig. 10. Package outline SOT108-1 (SO14)

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

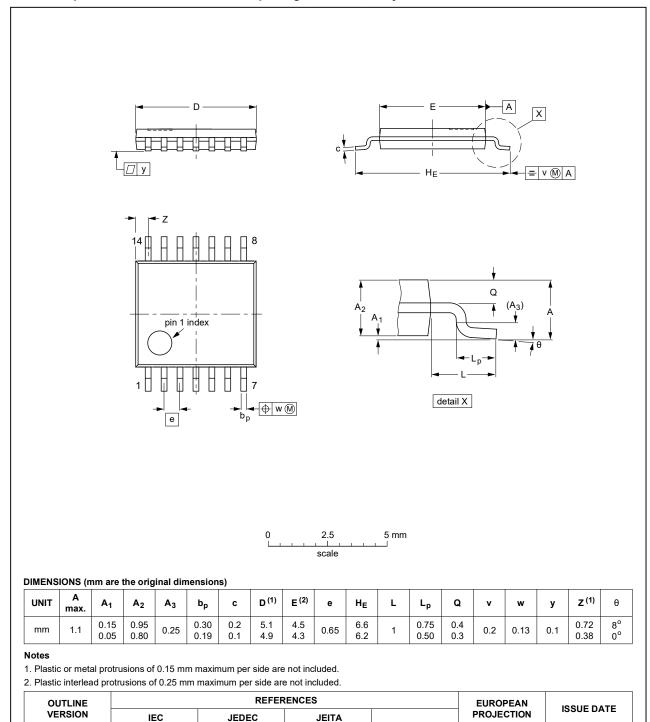


Fig. 11. Package outline SOT402-1 (TSSOP14)

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SOT402-1

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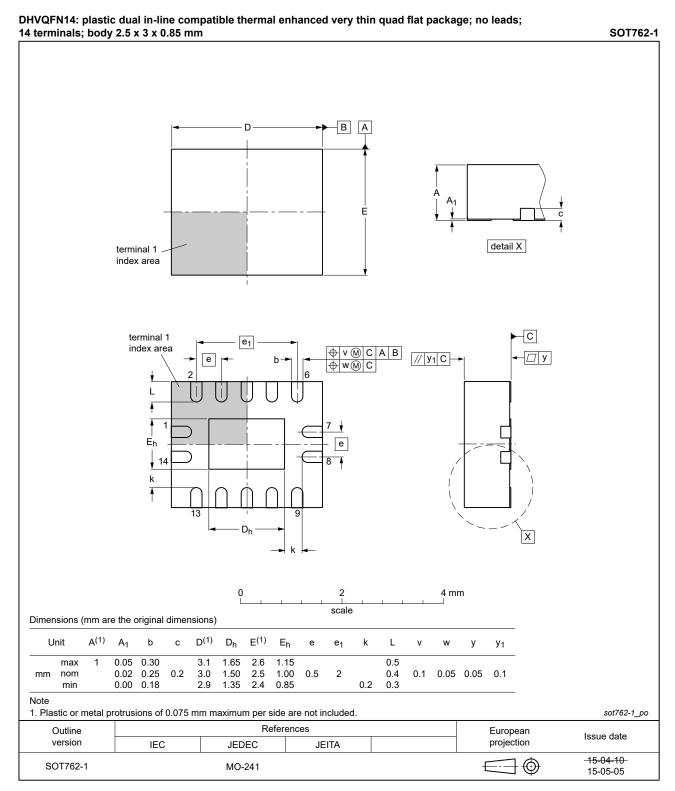


Fig. 12. Package outline SOT762-1 (DHVQFN14)

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12. Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
74LVT14 v.4	20210728	Product data sheet	-	74LVT14 v.3		
Modifications:	• <u>Section 1</u> and	Occident and Occident updated.				
74LVT14 v.3	20180406	Product data sheet	-	74LVT14 v.2		
Modifications:	Nexperia.					
74LVT14 v.2	20080425	Product data sheet	-	74LVT14 v.1		
Modifications:	guidelines of Legal texts ha Quick referen	this data sheet has been redes NXP Semiconductors. ave been adapted to the new concessection removed. backage added to Section 3 and Ided.	ompany name where	•		
74LVT14 v.1	19960828	Product specification	-	-		

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14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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