74AHCV05A

Hex inverter Schmitt trigger with open-drain outputs Rev. 1 — 24 June 2019 Product data sheet

1. General description

The 74AHCV05A is a hex inverter with Schmitt trigger inputs and open-drain outputs. The outputs are open-drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

The data (nA) inputs include Schmitt trigger inputs capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 1.8 V to 5.5 V
- Typical t_{PZL} of 3.6 ns at 5 V
- Typical $V_{OL(p)}$ < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C
- Supports mixed-mode voltage operation on all ports
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA per JESD 78 Class II
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 3 kV
 - MM: JESD22-A115-A exceeds 150 V
 - CDM: ANSI/ESDA/JEDEC JS-002 Class C3, exceeds 2 kV
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

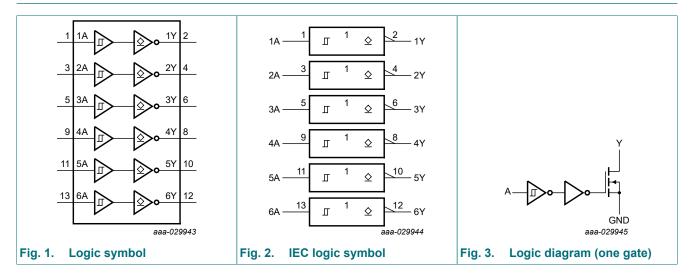
Table 1. Ordering information

Type number	Package					
	Temperature range	Name	Description	Version		
74AHCV05APW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1		



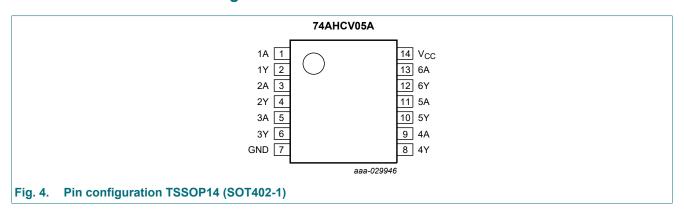
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4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

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6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state

Input	Output
nA	nY
L	Z
Н	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
VI	input voltage	[1]	-0.5	+7.0	V
V _O	output voltage	output LOW state, [2] 3-state or power-down	-0.5	+7.0	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
Io	output current	$V_O = 0 V \text{ to } V_{CC}$	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$ [3]	-	500	mW

The minimum input voltage ratings may be exceeded if the input current ratings are observed. The output voltage ratings may be exceeded if the output current ratings are observed.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{CC}	supply voltage		1.8	5.0	5.5	V
VI	input voltage		0	-	5.5	V
Vo	output voltage	output LOW state, 3-state or power-down	0	-	5.5	V
T _{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.3 V to 2.7 V	-	-	50	ms/V
		V _{CC} = 3.0 V to 3.6 V	-	-	20	ms/V
		V _{CC} = 4.5 V to 5.5 V	-	-	1	ms/V

For TSSOP14 packages: above 75 °C the value of Ptot derates linearly at 7 mW/K.

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9. Static characteristics

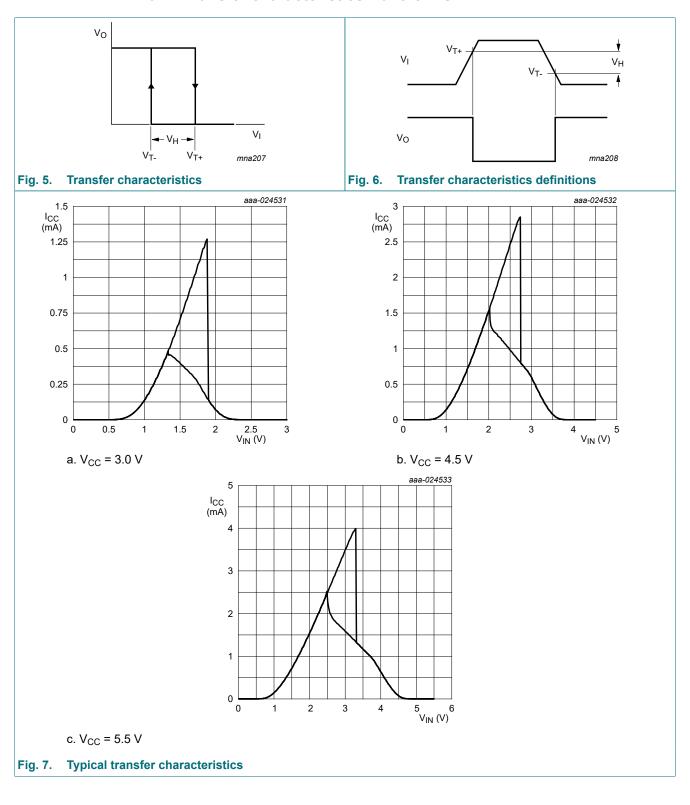
Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C		-40 °C to +85 °C		-40 °C to +125 °C		Unit	
			Min	Тур	Max	Min	Max	Min	Max	
V_{T+}	positive-going	V _{CC} = 1.8 V	-	-	1.65	-	1.65	-	1.65	V
	threshold voltage	V _{CC} = 2.3 V	-	-	1.85	-	1.85	-	1.85	V
	Voltage	V _{CC} = 3.0 V	-	-	2.2	-	2.2	-	2.2	V
		V _{CC} = 4.5 V	-	-	3.15	-	3.15	-	3.15	V
		V _{CC} = 5.5 V	-	-	3.85	-	3.85	-	3.85	V
V _{T-}	negative-going	V _{CC} = 1.8 V	0.15	-	-	0.15	-	0.15	-	V
	threshold voltage	V _{CC} = 2.3 V	0.45	-	-	0.45	-	0.45	-	V
	Voltage	V _{CC} = 3.0 V	0.9	-	-	0.9	-	0.9	-	V
		V _{CC} = 4.5 V	1.35	-	-	1.35	-	1.35	-	V
		V _{CC} = 5.5 V	1.65	-	-	1.65	-	1.65	-	V
V_{H}	hysteresis	V _{CC} = 1.8 V	0.15	-	1.05	0.15	1.05	0.15	1.05	V
	voltage	V _{CC} = 2.3 V	0.2	-	1.1	0.2	1.1	0.2	1.1	V
		V _{CC} = 3.0 V	0.3	-	1.2	0.3	1.2	0.3	1.2	V
		V _{CC} = 4.5 V	0.4	-	1.4	0.4	1.4	0.4	1.4	V
		V _{CC} = 5.5 V	0.5	-	1.6	0.5	1.6	0.5	1.6	V
V_{OL}	LOW-level	$V_I = V_{T+}$ or V_{T-}								
	output voltage	I _O = 50 μA; V _{CC} = 1.8 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 8 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.36	-	0.44	-	0.44	V
		I _O = 16 mA; V _{CC} = 4.5 V	-	-	0.44	-	0.55	-	0.55	V
I _{OZ}	OFF-state output current	V_{CC} = 5.5 V; V_I = V_{IH} or V_{IL} ; V_O = GND to 5.5 V	-	-	±0.25	-	±2.5	-	±2.5	μA
I _{OFF}	power-off leakage current	V_I or V_O = GND to 5.5 V; V_{CC} = 0 V	-	-	0.5	-	5	-	5	μΑ
l _l	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 0$ V to 5.5 V	-	-	±0.1	-	±1	-	±1	μA
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	2	-	20	-	20	μΑ

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9.1. Transfer characteristics waveforms



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10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V. For test circuit see Fig. 9.

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to	+125 °C	Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t _{PZL}	OFF-state to LOW	nA to nY; see Fig. 8								
	propagation delay	V _{CC} = 2.3 V to 2.7 V								
		C _L = 15 pF	-	5.8	12.2	1	15	1	17	ns
		C _L = 50 pF	-	8.2	16.6	1	19.5	1	21.5	ns
		V _{CC} = 3.0 V to 3.6 V								
		C _L = 15 pF	-	4.6	7.1	1	8.5	1	10.0	ns
		C _L = 50 pF	-	6.5	10.6	1	12	1	13.5	ns
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	3.6	5.5	1	6.5	1	7.5	ns
		C _L = 50 pF	-	5.3	7.5	1	8.5	1	9.5	ns
t _{PLZ}	LOW to OFF-state	nA to nY; see Fig. 8								
	propagation delay	V _{CC} = 2.3 V to 2.7 V								
		C _L = 15 pF	-	5.4	10.5	1	12.0	1	14.0	ns
		C _L = 50 pF	-	10.0	15.2	1	18	1	20.0	ns
		V _{CC} = 3.0 V to 3.6 V								
		C _L = 15 pF	-	4.3	7.2	1	9.0	1	10.5	ns
		C _L = 50 pF	-	7.7	10.6	1	12	1	13.5	ns
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	3.4	5.5	1	6.5	1	7.5	ns
		C _L = 50 pF	-	5.6	7.5	1	8.5	1	9.5	ns
Cı	input capacitance	$V_I = V_{CC}$ or GND; $V_{CC} = 3.3 \text{ V}$	-	2	6	-	6	-	6	pF
Co	output capacitance	$V_O = V_{CC}$ or GND; $V_{CC} = 3.3 \text{ V}$	-	5	-	-	-	-	-	pF
C _{PD}	power dissipation capacitance	per buffer; $C_L = 0$ pF; [2] $f = 10$ MHz; $V_{CC} = 5$ V; $V_I = GND$ to V_{CC}	-	3	-	-	-	-	-	pF

Typical values are measured at T_{amb} = 25 °C and V_{CC} = 2.5 V, 3.3 V, and 5 V respectively, unless otherwise specified. C_{PD} is used to determine the dynamic power dissipation P_D (μ W).

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 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

 f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts.

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Table 8. Noise characteristics

GND = 0 V. For test circuit see Fig. 9.

Symbol	Parameter	Conditions	1	T _{amb} = 25 °C			
			Min	Тур	Max		
V _{CC} = 3.3	V; C _L = 50 pF					'	
$V_{OL(p)}$	LOW-level output voltage (peak)		-	0.3	0.8	V	
V _{OL(v)}	LOW-level output voltage (valley)		-0.8	-0.1	-	V	
V _{IH(AC)}	AC HIGH-level input voltage (dynamic)		2.31	-	-	V	
V _{IL(AC)}	AC LOW-level input voltage (dynamic)		-	-	0.99	V	
V _{CC} = 5.0	V; C _L = 50 pF					·	
V _{OL(p)}	LOW-level output voltage (peak)		-	0.6	-	V	
√ _{OL(v)}	LOW-level output voltage (valley)		-	-0.4	-	V	
V _{IH(AC)}	AC HIGH-level input voltage (dynamic)		3.5	-	-	V	
V _{IL(AC)}	AC LOW-level input voltage (dynamic)		-	-	1.5	V	

10.1. Waveforms and test circuit

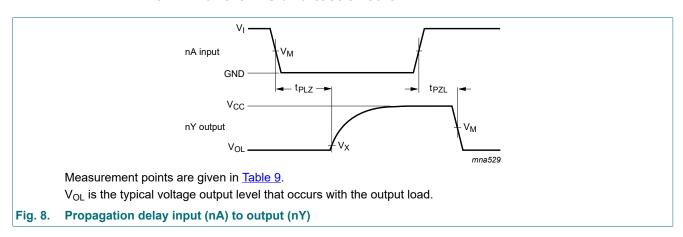
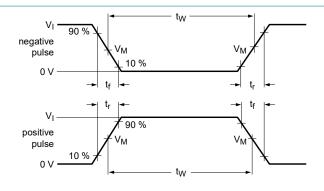
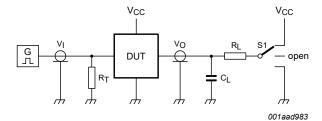


Table 9. Measurement points

Input	Dutput			
V_{M}	V _M	V_X		
0.5 × V _{CC}	0.5 × V _{CC}	V _{OL} + 0.3 V		

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Test data is given in Table 10.

Definitions test circuit:

 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator

 C_L = Load capacitance including jig and probe capacitance

R_L = Load resistance

S1 = Test selection switch

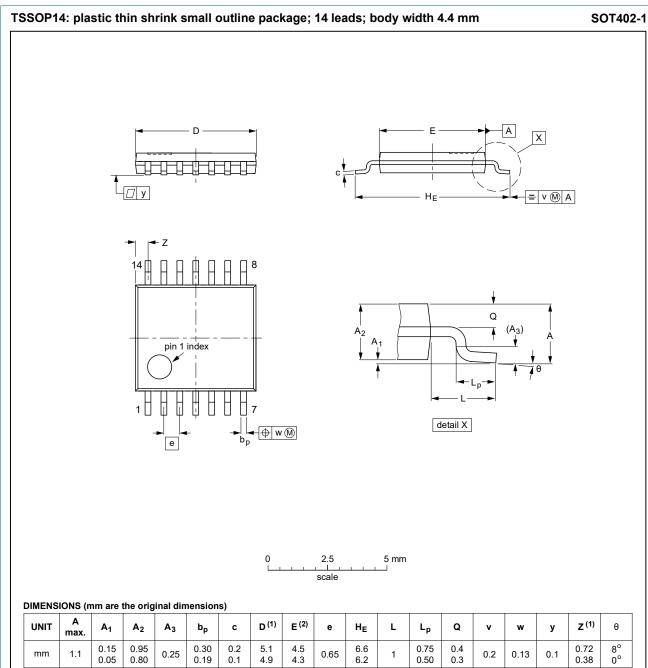
Fig. 9. Test circuit for measuring switching times

Table 10. Test data

Input		Load	S1 position	
V_{I}	t _r , t _f	CL	R_L	t _{PLZ} , t _{PZL}
GND to V _{CC}	3.0 ns	15 pF, 50 pF	1 kΩ	V _{CC}

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11. Package outline



Notos

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFERENCES			EUROPEAN ISSUE DAT		
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT402-1		MO-153				99-12-27 03-02-18	

Fig. 10. Package outline SOT402-1 (TSSOP14)

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12. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charge Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model

13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHCV05A v.1	20190624	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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