



# PMPB09R5VP

12 V, P-channel Trench MOSFET

10 February 2021

Product data sheet

## 1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless medium power DFN2020M-6 (SOT1220-2) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Low threshold voltage
- Trench MOSFET technology
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- Exposed drain pad for excellent thermal conduction

## 3. Applications

- Charging switch for portable devices
- DC-to-DC converters
- Power management in battery-driven portable devices
- Computing power management

## 4. Quick reference data

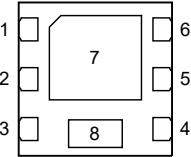
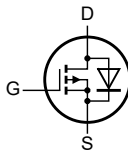
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ }^\circ\text{C}$	-	-	-12	V
$V_{GS}$	gate-source voltage		-8	-	8	V
$I_D$	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ }^\circ\text{C}; t \leq 5\text{ s}$	[1]	-	-15	A
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}; I_D = -10.5\text{ A}; T_j = 25\text{ }^\circ\text{C}$	-	9.5	12	m $\Omega$

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 <p>Transparent top view <b>DFN2020M-6 (SOT1220-2)</b></p>	 <p>017aaa094</p>
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		
7	D	drain		
8	S	source		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMPB09R5VP	DFN2020M-6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm	SOT1220-2

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PMPB09R5VP	ZJ

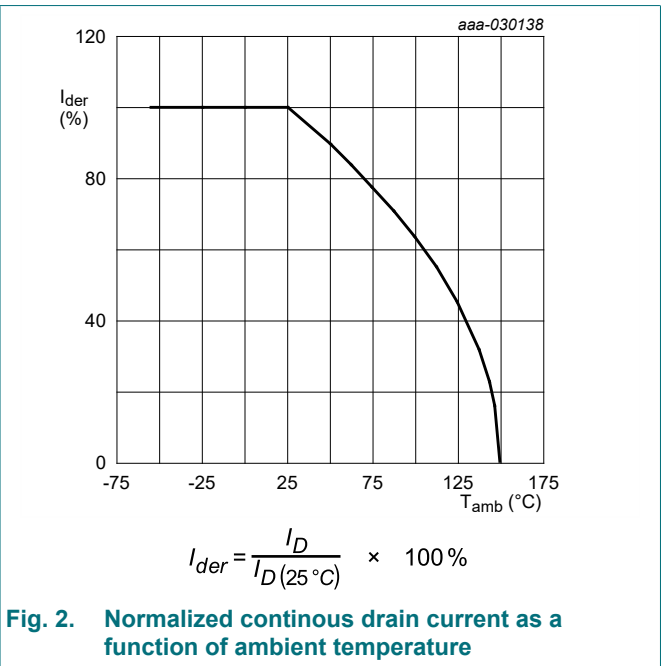
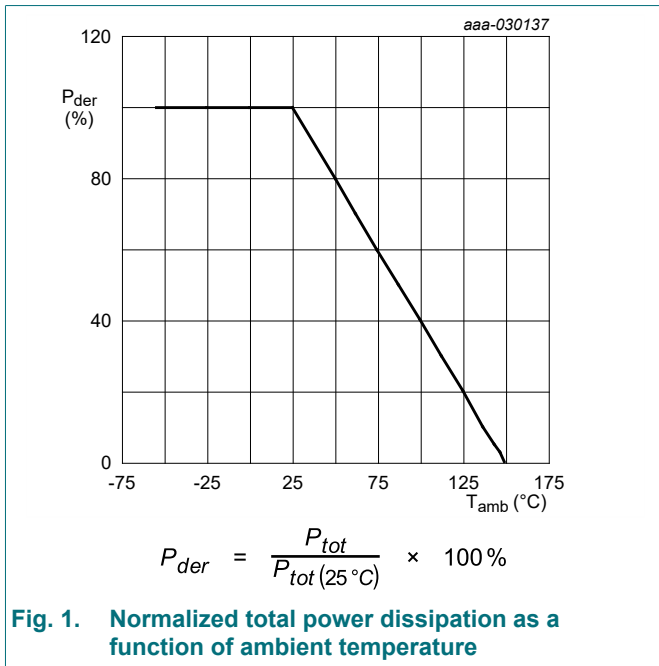
## 8. Limiting values

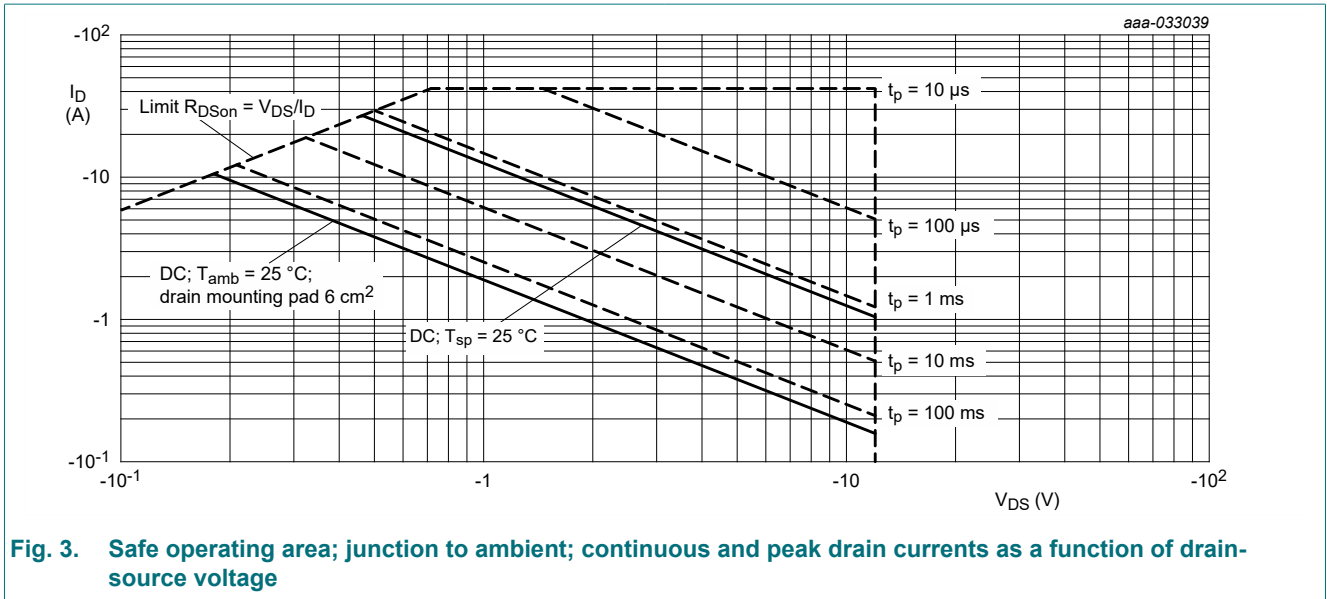
**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C		-	-12	V
V <sub>GS</sub>	gate-source voltage			-8	8	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = -4.5 V; T <sub>amb</sub> = 25 °C; t ≤ 5 s	[1]	-	-15	A
		V <sub>GS</sub> = -4.5 V; T <sub>amb</sub> = 25 °C	[1]	-	-10.5	A
		V <sub>GS</sub> = -4.5 V; T <sub>amb</sub> = 100 °C	[1]	-	-6.6	A
I <sub>DM</sub>	peak drain current	T <sub>amb</sub> = 25 °C; single pulse; t <sub>p</sub> ≤ 10 μs		-	-42	A
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C; t ≤ 5 s	[1]	-	3.8	W
		T <sub>amb</sub> = 25 °C	[1]	-	1.9	W
		T <sub>sp</sub> = 25 °C		-	12.5	W
T <sub>j</sub>	junction temperature			-55	150	°C
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>amb</sub> = 25 °C	[1]	-	-1.8	A

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.





### 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	223	256	K/W
			[2]	-	57	66	K/W
		in free air; $t \leq 5$ s	[2]	-	29	33	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	6	10	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.

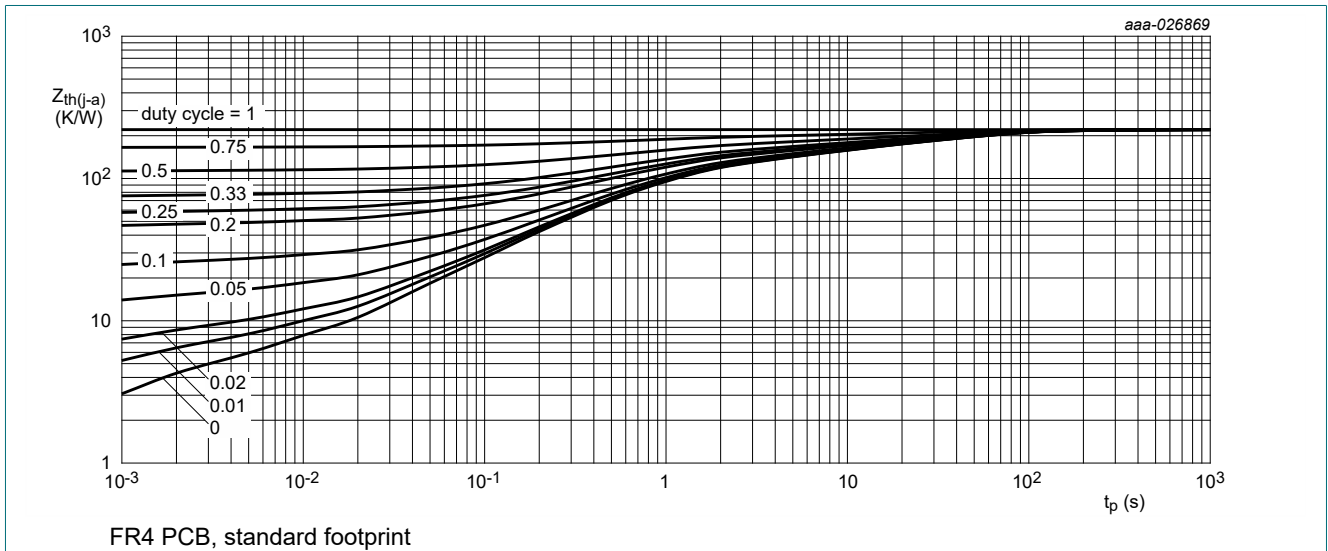


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

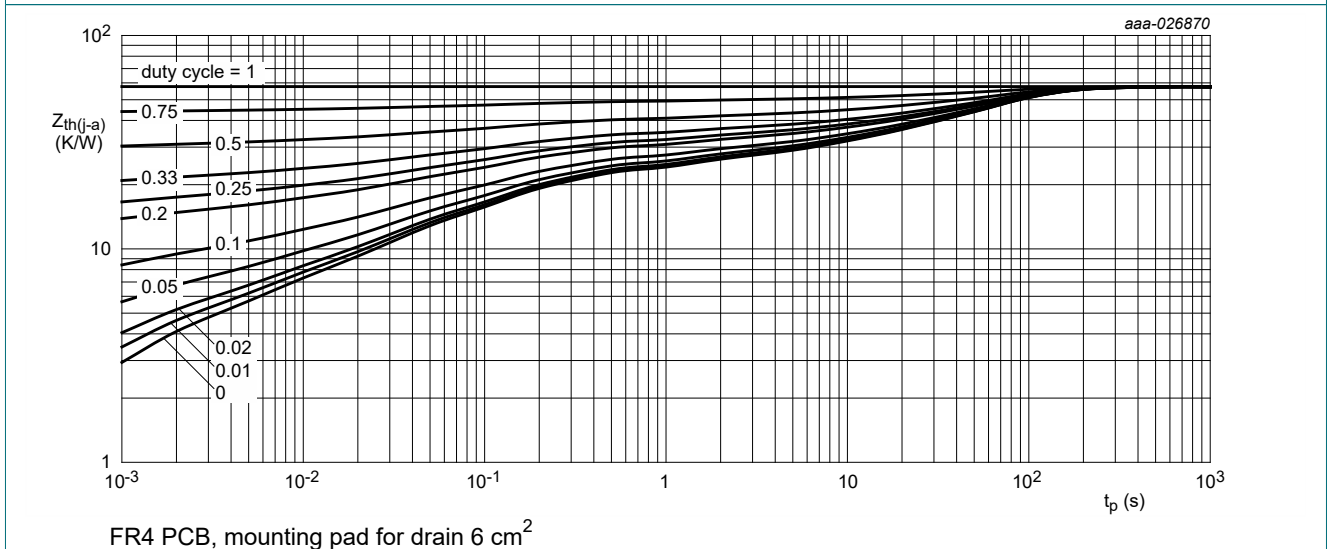


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu\text{A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-12	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = -250 \mu\text{A}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-0.4	-0.65	-0.9	V
$I_{DSS}$	drain leakage current	$V_{DS} = -12 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-1	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = -8 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-100	nA
		$V_{GS} = 8 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}$ ; $I_D = -10.5 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	9.5	12	m $\Omega$
		$V_{GS} = -4.5 \text{ V}$ ; $I_D = -10.5 \text{ A}$ ; $T_j = 150 \text{ }^\circ\text{C}$	-	14	17	m $\Omega$
		$V_{GS} = -2.5 \text{ V}$ ; $I_D = -8.8 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	13	17	m $\Omega$
		$V_{GS} = -1.8 \text{ V}$ ; $I_D = -3 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	20	32	m $\Omega$
		$V_{GS} = -1.5 \text{ V}$ ; $I_D = -0.5 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	30	75	m $\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = -10 \text{ V}$ ; $I_D = -10.3 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	27.3	-	S
$R_G$	gate resistance	$f = 1 \text{ MHz}$	-	5.3	-	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -6 \text{ V}$ ; $I_D = -10.3 \text{ A}$ ; $V_{GS} = -4.5 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	32	46	nC
$Q_{GS}$	gate-source charge		-	4.3	-	nC
$Q_{GD}$	gate-drain charge		-	10.3	-	nC
$C_{iss}$	input capacitance	$V_{DS} = -6 \text{ V}$ ; $f = 1 \text{ MHz}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	2700	-	pF
$C_{oss}$	output capacitance		-	700	-	pF
$C_{rss}$	reverse transfer capacitance		-	650	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -6 \text{ V}$ ; $I_D = -10 \text{ A}$ ; $V_{GS} = -4.5 \text{ V}$ ; $R_{G(ext)} = 6 \text{ } \Omega$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	6	-	ns
$t_r$	rise time		-	24	-	ns
$t_{d(off)}$	turn-off delay time		-	86	-	ns
$t_f$	fall time		-	69	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = -1.8 \text{ A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-0.7	-1.2	V

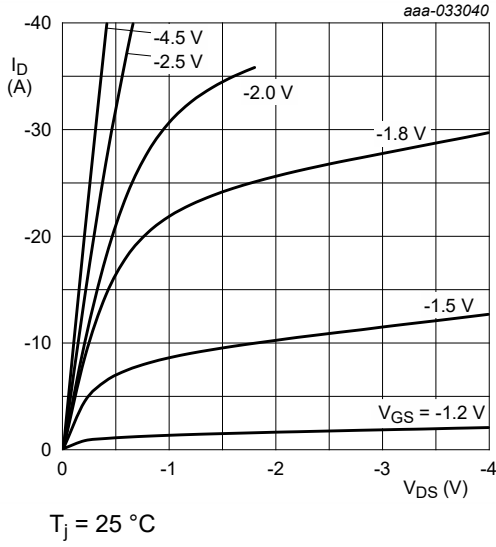


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

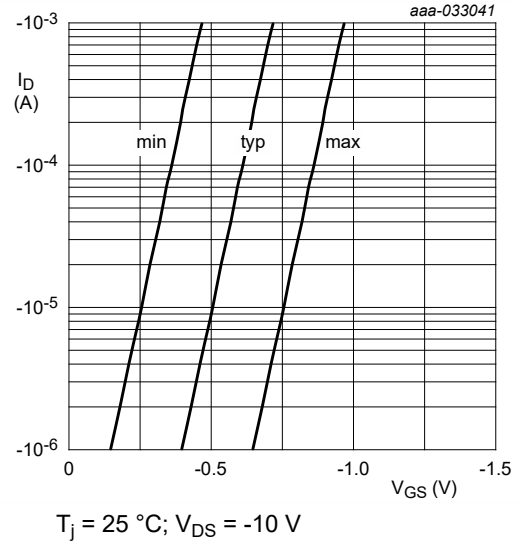


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

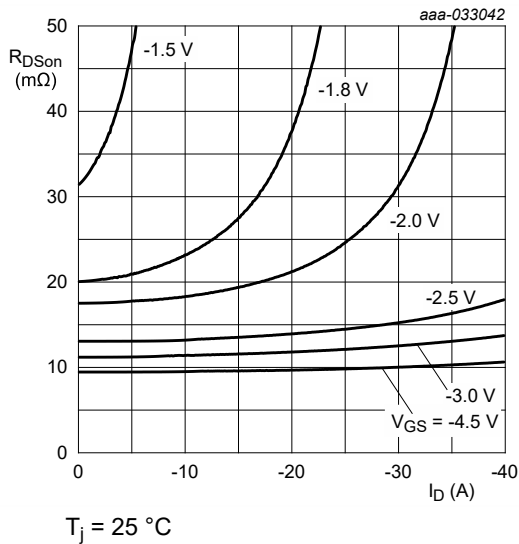


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

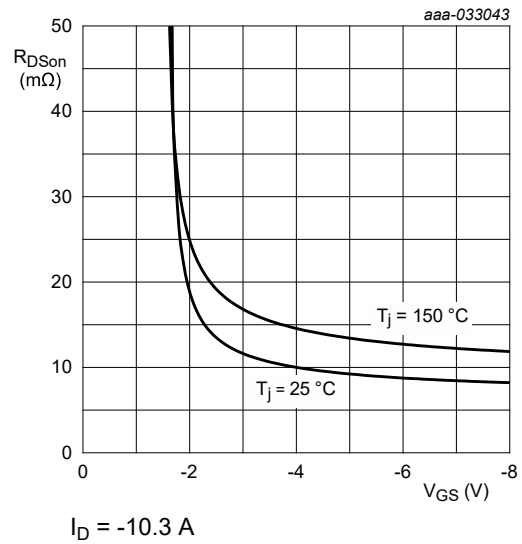


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

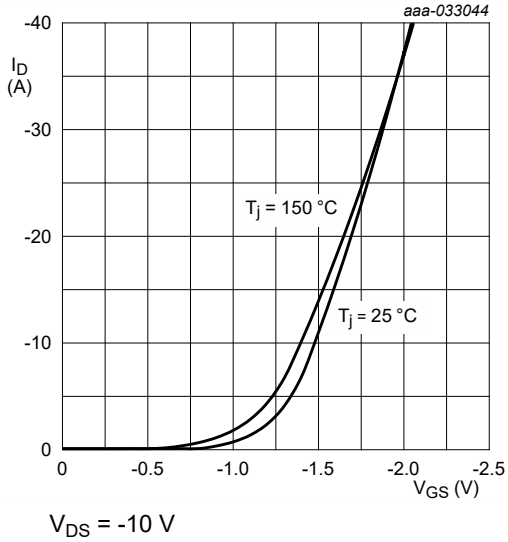


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

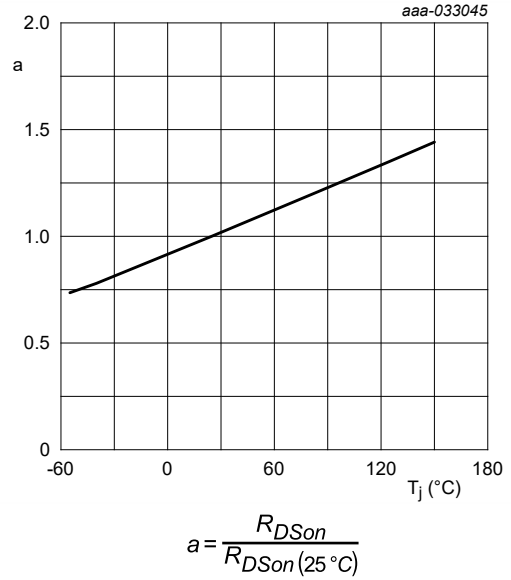


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

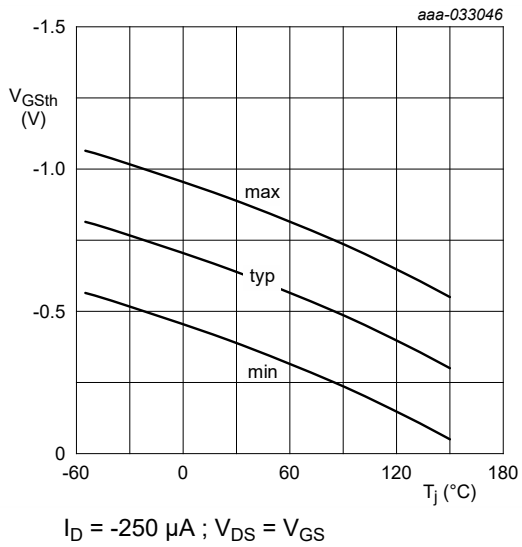


Fig. 12. Gate-source threshold voltage as a function of junction temperature

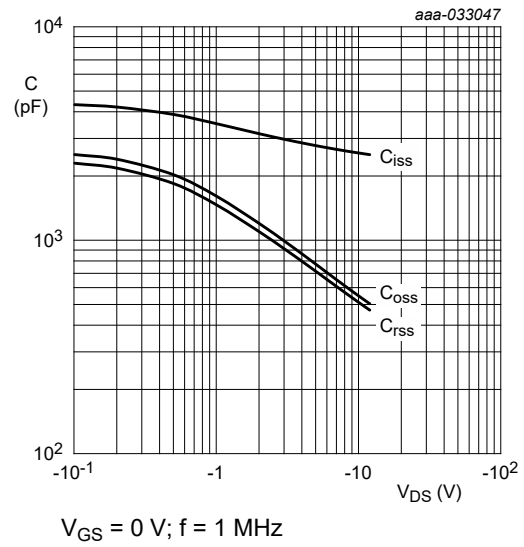


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



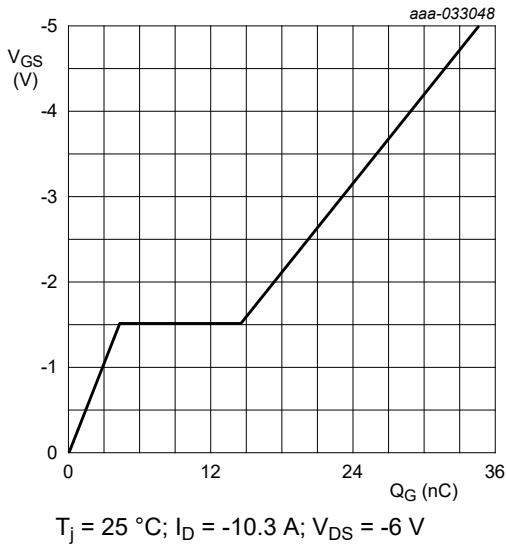


Fig. 14. Gate-source voltage as a function of gate charge; typical values

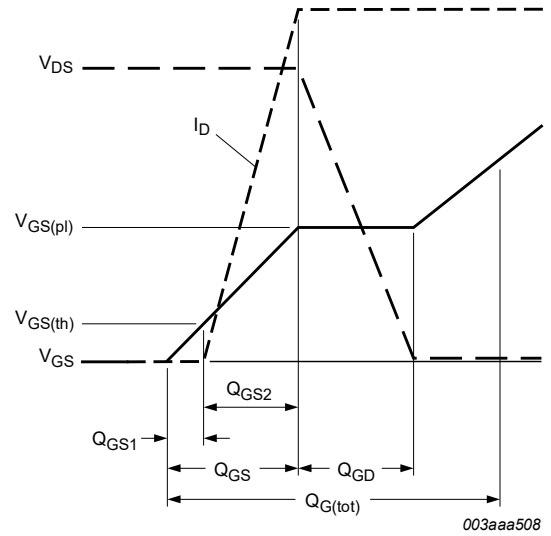


Fig. 15. Gate charge waveform definitions

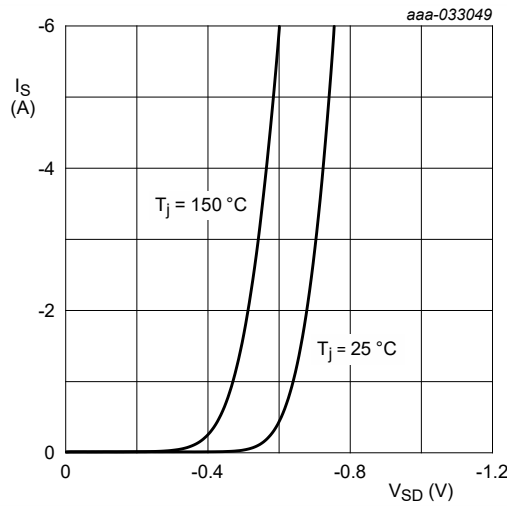


Fig. 16. Source current as a function of source-drain voltage; typical values

## 11. Test information

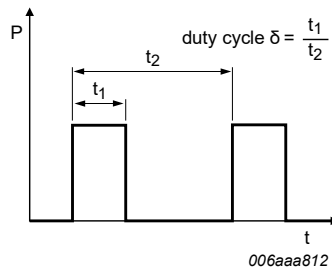
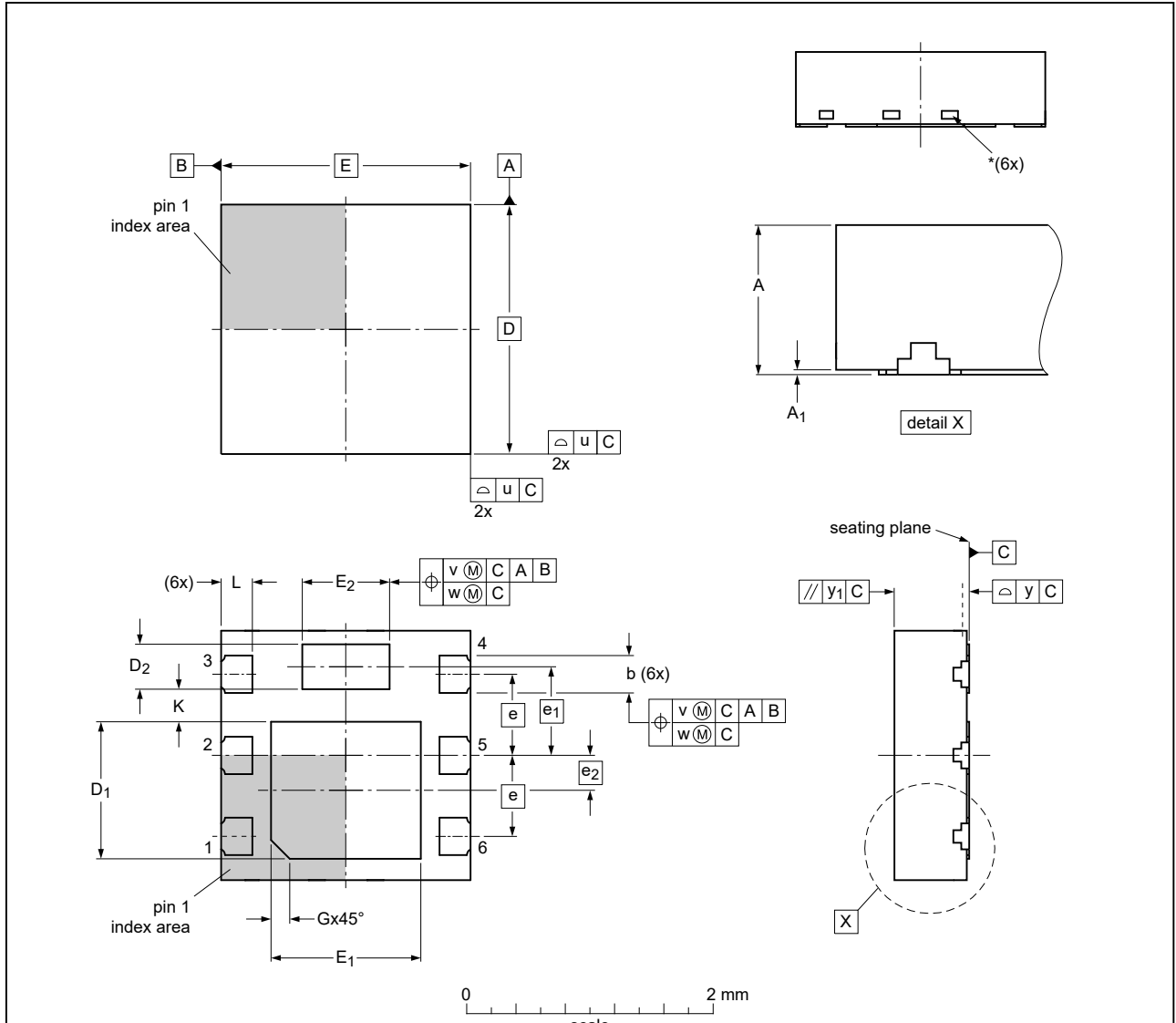


Fig. 17. Duty cycle definition

## 12. Package outline

DFN2020M-6: plastic thermal enhanced ultra thin small outline package; no leads;  
6 terminals; body 2 x 2 x 0.65 mm

SOT1220-2



Dimensions (mm are the original dimensions)

Unit	A	A <sub>1</sub>	b	D	D <sub>1</sub>	D <sub>2</sub>	E	E <sub>1</sub>	E <sub>2</sub>	e	e <sub>1</sub>	e <sub>2</sub>	G	K	L	u	v	w	y	y <sub>1</sub>
min	0.55	0	0.25	1.0	0.31	1.1	0.6							0.2	0.20					
mm	nom	0.60	0.02	0.30	2	1.1	0.36	2	1.2	0.7	0.65	0.71	0.28	0.15 (ref)	0.25	0.05	0.1	0.05	0.05	0.05
	max	0.65	0.04	0.35	1.2	0.41	1.3	0.8							0.30					

Note

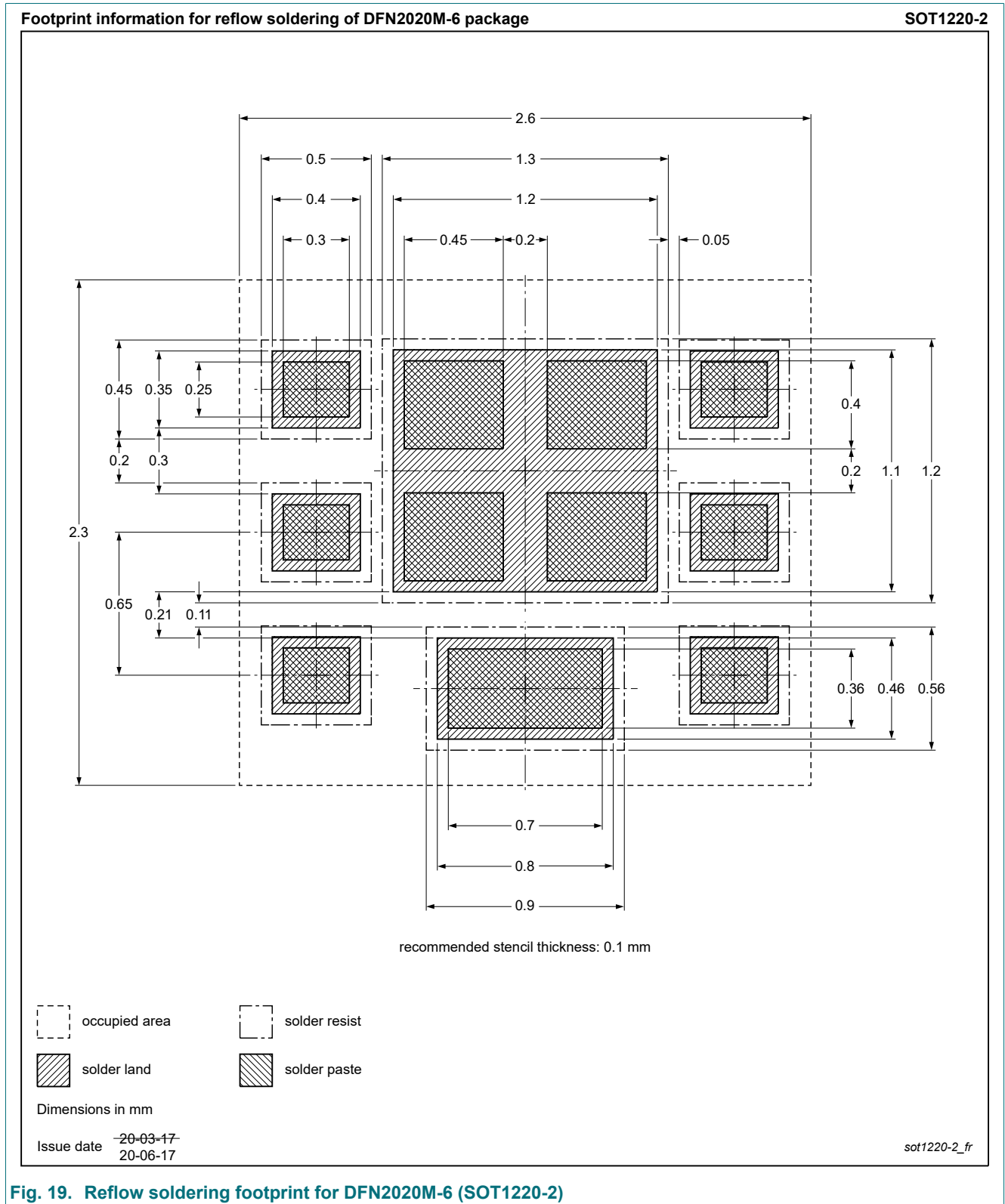
1. Dimension A is including plating thickness.
2. \* Visible depend upon used manufacturing technology.

sot1220-2\_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1220-2		---				20-03-31 20-04-01

Fig. 18. Package outline DFN2020M-6 (SOT1220-2)

### 13. Soldering



**Fig. 19. Reflow soldering footprint for DFN2020M-6 (SOT1220-2)**

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMPB09R5VP v.1	20210210	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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