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Kind regards,

Team Nexperia

DATA SHEET

74ALVCH16821

20-bit bus-interface D-type flip-flop;
positive-edge trigger (3-State)

Product specification

1998 May 29

IC24 Data Handbook

20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

74ALVCH16821

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Current drive ± 24 mA at 3.0 V
- CMOS low power consumption
- Direct interface with TTL levels
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and ground pins for minimum noise and ground bounce
- All data inputs have bus hold
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74ALVCH16821 has two 10-bit, edge triggered registers, with each register coupled to a 3-State output buffer. The two sections of each register are controlled independently by the clock (nCP) and Output Enable ($\overline{nOE}$) control gates.

Each register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

When $\overline{nOE}$ is LOW, the data in the register appears at the outputs. When $\overline{nOE}$ is HIGH, the outputs are in high impedance OFF state. Operation of the $\overline{nOE}$ input does not affect the state of the flip-flops.

The 74ALVCH16821 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

QUICK REFERENCE DATA

GND = 0V; $T_{amb} = 25^{\circ}\text{C}$; $t_r = t_f \leq 2.5\text{ns}$

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nCP to nQ _n	$V_{CC} = 2.5\text{V}$, $C_L = 30\text{pF}$ $V_{CC} = 3.3\text{V}$, $C_L = 50\text{pF}$		2.6 2.5	ns
C_I	Input capacitance			5.0	pF
C_{PD}	Power dissipation capacitance per buffer	$V_I = \text{GND to } V_{CC}^1$	Outputs enabled	33	pF
			Outputs disabled	17	
F_{max}	Maximum clock frequency	$V_{CC} = 2.5\text{V}$, $C_L = 30\text{pF}$ $V_{CC} = 3.3\text{V}$, $C_L = 50\text{pF}$		250 350	MHz

NOTE:

- C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacitance in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	-40°C to $+85^{\circ}\text{C}$	74ALVCH16821 DL	ACH16821 DL	SOT371-1
56-Pin Plastic TSSOP Type II	-40°C to $+85^{\circ}\text{C}$	74ALVCH16821 DGG	ACH16821 DGG	SOT364-1

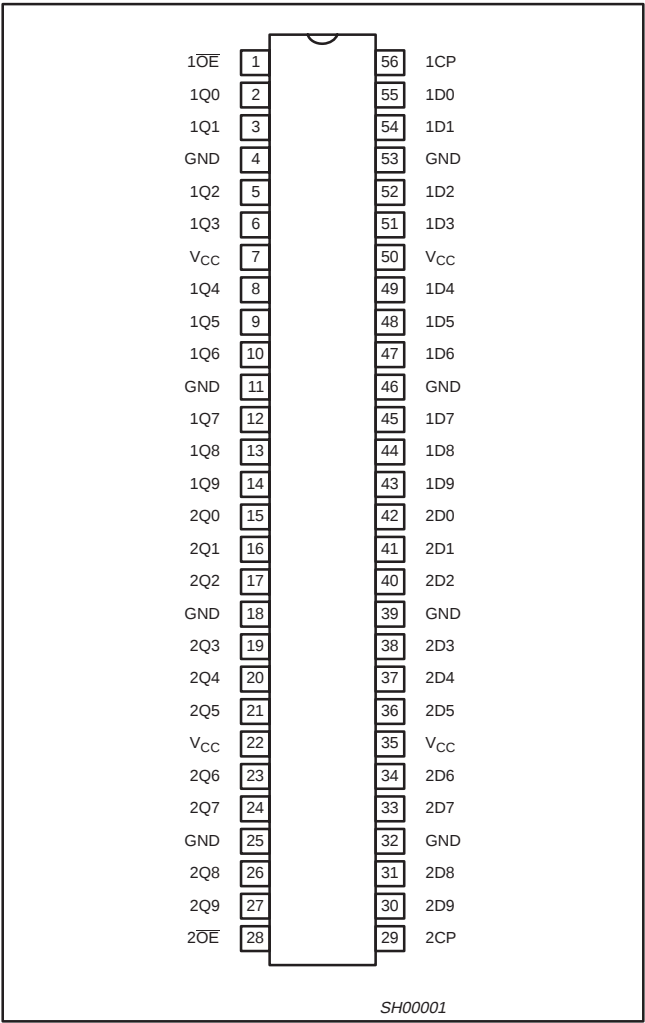
20-bit bus-interface D-type flip-flop;
positive-edge trigger (3-State)

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PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
55, 54, 52, 51, 49, 48, 47, 45, 44, 43	1D0 - 1D9	Data inputs
42, 41, 40, 38, 37, 36, 34, 33, 31, 30	2D0 - 2D9	
2, 3, 5, 6, 8, 9, 10, 12, 13, 14	1Q0 - 1Q9	Data outputs
15, 16, 17, 19, 20, 21, 23, 24, 26, 27	2Q0 - 2Q9	
1, 28	1OE, 2OE	Output enable inputs (active-Low)
56, 29	1CP, 2CP	Clock pulse inputs (active rising edge)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V _{CC}	Positive supply voltage

PIN CONFIGURATION

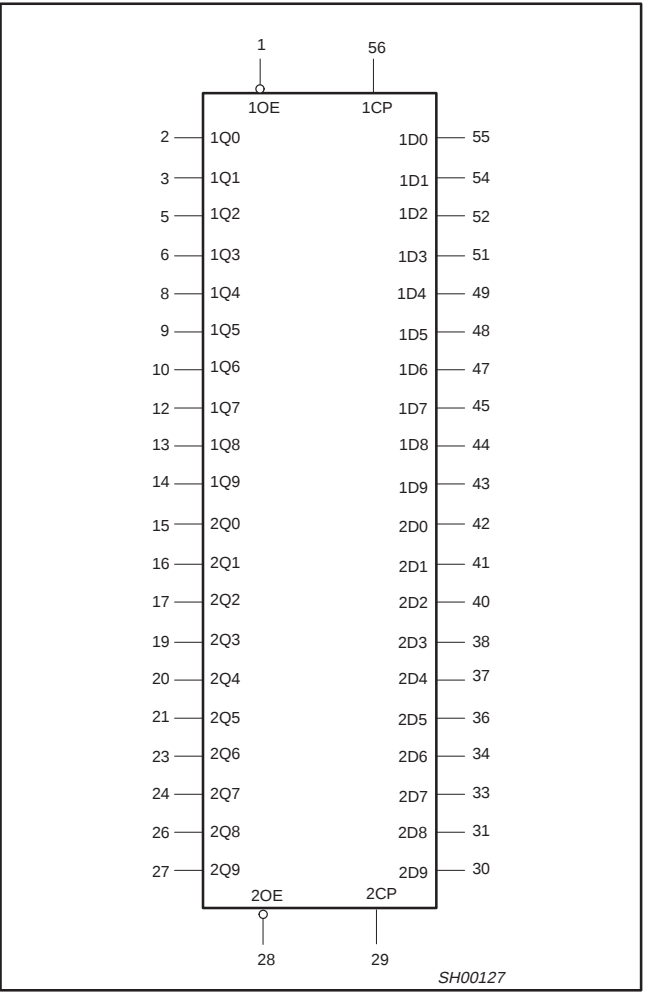


FUNCTION TABLE

INPUTS			OUTPUT
nOE	CP	Dx	Q
L	↑	L	L
L	↑	H	H
L	‡	X	Q0
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance OFF state
↑ = LOW to HIGH clock transition
‡ = Not a LOW-to-HIGH clock transition

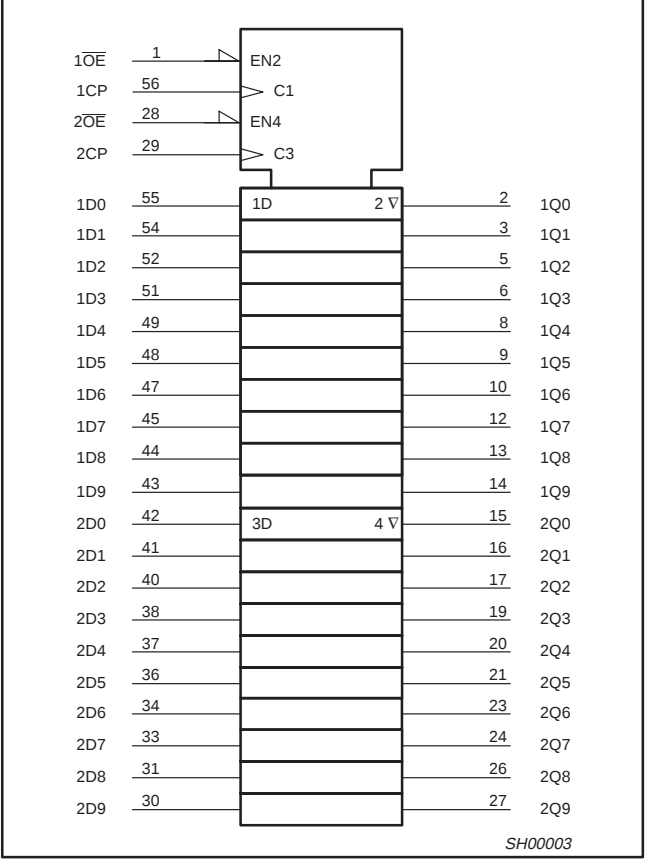
LOGIC SYMBOL



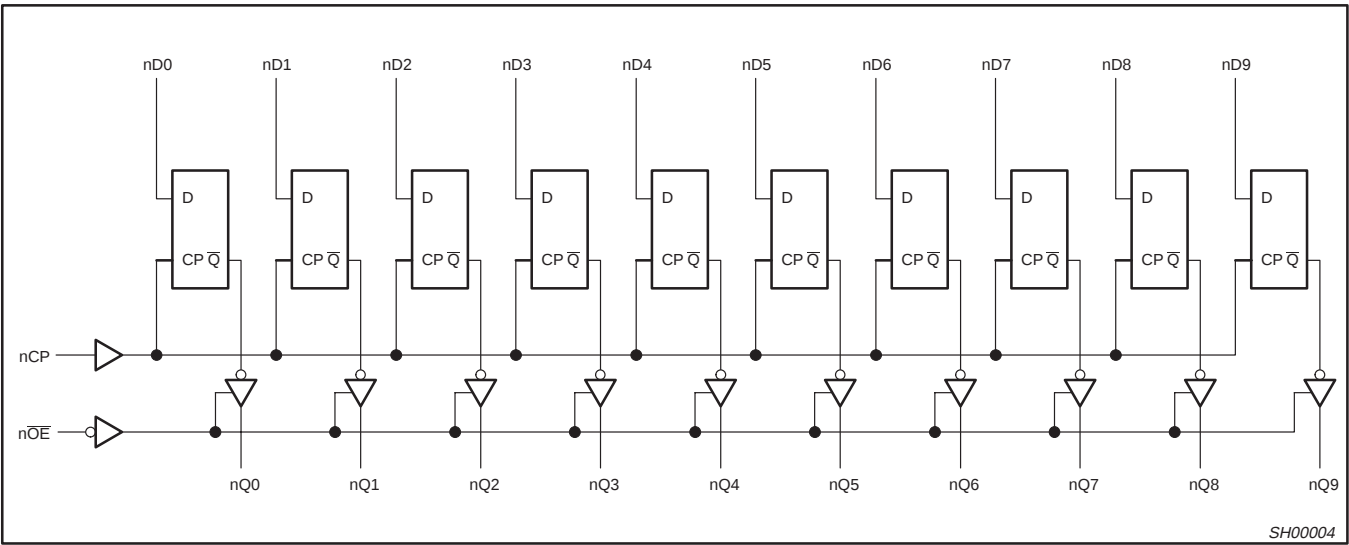
20-bit bus-interface D-type flip-flop;
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LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
V_I	DC Input voltage range		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		-40	+85	°C
t_r, t_f	Input rise and fall times	$V_{CC} = 2.3$ to 3.0V $V_{CC} = 3.0$ to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage	For control pins ¹	-0.5 to +4.6	V
		For data inputs ¹	-0.5 to $V_{CC} + 0.5$	
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	± 50	mA
V_O	DC output voltage	Note 1	-0.5 to $V_{CC} + 0.5$	V
I_O	DC output source or sink current	$V_O = 0$ to V_{CC}	± 50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		± 100	mA
T_{stg}	Storage temperature range		-65 to +150	°C
P_{TOT}	Power dissipation per package -plastic medium-shrink (SSOP) -plastic thin-medium-shrink (TSSOP)	For temperature range: -40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	850 600	mW

NOTE:

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V _{IH}	HIGH level Input voltage	V _{CC} = 2.3 to 2.7V	1.7	1.2		V
		V _{CC} = 2.7 to 3.6V	2.0	1.5		
V _{IL}	LOW level Input voltage	V _{CC} = 2.3 to 2.7V		1.2	0.7	V
		V _{CC} = 2.7 to 3.6V		1.5	0.8	
V _{OH}	HIGH level output voltage	V _{CC} = 2.3 to 3.6V; V _I = V _{IH} or V _{IL} ; I _O = -100μA	V _{CC} - 0.2	V _{CC}		V
		V _{CC} = 2.3V; V _I = V _{IH} or V _{IL} ; I _O = -6mA	V _{CC} - 0.3	V _{CC} - 0.08		
		V _{CC} = 2.3V; V _I = V _{IH} or V _{IL} ; I _O = -12mA	V _{CC} - 0.6	V _{CC} - 0.26		
		V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = -12mA	V _{CC} - 0.5	V _{CC} - 0.14		
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -12mA	V _{CC} - 0.6	V _{CC} - 0.09		
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -24mA	V _{CC} - 1.0	V _{CC} - 0.28		
V _{OL}	LOW level output voltage	V _{CC} = 2.3 to 3.6V; V _I = V _{IH} or V _{IL} ; I _O = 100μA		GND	0.20	V
		V _{CC} = 2.3V; V _I = V _{IH} or V _{IL} ; I _O = 6mA		0.07	0.40	V
		V _{CC} = 2.3V; V _I = V _{IH} or V _{IL} ; I _O = 12mA		0.15	0.70	V
		V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 12mA		0.14	0.40	
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 24mA		0.27	0.55	
I _I	Input leakage current	V _{CC} = 2.3 to 3.6V; V _I = V _{CC} or GND		0.1	5	μA
I _{OZ}	3-State output OFF-state current	V _{CC} = 2.7 to 3.6V; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND		0.1	10	μA
I _{CC}	Quiescent supply current	V _{CC} = 2.3 to 3.6V; V _I = V _{CC} or GND; I _O = 0		0.2	40	μA
ΔI _{CC}	Additional quiescent supply current	V _{CC} = 2.3V to 3.6V; V _I = V _{CC} - 0.6V; I _O = 0		150	750	μA
I _{BHL}	Bus hold LOW sustaining current	V _{CC} = 2.3V; V _I = 0.7V ²	45	—		μA
		V _{CC} = 3.0V; V _I = 0.8V ²	75	150		
I _{BHH}	Bus hold HIGH sustaining current	V _{CC} = 2.3V; V _I = 1.7V ²	-45			μA
		V _{CC} = 3.0V; V _I = 2.0V ²	-75	-175		
I _{BHLO}	Bus hold LOW overdrive current	V _{CC} = 3.6V ²	500			μA
I _{BHHO}	Bus hold HIGH overdrive current	V _{CC} = 3.6V ²	-500			μA

NOTES:

1. All typical values are at $T_{amb} = 25^\circ C$.
2. Valid for data inputs of bus hold parts.

20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

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AC CHARACTERISTICS FOR $V_{CC} = 2.3V$ TO $2.7V$ RANGE

GND = 0V; $t_r = t_f \leq 2.0ns$; $C_L = 30pF$

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V _{CC} = 2.5V ± 0.2V			
			MIN	TYP ¹	MAX	
t _{PLH} /t _{PHL}	Propagation delay nCP to nQ _n	1, 4	1.0	2.6	5.8	ns
t _{PZH} /t _{PZL}	3-State output enable time nOE _n to nQ _n	2, 4	1.0	2.8	6.6	ns
t _{PHZ} /t _{PLZ}	3-State output disable time nOE _n to nQ _n	2, 4	1.0	2.2	5.7	ns
t _W	nCP pulse width HIGH or LOW	3, 4	3.0	1.8		ns
t _{SU}	Set up time nD _n to nCP	3, 4	1.4	0.3		ns
t _h	Hold time nD _n to nCP	3, 4	0.4	0.0		ns
F _{max}	Maximum clock pulse frequency	1, 4	150	250		MHz

NOTE:

1. All typical values are at $V_{CC} = 2.5V$ and $T_{amb} = 25^\circ C$.

AC CHARACTERISTICS FOR $V_{CC} = 3.0V$ TO $3.6V$ RANGE AND $V_{CC} = 2.7V$

GND = 0V; $t_r = t_f \leq 2.5ns$; $C_L = 50pF$

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V _{CC} = 3.3 ± 0.3V			V _{CC} = 2.7V			
			MIN	TYP ¹	MAX	MIN	TYP ¹	MAX	
t _{PHL} /t _{PLH}	Propagation delay nCP to nQ _n	1, 4	1.0	2.5	4.5	1.0	2.8	5.3	ns
t _{PZH} /t _{PZL}	3-State output enable time nOE _n to nQ _n	2, 4	1.0	2.3	5.1	1.0	3.2	6.2	ns
t _{PHZ} /t _{PLZ}	3-State output disable time nOE _n to nQ _n	2, 4	1.0	2.8	4.6	1.0	3.1	5.0	ns
t _W	nCP pulse width HIGH or LOW	3, 4	3.3	0.2		3.3	1.7		ns
t _{SU}	Set up time nD _n to nCP	3, 4	1.0	0.2		1.2	0.3		ns
t _h	Hold time nD _n to nCP	3, 4	0.8	0.4		0.6	−0.3		ns
F _{max}	Maximum clock pulse frequency	1, 4	150	350		150	300		MHz

NOTES:

1. All typical values are at $T_{amb} = 25^\circ C$.

20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

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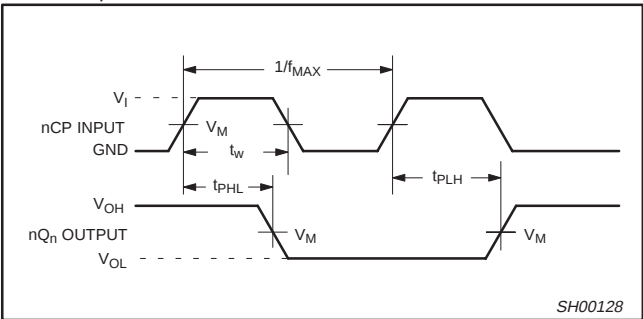
AC WAVEFORMS

$V_{CC} = 2.3 \text{ TO } 2.7 \text{ V RANGE}$

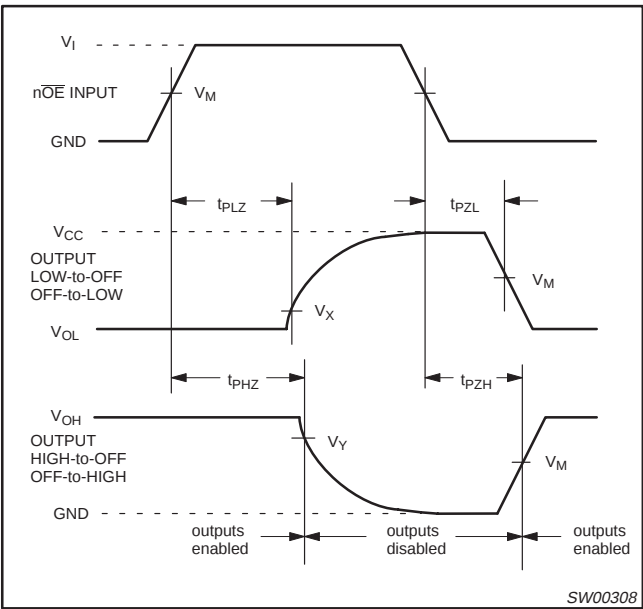
1. $V_M = 0.5 \text{ V}$
2. $V_X = V_{OL} + 0.15 \text{ V}$
3. $V_Y = V_{OH} - 0.15 \text{ V}$
4. $V_I = V_{CC}$
5. V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

$V_{CC} = 3.0 \text{ TO } 3.6 \text{ V RANGE AND } V_{CC} = 2.7 \text{ V}$

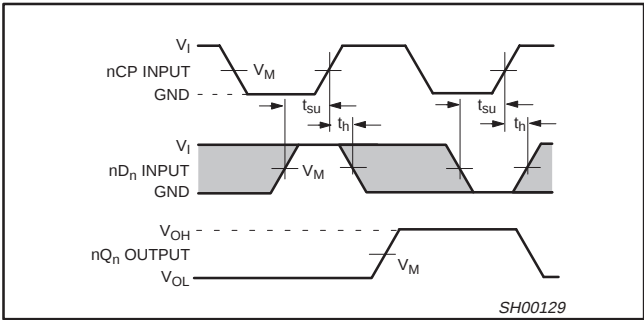
1. $V_M = 1.5 \text{ V}$
2. $V_X = V_{OL} + 0.3 \text{ V}$
3. $V_Y = V_{OH} - 0.3 \text{ V}$
4. $V_I = 2.7 \text{ V}$
5. V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



Waveform 1. The input (nCP) to output propagation delays.

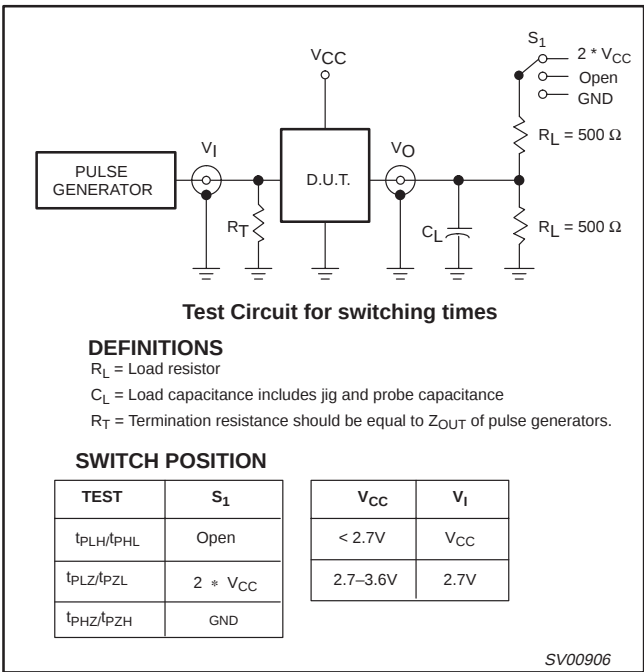


Waveform 2. The 3-State enable and disable times.



Waveform 3. Set up and hold times.

TEST CIRCUIT



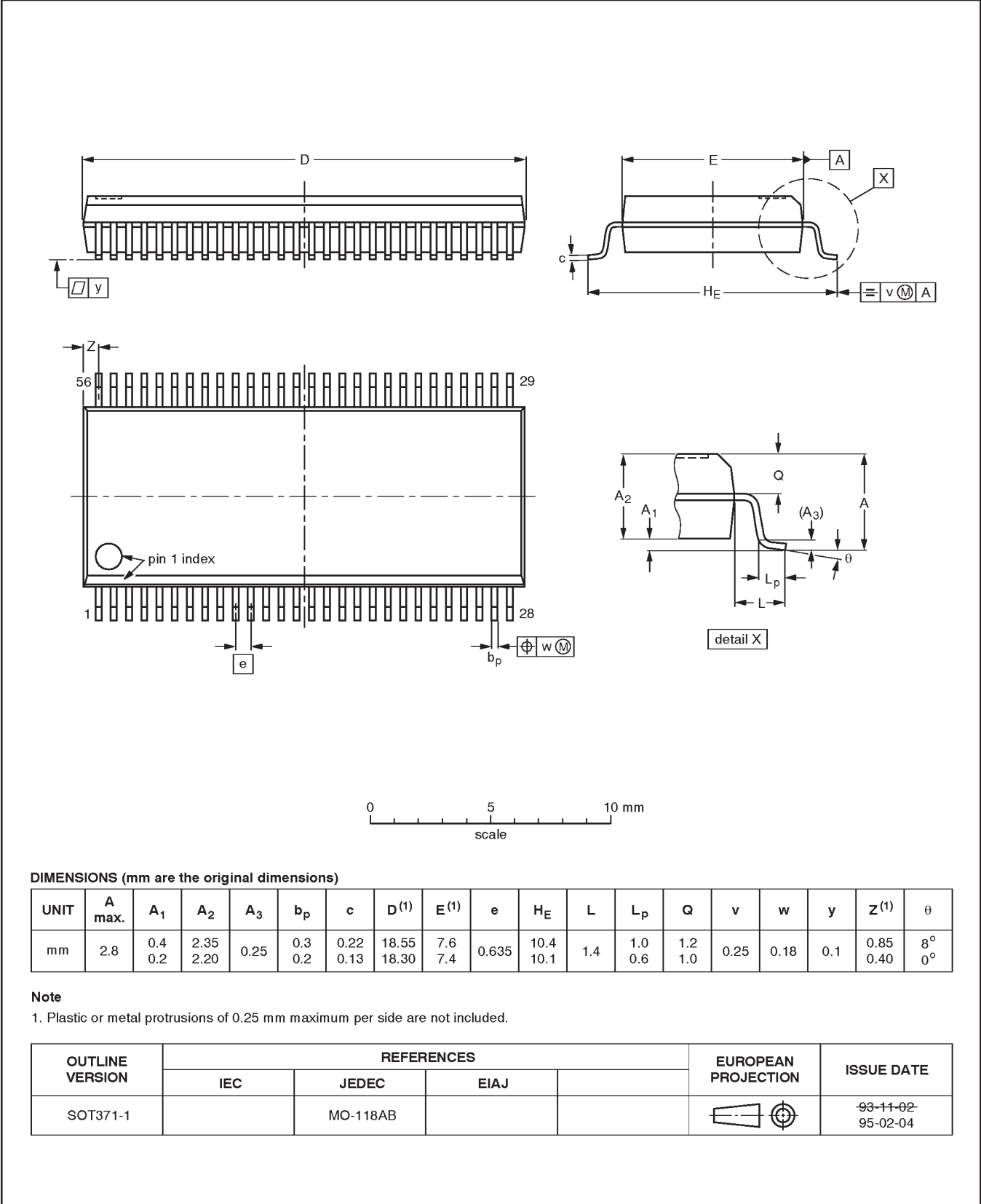
Waveform 4. Load circuitry for switching times

20-bit bus-interface D-type flip-flop;
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SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1

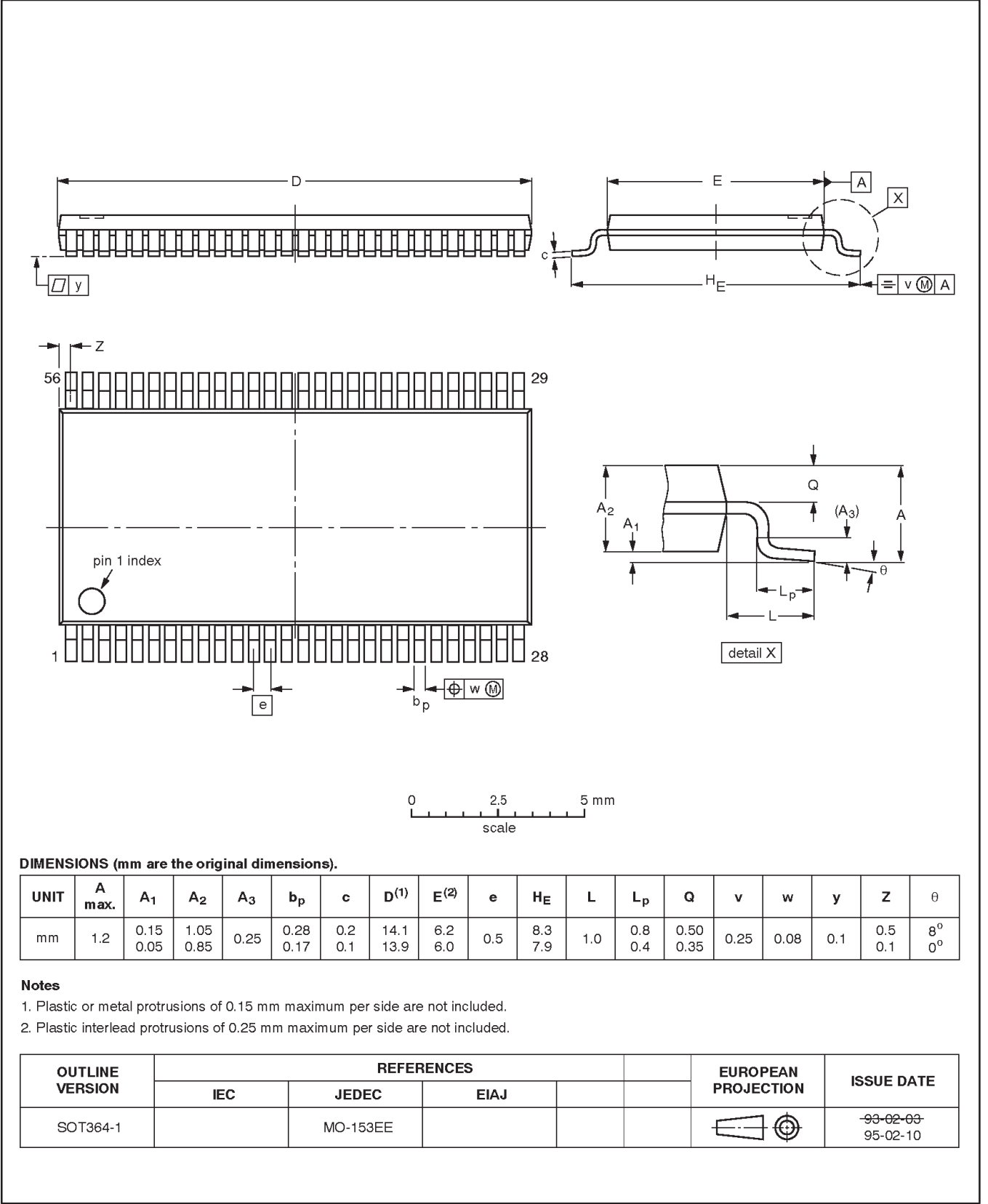


20-bit bus-interface D-type flip-flop;
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74ALVCH16821

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



20-bit bus-interface D-type flip-flop;
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74ALVCH16821

NOTES

20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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print code

Date of release: 05-96

Document order number:

9397-750-04553

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