74HCU04

Hex unbuffered inverter

Rev. 8 — 16 July 2020

Product data sheet

1. General description

The 74HCU04 is a hex unbuffered inverter. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- · CMOS low power dissipation
- · High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- · Balanced propagation delays
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +125 °C

3. Ordering information

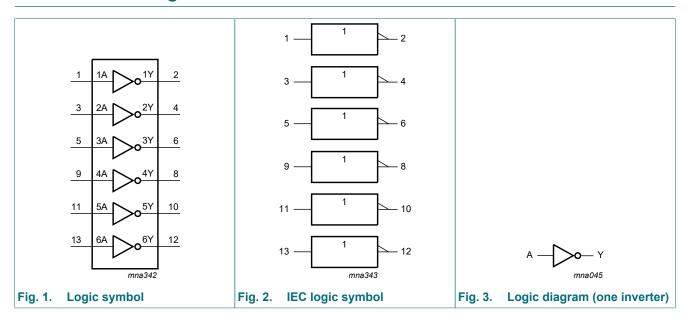
Table 1. Ordering information

Type number	Package						
	Temperature range	Name	Description	Version			
74HCU04D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1			
74HCU04DB	-40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1			
74HCU04PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1			
74HCU04BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1			



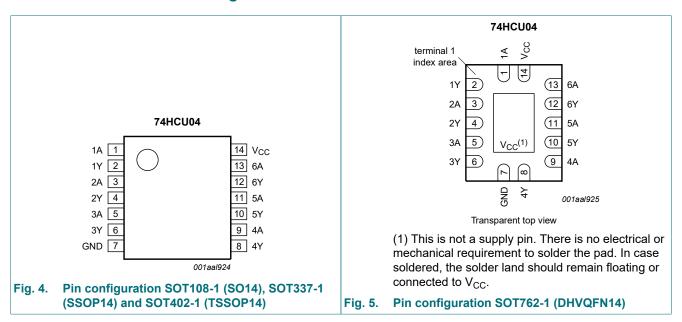
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4. Functional diagram



5. Pinning information

5.1. Pinning



Hex unbuffered inverter

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level

Input	Output
nA	nY
L	Н
Н	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
I _{IK}	input clamping current	$V_1 < -0.5 \text{ V or } V_1 > V_{CC} + 0.5 \text{ V}$ [1]	-	±20	mA
I _{OK}	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$ [1]	-	±50	mA
Io	output current	$-0.5 \text{ V} < \text{V}_{\text{O}} < \text{V}_{\text{CC}} + 0.5 \text{ V}$	-	±25	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	[2]	-	500	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

For SOT337-1 (SSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

For SOT762-1 (DHVQFN14) package: Ptot derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{CC}	supply voltage		2.0	5.0	6.0	V
VI	input voltage		0	-	V _{CC}	V
Vo	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C

^[2] For SOT108-1 (SO14) package: Ptot derates linearly with 10.1 mW/K above 100 °C.

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9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C to	o +85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level	V _{CC} = 2.0 V	1.7	1.4	-	1.7	-	1.7	-	V
	input voltage	V _{CC} = 4.5 V	3.6	2.6	-	3.6	-	3.6	-	V
		V _{CC} = 5.5 V	4.8	3.4	-	4.8	-	4.8	-	V
V _{IL}	LOW-level	V _{CC} = 2.0 V	-	0.6	0.3	-	0.3	-	0.3	V
	input voltage	V _{CC} = 4.5 V	-	1.9	0.9	-	0.9	-	0.9	V
		V _{CC} = 5.5 V	-	2.6	1.2	-	1.2	-	1.2	V
V _{OH}	HIGH-level	V _I = V _{IH} or V _{IL}								
	output voltage	I _O = -20 μA; V _{CC} = 2.0 V	1.8	2.0	-	1.8	-	1.8	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.0	4.5	-	4.0	-	4.0	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.5	6.0	-	5.5	-	5.5	-	V
		I_{O} = -5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.2	-	0.2	-	0.2	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.5	-	0.5	-	0.5	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.5	-	0.5	-	0.5	V
		I_{O} = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
l _l	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1.0	-	±1.0	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	2	-	20	-	20	μΑ
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

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10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); For test circuit see Fig. 7.

Symbol	Parameter	Conditions		25 °C		-40 °C to +85 °C	-40 °C to +125 °C	Unit
				Тур	Max	Max	Max	
t _{pd}	propagation delay	nA to nY; see Fig. 6	[1]					
		$V_{CC} = 2.0 \text{ V}; C_L = 50 \text{ pF}$		19	70	90	105	ns
		V _{CC} = 4.5 V; C _L = 50 pF		7	14	18	21	ns
		V _{CC} = 5.0 V; C _L = 15 pF		5	-	-	-	ns
		V _{CC} = 6.0 V; C _L = 50 pF		6	12	15	18	ns
t _t	transition time	see Fig. 6	[2]					
		$V_{CC} = 2.0 \text{ V}; C_L = 50 \text{ pF}$		19	75	95	110	ns
		V _{CC} = 4.5 V; C _L = 50 pF		7	15	19	22	ns
		$V_{CC} = 6.0 \text{ V}; C_L = 50 \text{ pF}$		6	13	16	19	ns
C _{PD}	power dissipation capacitance	per inverter; V _I = GND to V _{CC}	[3]	10	-	-	-	pF

- t_{pd} is the same as t_{PHL} , t_{PLH} .
- t_t is the same as t_{THL} , t_{TLH} .
- C_{PD} is used to determine the dynamic power dissipation (P_D in μ W). $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

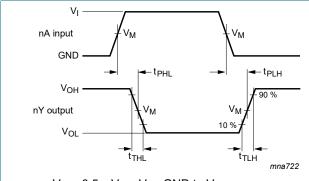
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

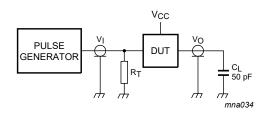
 $\Sigma(C_L \times V_{CC})^2 \times f_0$ = sum of outputs.

10.1. Waveform and test circuit



 $V_M = 0.5 \times V_{CC}$; $V_I = GND$ to V_{CC} .

Fig. 6. The input (nA) to output (nY) propagation delay times



Definitions for test circuit:

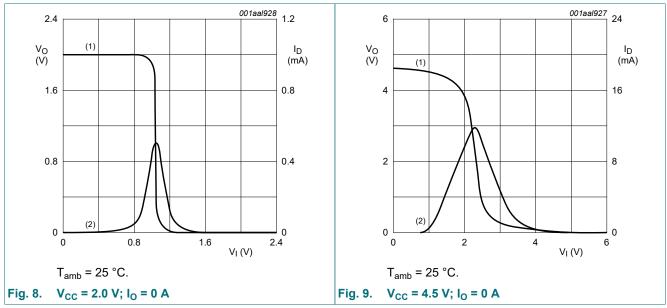
C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_{o} of the pulse generator.

Test circuit for measuring switching times Fig. 7.

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11. Typical transfer characteristics



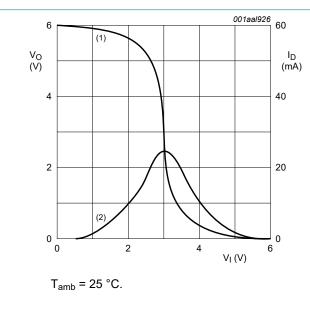


Fig. 10. $V_{CC} = 6.0 \text{ V}$; $I_O = 0 \text{ A}$

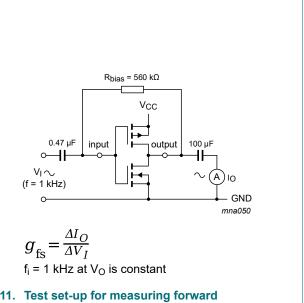
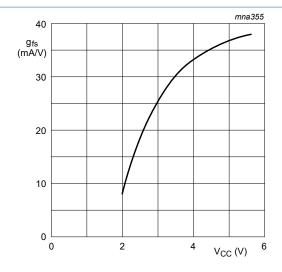


Fig. 11. Test set-up for measuring forward transconductance

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 $T_{amb} = 25 \, ^{\circ}C.$

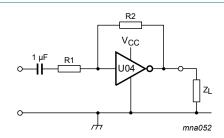
Fig. 12. Typical forward transconductance as a function of the supply voltage

12. Application information

Some applications are:

- · Linear amplifier (see Fig. 13)
- · Crystal oscillator design (see Fig. 14)
- Astable multivibrator (see <u>Fig. 15</u>)

Remark: All values given are typical unless otherwise specified.



Maximum $V_{o(p-p)} = V_{CC}$ - 2.0 V centered at 0.5V_{CC}.

$$G_v = -\frac{G_{\text{ol}}}{1 + \frac{R1}{R2}(1 + G_{\text{ol}})}$$

G_{ol} = open loop gain

G_v = voltage gain

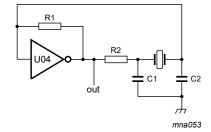
 $R1 \ge 3 \text{ k}\Omega, R2 \le 1 \text{ M}\Omega$

 $Z_L > 10 \text{ k}\Omega$; $G_{ol} = 20 \text{ (typical)}$

 $V_{CC} = 6.0 \text{ V}$

Typical unity gain bandwidth product is 5 MHz.

Fig. 13. Linear amplifier



C1 = 47 pF (typical)

C2 = 33 pF (typical)

R1 = 1 M Ω to 10 M Ω (typical

R2 optimum value depends on the frequency and required stability against changes in V_{CC} or average minimum I_{CC} .

 I_{CC} is typically 5 mA at V_{CC} = 5 V and f_i = 10 MHz.

Fig. 14. Crystal oscillator

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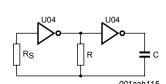
Table 8. External components for resonator (f < 1 MHz)

All values given are typical and must be used as an initial set-up.

Frequency	R1	R2	C1	C2
10 kHz to 15.9 kHz	22 ΜΩ	220 kΩ	56 pF	20 pF
16 kHz to 24.9 kHz	22 ΜΩ	220 kΩ	56 pF	10 pF
25 kHz to 54.9 kHz	22 ΜΩ	100 kΩ	56 pF	10 pF
55 kHz to 129.9 kHz	22 ΜΩ	100 kΩ	47 pF	5 pF
130 kHz to 199.9 kHz	22 ΜΩ	47 kΩ	47 pF	5 pF
200 kHz to 349.9 kHz	10 ΜΩ	47 kΩ	47 pF	5 pF
350 kHz to 600 kHz	10 ΜΩ	47 kΩ	47 pF	5 pF

Table 9. Optimum value for R2

Frequency	R2	Optimum for	
3 kHz	2.0 kΩ	minimum required I _{CC}	
	8.0 kΩ	minimum influence due to change in V _{CC}	
6 kHz	1.0 kΩ	minimum required I _{CC}	
	4.7 kΩ	minimum influence by V _{CC}	
10 kHz	0.5 kΩ	minimum required I _{CC}	
	2.0 kΩ	minimum influence by V _{CC}	
14 kHz	0.5 kΩ	minimum required I _{CC}	
	1.0 kΩ	minimum influence by V _{CC}	
>14 kHz	-	replace R2 by C3 with a typical value of 35 pF	

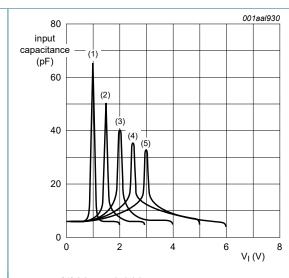


$$f = \frac{1}{T} \approx \frac{1}{2.2 \text{RC}}$$

$$R_S \approx 2 \times R$$

The average I_{CC} (mA) is approximately 3.5 + 0.05 × f (MHz) × C (pF) at V_{CC} = 5.0 V.





- (1) $V_{CC} = 2.0 \text{ V}$
- (2) $V_{CC} = 3.0 \text{ V}$
- $(3) V_{CC} = 4.0 V$
- $(4) V_{CC} = 5.0 V$
- $(5) V_{CC} = 6.0 V$
- T_{amb} = 25 °C.

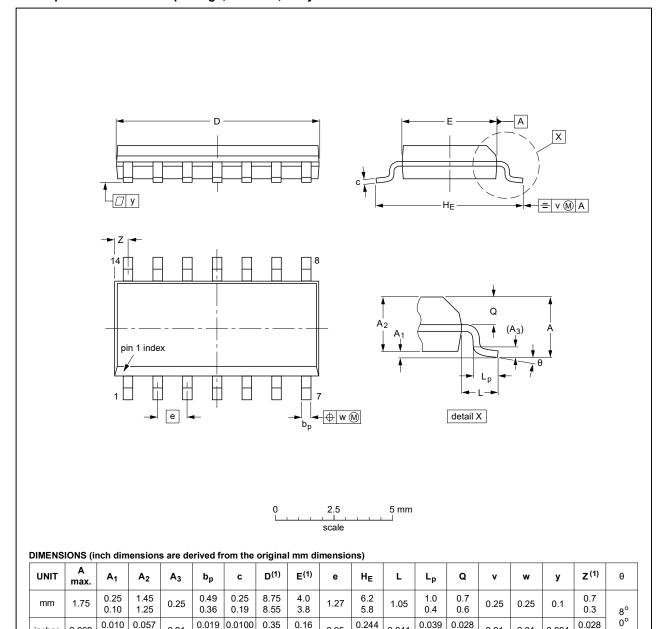
Fig. 16. Input capacitance as function of input voltage

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13. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



Note

0.069

0.004

0.049

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

0.014 0.0075

0.01

OUTLINE	REFERENCES				EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT108-1	076E06	MS-012				99-12-27 03-02-19	

0.05

0.228

0.15

0.041

0.016

0.024

0.01

0.01

0.004

0.012

Fig. 17. Package outline SOT108-1 (SO14)

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SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

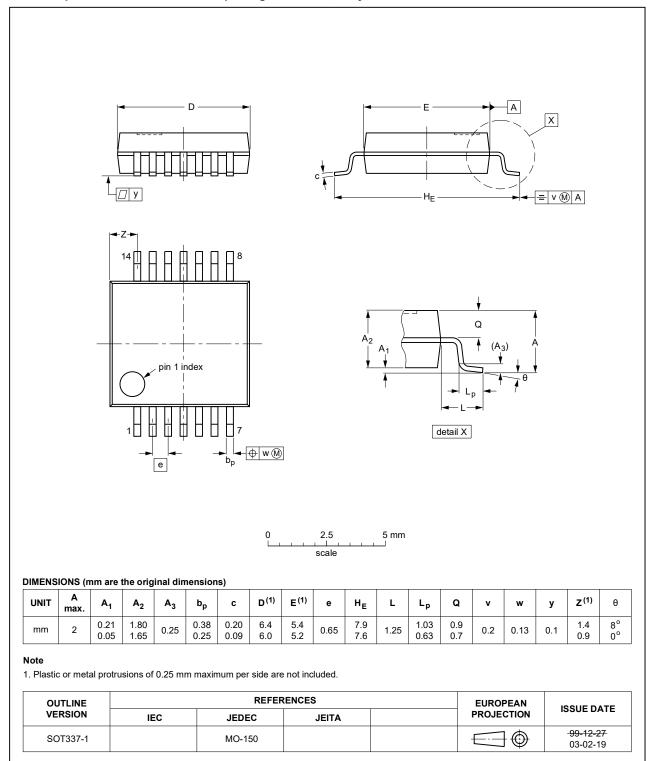


Fig. 18. Package outline SOT337-1 (SSOP14)

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

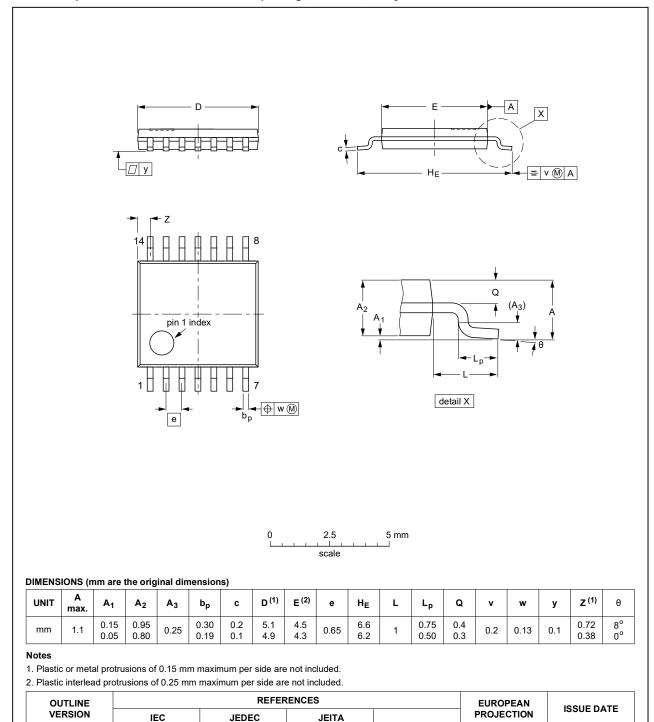


Fig. 19. Package outline SOT402-1 (TSSOP14)

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SOT402-1

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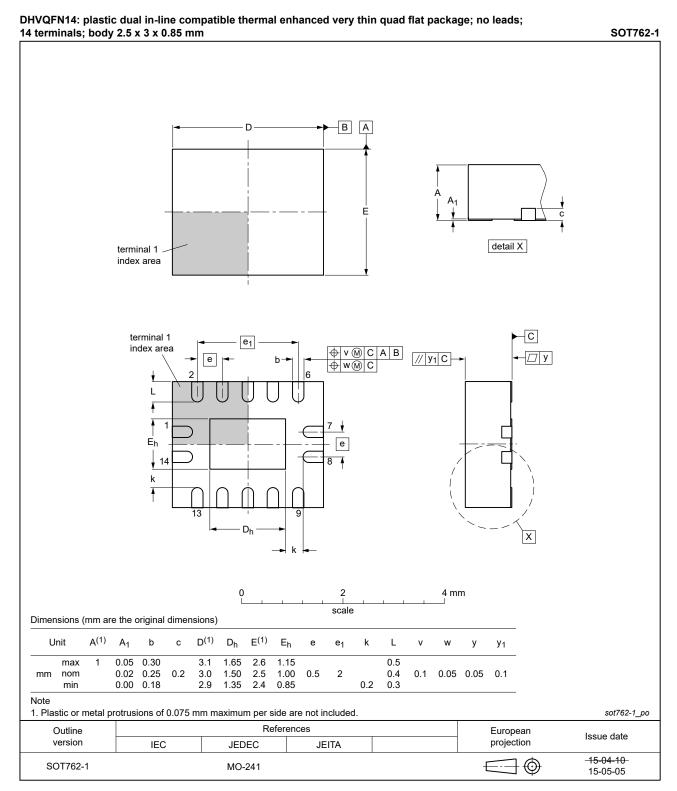


Fig. 20. Package outline SOT762-1 (DHVQFN14)

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14. Abbreviations

Table 10. Abbreviations

Acronym	escription			
CMOS	mplementary Metal Oxide Semiconductor			
ESD	ctroStatic Discharge			
HBM	Human Body Model			
MM Machine Model				

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes				
74HCU04 v.8	20200716	Product data sheet	-	74HCU04 v.7				
Modifications:	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 2 updated. Section 7: Derating values for P_{tot} total power dissipation have been updated. 							
74HCU04 v.7	20151208	Product data sheet	-	74HCU04 v.6				
Modifications:	1	U04N (SOT27-1) removed V _{IH} corrected (errata).						
74HCU04 v.6	20121227	Product data sheet	-	74HCU04 v.5				
Modifications:	 New general descrip 	otion.						
74HCU04 v.5	20120806	Product data sheet	-	74HCU04 v.4				
Modifications:	Measurement points	s added to figure 6 (errata)						
74HCU04 v.4	20111212	Product data sheet	-	74HCU04 v.3				
Modifications:	Legal pages updated.							
74HCU04 v.3	20100916	Product data sheet	-	74HCU04_CNV v.2				
74HCU04_CNV v.2	19970826	Product specification	-	-				

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16. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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