

# NCA9306

## 2-bit bidirectional multi-voltage level translator; open-drain; push-pull

Rev. 2 — 26 November 2021

Product data sheet

### 1. General description

The NCA9306 is a 2 channel bidirectional I<sup>2</sup>C and SMBus multi-voltage level translator with an enable (EN) pin input. It allows voltage translation between 0.95 V and 5 V without the use of a direction pin. It supports up to 100 MHz up translation and >100 MHz down translation at ≤ 30 pF capacitive load. There is no need for a direction pin which minimizes the system effort. The NCA9306 supports 5 V tolerant I/O pins to support mixed mode signal operation. The ability to set up different voltage translation levels on each channel makes the device very flexible and suitable for a lot of different applications.

The low ON-state resistance  $R_{ON}$  of the switch allows connections to be made with minimal propagation delay. When EN is HIGH, the translator switch is on, and the SCLA and SDAA I/O are connected to the SCLB and SDAB I/O respectively, allowing bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high-impedance state exists between ports. As with the standard I<sup>2</sup>C bus-system, pull-up resistors are required to provide the logic HIGH levels on the translators bus. The NCA9306 has a standard open-drain configuration of the I<sup>2</sup>C-bus. The size of these pull-up resistors depend on the system. Each side of the translator must have a pull-up resistors. NCA9306 is designed to work with Standard-mode, Fast-mode and Fast-mode plus I<sup>2</sup>C bus devices in addition to the SMBus devices.

When the SDAA or SDAB pin is LOW, the clamp is in the ON-state and a low resistance connections exists between the SDAA and SDAB ports. Assuming the higher voltage is on the SDAB port when the SDAB port is HIGH, the voltage on the SDAA port is limited to the voltage set by refA. When the SDAA port is HIGH, the SDAB port is pulled to the refB supply voltage by the pull-up resistors. The SCLA or SCLB pins also follows the same behavior as described for SDAA or SDAB pins.

### 2. Features and benefits

- 2-channel bidirectional voltage translator for SDA and SCL lines in mixed mode I<sup>2</sup>C bus applications
- Open-drain I<sup>2</sup>C-bus I/O ports (SCLA, SDAA, SCLB and SDAB)
- Provides bidirectional voltage translation with no direction pin
- High-impedance SCLA, SDAA, SCLB and SDAB for EN = LOW
- Up translation
  - < 100 MHz;  $C_L = 30$  pF
  - < 40 MHz;  $C_L = 50$  pF
- Down translation
  - > 100 MHz;  $C_L = 30$  pF
  - < 40 MHz;  $C_L = 50$  pF
- Hot insertion
- Bidirectional voltage level translation between:
  - 0.95 V and 1.8 V, 2.5 V, 3.3 V and 5.0 V
  - 1.2 V and 1.8 V, 2.5 V, 3.3 V and 5.0 V
  - 1.8 V and 2.5 V, 3.3 V and 5.0 V
  - 2.5 V and 3.3 V and 5.0 V
  - 3.3 V and 5.0 V
- Low standby current
- 5 V tolerant I<sup>2</sup>C-bus I/O pins to support mixed mode signal operation

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- Low  $R_{ON}$  provides less signal distortion
- Latch-up performance exceeds 100 mA per JESD78 class II level A
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2000 V
  - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 1000 V
- Specified from -40 °C to +125 °C

### 3. Applications

- GPIO, MDIO, PMBus, SMBus, SDIO, UART, I<sup>2</sup>C, and other interfaces in Telecom infrastructure
- Industrial
- Personal computing
- Router and Industrial Automation

### 4. Ordering information

**Table 1. Ordering information**

Type number	Package			Version
	Temperature range	Name	Description	
NCA9306DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
NCA9306DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
NCA9306GX	-40 °C to +125 °C	X2SON8	plastic thermal enhanced extremely thin small outline package; no leads; 8 terminals; body 1.35 × 0.8 × 0.32 mm	SOT1233-2

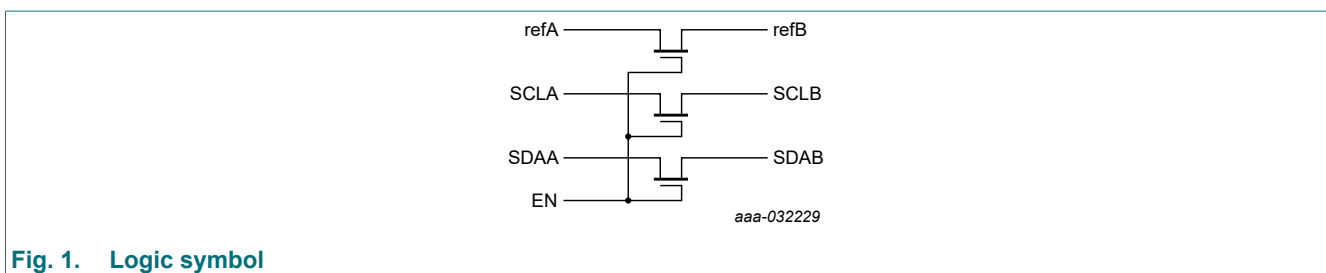
### 5. Marking

**Table 2. Marking**

Type number	Marking code <sup>[1]</sup>
NCA9306DP	h9
NCA9306DC	h9
NCA9306GX	h9

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

### 6. Functional diagram



## 7. Pinning information

### 7.1. Pinning

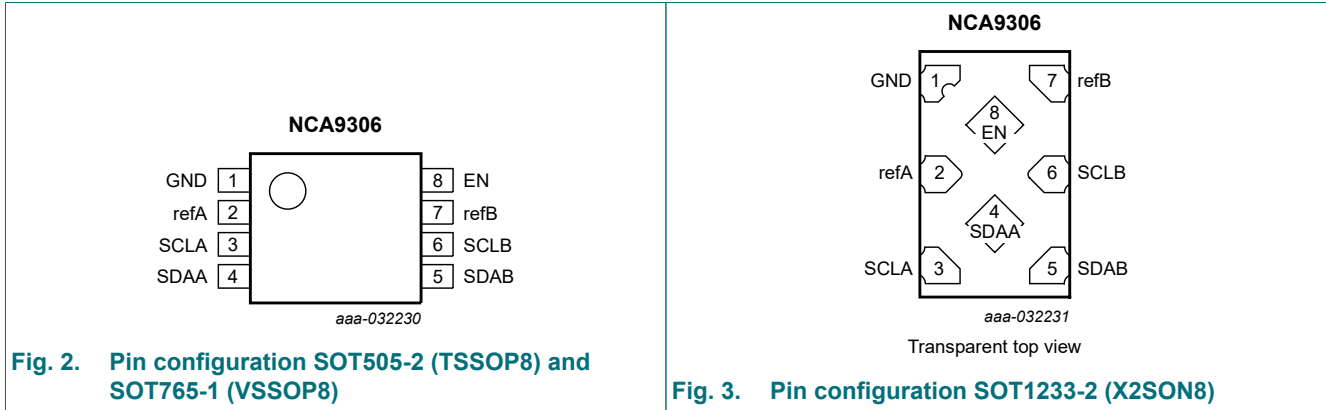


Fig. 2. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)

Fig. 3. Pin configuration SOT1233-2 (X2SON8)

### 7.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
GND	1	ground (0 V)
refA	2	low-voltage side reference supply voltage for SCLA and SDAA
SCLA, SCLB	3, 6	data input/output SCL
SDAA, SDAB	4, 5	data input/output SDA
refB	7	high-voltage side reference supply voltage for SCLB and SDAB
EN	8	enable input (active HIGH)

## 8. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input	input/output
EN	SCLn, SDAn channel
H	SCLA = SCLB; SDAA = SDAB
L	Z

## 9. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_I$	input voltage	pins refA, refB, SCLn, SDAn and EN [1]	-0.5	+7.0	V
$I_{I/O}$	input/output current	pins refA, refB, SCLn, SDAn; continuous channel current	-	+128	mA
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C			
		For SOT505-2 and SOT765-1 [2]	-	250	mW
		For SOT1233-2 [3]	-	300	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] For SOT505-2 (TSSOP8) package:  $P_{tot}$  derates linearly with 4.6 mW/K above 96 °C.

For SOT765-1 (VSSOP8) package:  $P_{tot}$  derates linearly with 4.9 mW/K above 99 °C.

[3] For SOT1233-2 (X2SON8) package:  $P_{tot}$  derates linearly with 7.7 mW/K above 118 °C.

## 10. Recommended operating conditions

**Table 6. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_I$	input voltage	pins refA, refB, SCLn, SDAn and EN	0.0	5.0	V
$I_{I/O}$	input/output current	pins refA, refB, SCLn, SDAn; continuous channel current	-	+64	mA
$T_{amb}$	ambient temperature		-40	+125	°C

## 11. Static characteristics

**Table 7. Static characteristics**

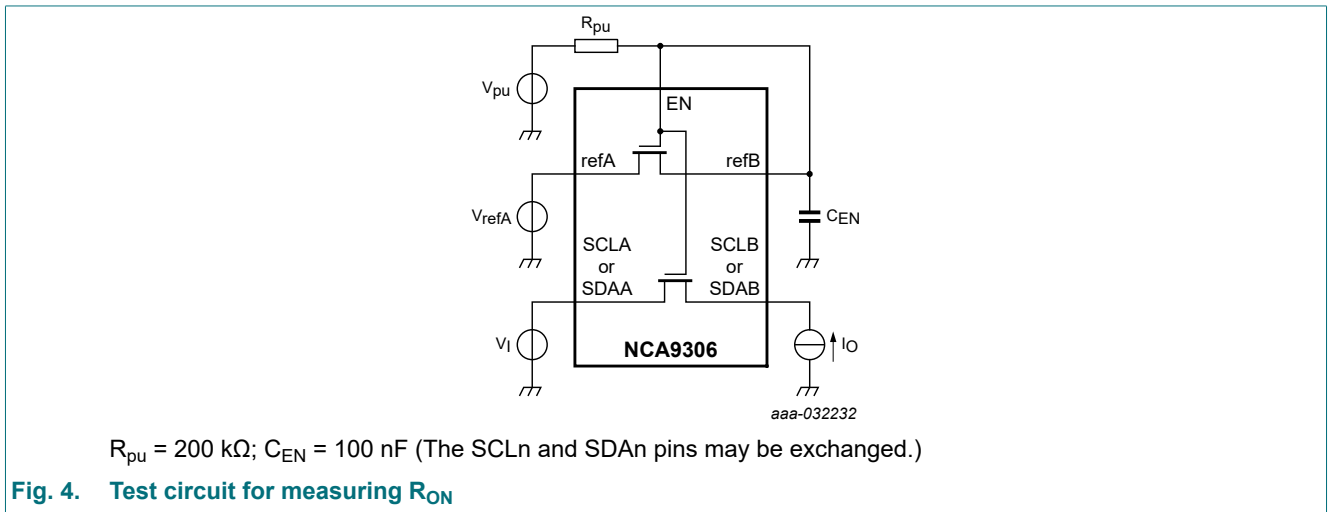
At recommended operating conditions voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$T_{amb} = -40$ °C to +125 °C			Unit
			Min	Typ[1]	Max	
$V_{IK}$	input clamping voltage	$V_{EN} = 0$ V; $I_I = -18$ mA	-1.2	-	-	V
$I_I$	leakage current	pins SCLn, SDAn, refA, refB and EN; $V_I = \text{GND to } 5.0$ V	-	1	5	μA
$C_I$	input capacitance	pins refA, refB and EN; $V_I = 0$ V or 3 V	-	6	-	pF
$C_{io(off)}$	OFF-state input/output capacitance	pins SCLn, SDAn; $V_O = 0$ V or 3 V; $V_{EN} = 0.0$ V	-	3.0	6.0	pF
$C_{io(on)}$	ON-state input/output capacitance	pins SCLn, SDAn; $V_O = 0$ V or 3 V; $V_{EN} = 3.0$ V	-	6.0	12.5	pF

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Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +125 °C			Unit
			Min	Typ[1]	Max	
R <sub>ON</sub>	ON resistance	see Fig. 4				
		V <sub>I</sub> = 0 V; V <sub>pu</sub> = 5.0 V; I <sub>O</sub> = 64 mA [2]				
		V <sub>refA</sub> = 3.3 V	-	3	7	Ω
		V <sub>refA</sub> = 1.8 V	-	4	10	Ω
		V <sub>I</sub> = 0 V; V <sub>refB</sub> = V <sub>EN</sub> = 5.0 V; I <sub>O</sub> = 32mA				
		V <sub>refA</sub> = 1.8 V	-	4	9	Ω
		V <sub>refA</sub> = 2.5 V	-	3	8	Ω
		V <sub>I</sub> = 1.8 V; V <sub>refB</sub> = V <sub>EN</sub> = 5.0 V; I <sub>O</sub> = 15 mA				
		V <sub>refA</sub> = 3.3 V	-	4	13	Ω
		V <sub>I</sub> = 1.0 V; V <sub>refB</sub> = V <sub>EN</sub> = 3.3 V; I <sub>O</sub> = 10 mA				
		V <sub>refA</sub> = 1.8 V	-	7	24	Ω
		V <sub>I</sub> = 0 V; V <sub>refB</sub> = V <sub>EN</sub> = 3.3 V; I <sub>O</sub> = 10 mA				
		V <sub>refA</sub> = 1.0 V	-	5	18	Ω
V <sub>I</sub> = 0 V; V <sub>refB</sub> = V <sub>EN</sub> = 1.8 V; I <sub>O</sub> = 10 mA						
V <sub>refA</sub> = 1.0 V	-	6	19	Ω		

- [1] All typical values are measured at T<sub>amb</sub> = 25 °C.
- [2] Measured by the voltage drop between the SCLn and SDAn pins at the indicated current through the switch. ON resistance is determined by the lowest voltage of the two (SCLn or SDAn) pins.



## 12. Dynamic characteristics

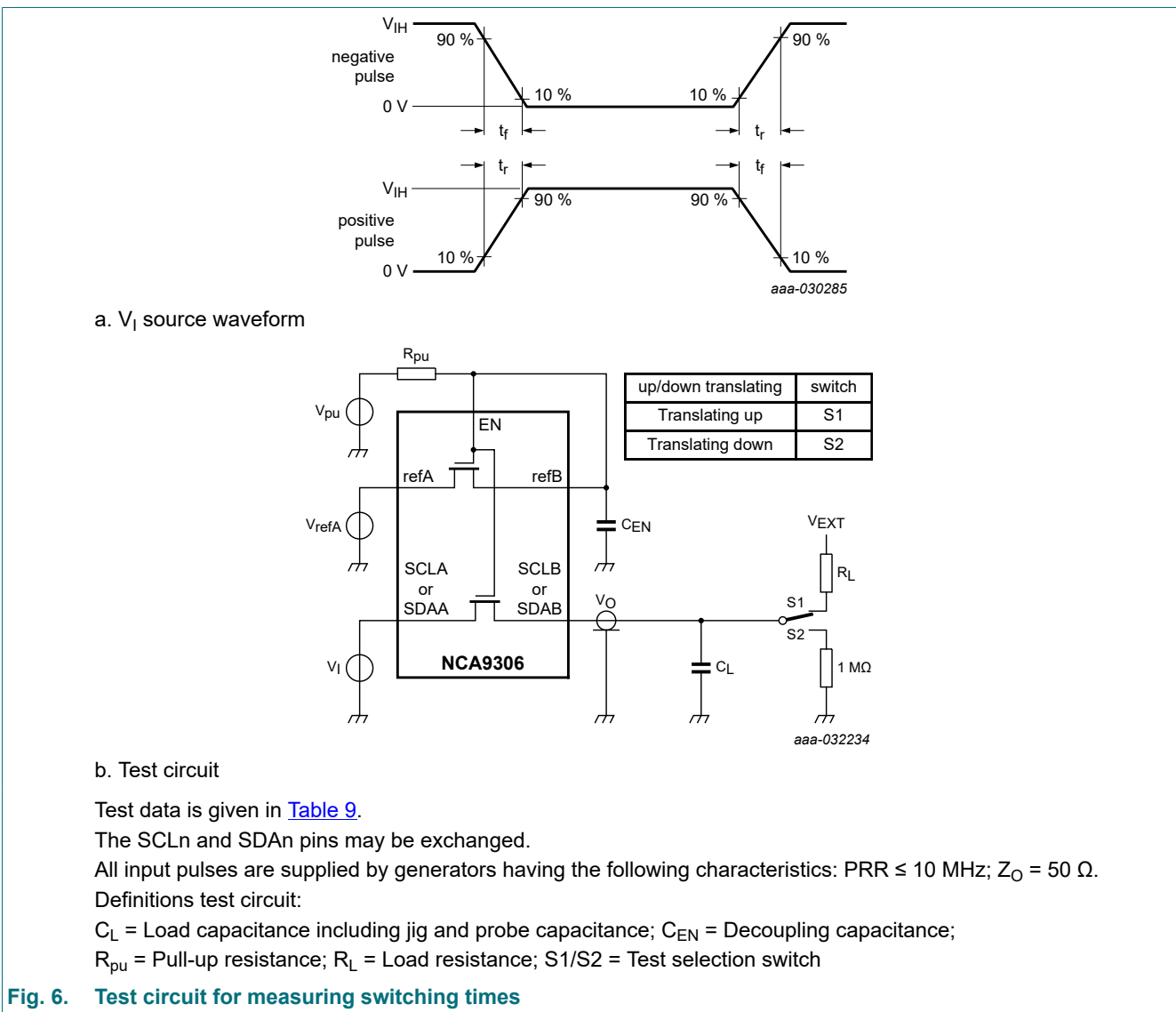
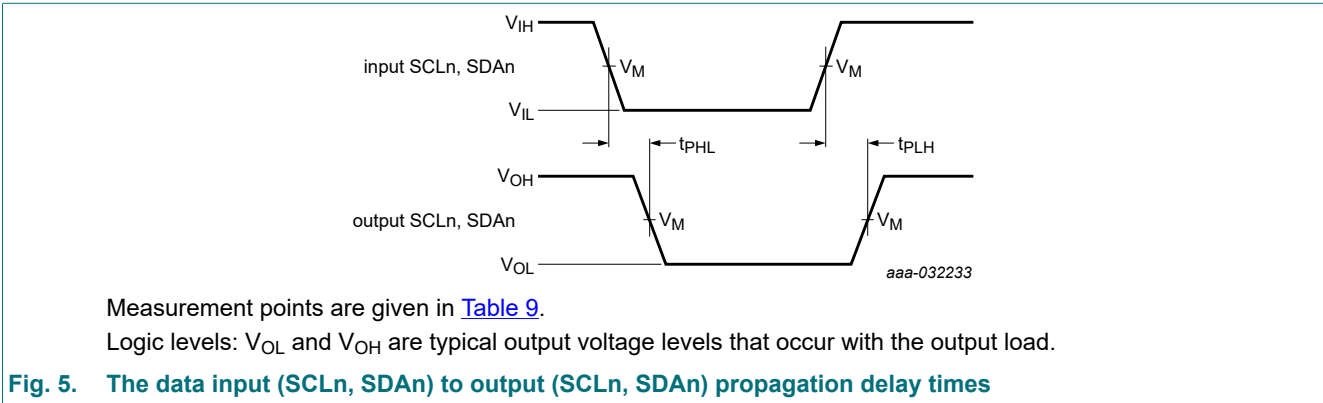
**Table 8. Switching characteristics**

$GND = 0\text{ V}$ ; for waveform see Fig. 5; for test circuit see Fig. 6

Symbol	Parameter	Conditions	$T_{\text{amb}} = -40\text{ °C to }+125\text{ °C}$			Unit
			Min	Typ[1]	Max	
<b>Translating down</b>						
$t_{\text{PLH}}$	LOW to HIGH propagation delay	SCLA, SDAA to SCLB, SDAB or SCLB, SDAB to SCLA, SDAA;				
		$V_{\text{IH}} = V_{\text{pu}} = V_{\text{refA}} + 1\text{ V}$				
		$V_{\text{refA}} = 1.5\text{ V}; C_{\text{L}} = 15\text{ pF}$	-	0.13	0.35	ns
		$V_{\text{refA}} = 1.5\text{ V}; C_{\text{L}} = 30\text{ pF}$	-	0.22	0.59	ns
		$V_{\text{refA}} = 1.5\text{ V}; C_{\text{L}} = 50\text{ pF}$	-	0.34	0.94	ns
		$V_{\text{refA}} = 2.3\text{ V}; C_{\text{L}} = 15\text{ pF}$	-	0.09	0.25	ns
		$V_{\text{refA}} = 2.3\text{ V}; C_{\text{L}} = 30\text{ pF}$	-	0.16	0.43	ns
		$V_{\text{refA}} = 2.3\text{ V}; C_{\text{L}} = 50\text{ pF}$	-	0.24	0.69	ns
$t_{\text{PHL}}$	HIGH to LOW propagation delay	SCLA, SDAA to SCLB, SDAB or SCLB, SDAB to SCLA, SDAA;				
		$V_{\text{IH}} = V_{\text{pu}} = V_{\text{refA}} + 1\text{ V}$				
		$V_{\text{refA}} = 1.5\text{ V}; C_{\text{L}} = 15\text{ pF}$	-	0.21	0.99	ns
		$V_{\text{refA}} = 1.5\text{ V}; C_{\text{L}} = 30\text{ pF}$	-	0.36	1.78	ns
		$V_{\text{refA}} = 1.5\text{ V}; C_{\text{L}} = 50\text{ pF}$	-	0.51	2.42	ns
		$V_{\text{refA}} = 2.3\text{ V}; C_{\text{L}} = 15\text{ pF}$	-	0.12	0.45	ns
		$V_{\text{refA}} = 2.3\text{ V}; C_{\text{L}} = 30\text{ pF}$	-	0.19	0.77	ns
		$V_{\text{refA}} = 2.3\text{ V}; C_{\text{L}} = 50\text{ pF}$	-	0.30	1.17	ns
<b>Translating up</b>						
$t_{\text{PLH}}$	LOW to HIGH propagation delay	SCLA, SDAA to SCLB, SDAB or SCLB, SDAB to SCLA, SDAA;				
		$V_{\text{IH}} = V_{\text{refA}}; V_{\text{EXT}} = V_{\text{pu}} = V_{\text{refA}} + 1\text{ V}$				
		$V_{\text{refA}} = 1.5\text{ V}; C_{\text{L}} = 15\text{ pF}$	-	0.06	0.11	ns
		$V_{\text{refA}} = 1.5\text{ V}; C_{\text{L}} = 30\text{ pF}$	-	0.14	0.32	ns
		$V_{\text{refA}} = 1.5\text{ V}; C_{\text{L}} = 50\text{ pF}$	-	0.26	0.58	ns
		$V_{\text{refA}} = 2.3\text{ V}; C_{\text{L}} = 15\text{ pF}$	-	0.06	0.13	ns
		$V_{\text{refA}} = 2.3\text{ V}; C_{\text{L}} = 30\text{ pF}$	-	0.13	0.28	ns
		$V_{\text{refA}} = 2.3\text{ V}; C_{\text{L}} = 50\text{ pF}$	-	0.20	0.50	ns
$t_{\text{PHL}}$	HIGH to LOW propagation delay	SCLA, SDAA to SCLB, SDAB or SCLB, SDAB to SCLA, SDAA;				
		$V_{\text{IH}} = V_{\text{refA}}; V_{\text{EXT}} = V_{\text{pu}} = V_{\text{refA}} + 1\text{ V}$				
		$V_{\text{refA}} = 1.5\text{ V}; C_{\text{L}} = 15\text{ pF}$	-	0.34	1.54	ns
		$V_{\text{refA}} = 1.5\text{ V}; C_{\text{L}} = 30\text{ pF}$	-	0.60	2.60	ns
		$V_{\text{refA}} = 1.5\text{ V}; C_{\text{L}} = 50\text{ pF}$	-	0.90	3.82	ns
		$V_{\text{refA}} = 2.3\text{ V}; C_{\text{L}} = 15\text{ pF}$	-	0.17	0.71	ns
		$V_{\text{refA}} = 2.3\text{ V}; C_{\text{L}} = 30\text{ pF}$	-	0.29	1.09	ns
		$V_{\text{refA}} = 2.3\text{ V}; C_{\text{L}} = 50\text{ pF}$	-	0.45	1.67	ns

[1] All typical values are measured at  $T_{\text{amb}} = 25\text{ °C}$ .

12.1. Waveforms and test circuit



## 2-bit bidirectional multi-voltage level translator; open-drain; push-pull

Table 9. Test data

Input		Output	Load			
$t_r, t_f$	$V_M$	$V_M$	$C_L$	$C_{EN}$ [1]	$R_L$ [1]	$R_{pu}$
$\leq 2$ ns	$0.5V_{refA}$	$0.5V_{refA}$	15 pF, 30 pF, 50 pF	100 nF	300 $\Omega$	200 k $\Omega$

[1] All typical values are measured at  $T_{amb} = 25$  °C.



### 13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

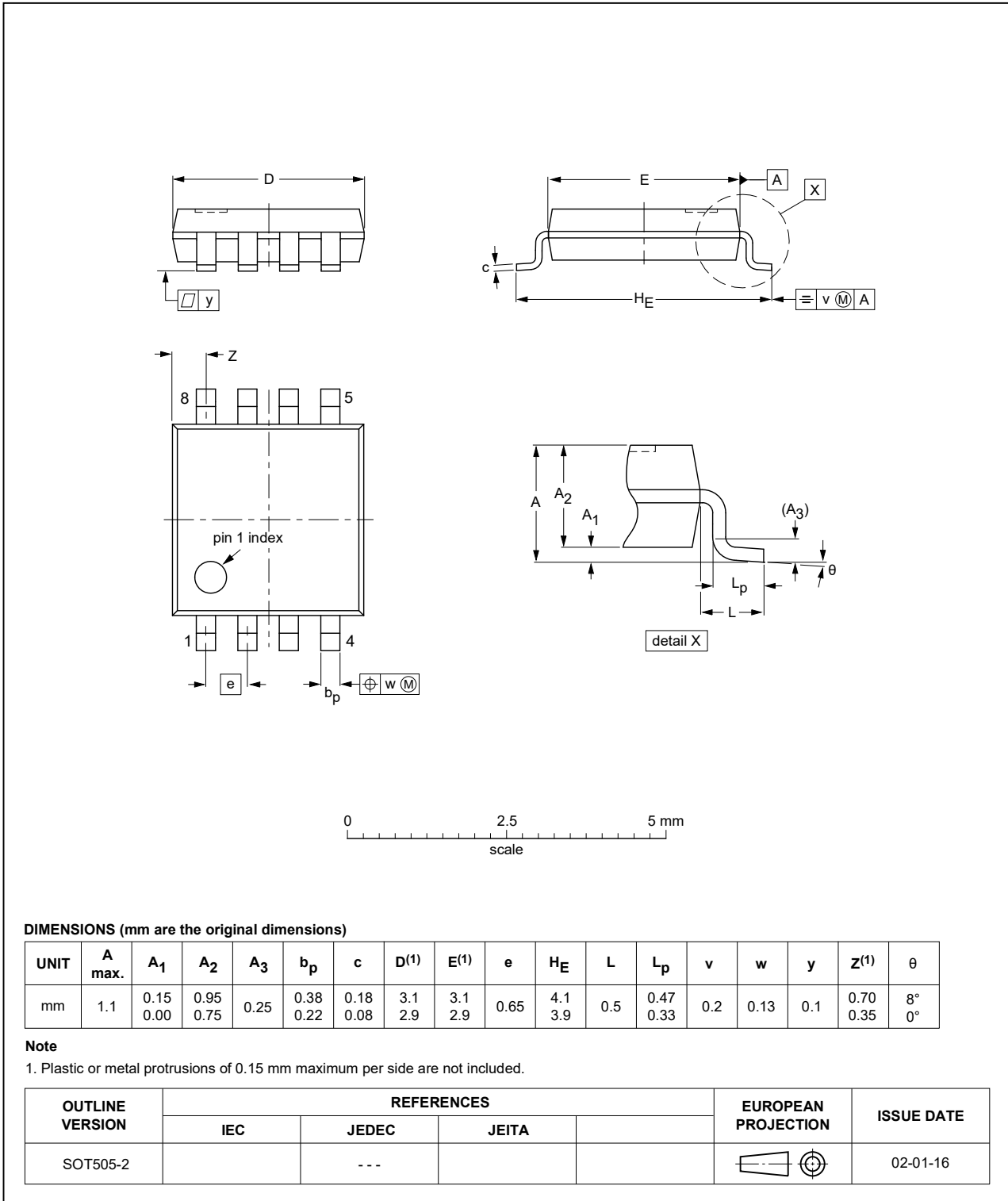


Fig. 7. Package outline SOT505-2 (TSSOP8)

2-bit bidirectional multi-voltage level translator; open-drain; push-pull

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

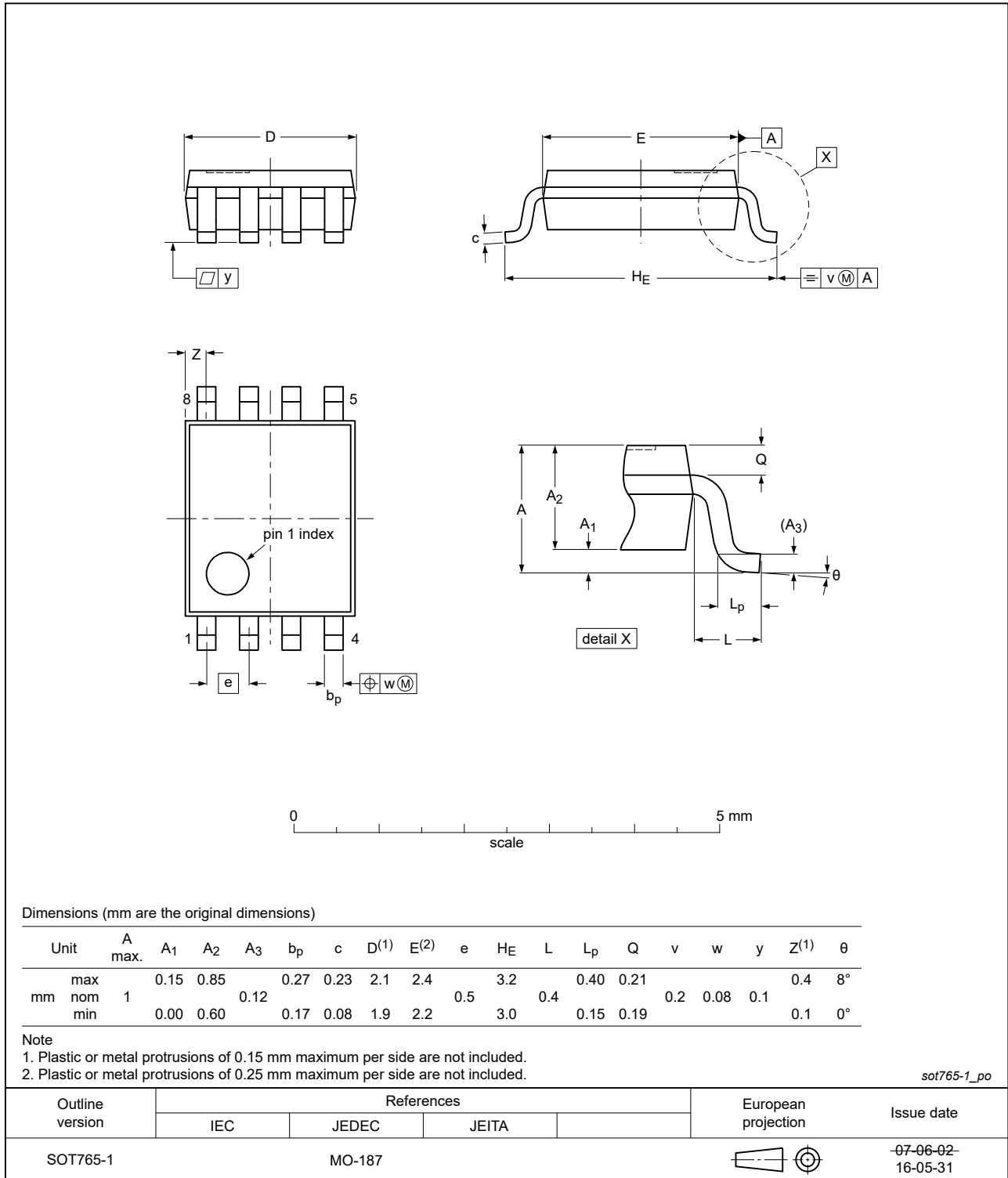


Fig. 8. Package outline SOT765-1 (VSSOP8)

2-bit bidirectional multi-voltage level translator; open-drain; push-pull

X2SON8: plastic thermal enhanced extremely thin small outline package; no leads; 8 terminals; body 1.35 x 0.8 x 0.32 mm

SOT1233-2

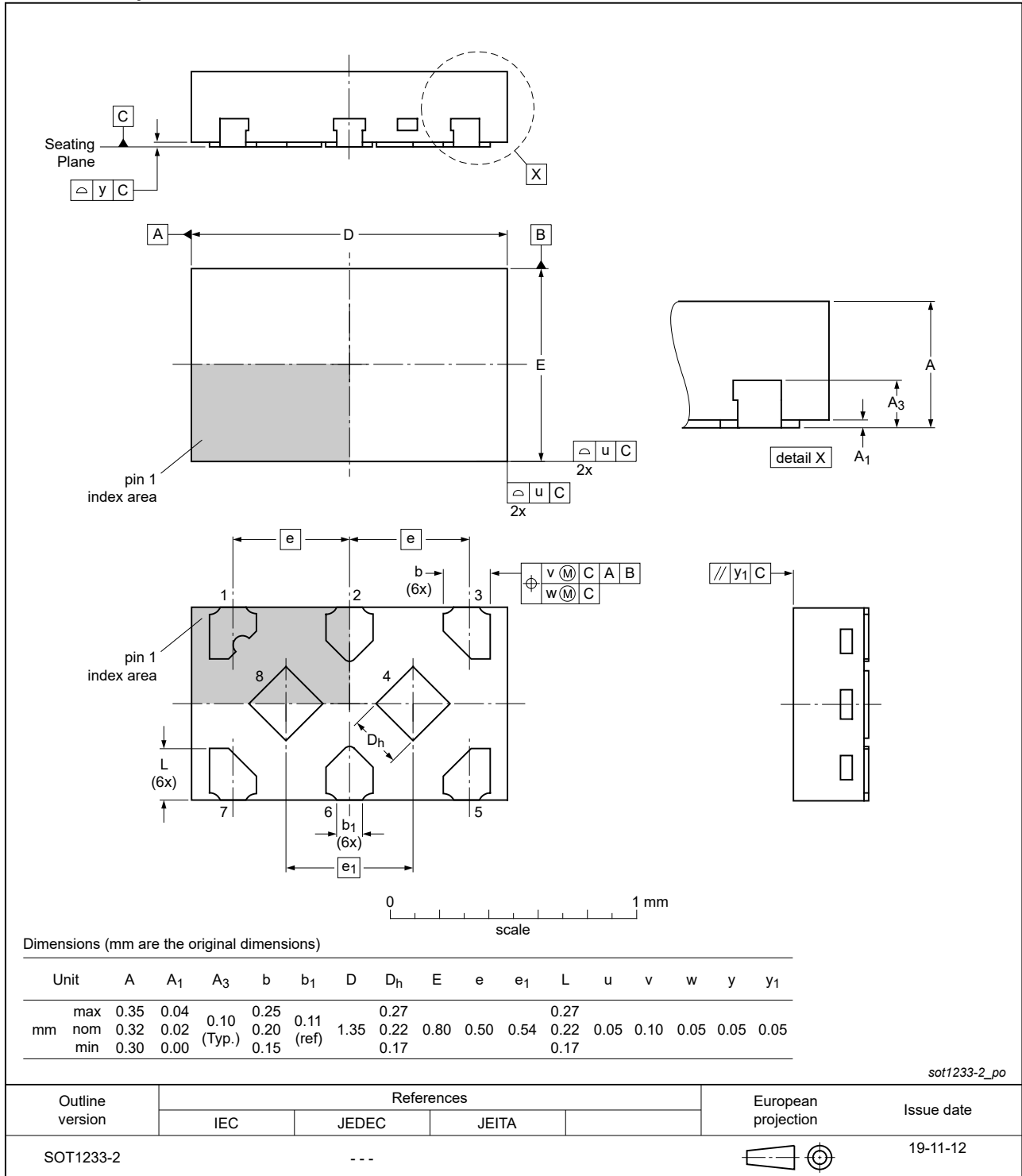


Fig. 9. Package outline SOT1233-2 (X2SON8)

## 14. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
I <sup>2</sup> C	Inter-Integrated Circuit
PMBus	Power Management Bus
PRR	Pulse Rate Repetition
SMBus	System Management Bus

## 15. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
NCA9306 v.2	20211126	Product data sheet	-	NCA9306 v.1
Modifications:	• <a href="#">Table 3</a> : Typo corrected in the description of pin refB (errata).			
NCA9306 v.1	20200922	Product data sheet	-	-

## 16. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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