74LV165-Q100

8-bit parallel-in/serial-out shift register

Rev. 3 — 21 September 2021 Product data sheet

1. General description

The 74LV165-Q100 is an 8-bit serial or parallel-in/serial-out shift register. The device features a serial data input (DS), eight parallel data inputs (D0 to D7) and two complementary serial outputs (Q7 and $\overline{Q7}$). When the parallel load input ($\overline{PL}$) is LOW the data from D0 to D7 is loaded into the shift register asynchronously. When $\overline{PL}$ is HIGH data enters the register serially at DS. When the clock enable input ($\overline{CE}$) is LOW data is shifted on the LOW-to-HIGH transitions of the CP input. A HIGH on $\overline{CE}$ will disable the CP input. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess V_{CC}.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 1.0 to 5.5 V
- CMOS low power dissipation
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Synchronous parallel-to-serial applications
- Synchronous serial input for easy expansion
- Complies with JEDEC standards:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C (2.7 V to 3.6 V)
  - JESD36 (4.5 V to 5.5 V)
- ESD protection:
  - MIL-STD-833, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV165D-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LV165PW-Q100	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

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4. Functional diagram

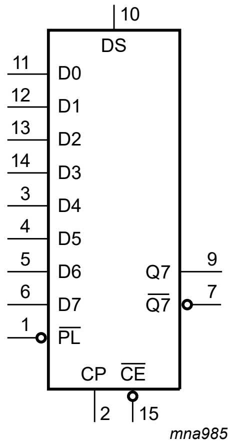


Fig. 1. Logic symbol

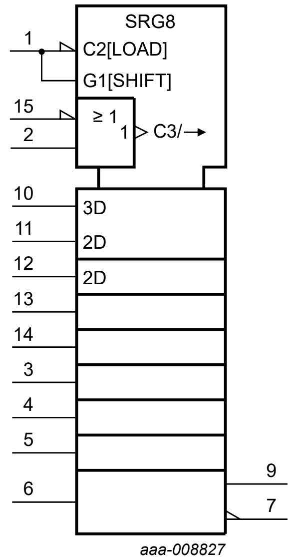


Fig. 2. IEC logic symbol

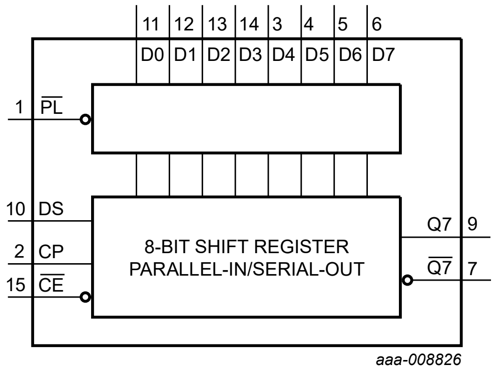


Fig. 3. Functional diagram

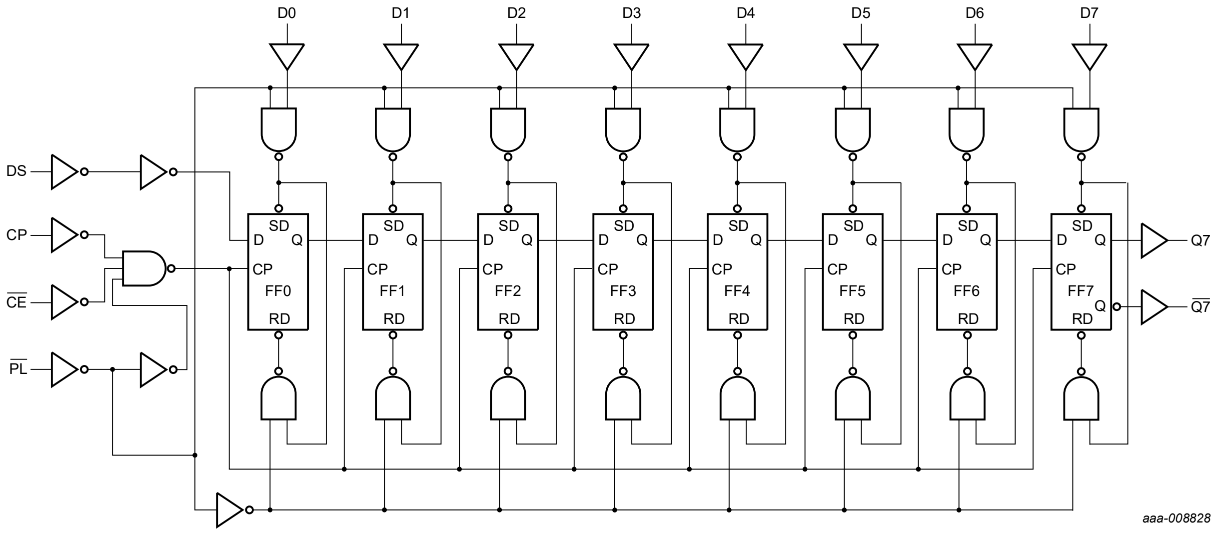


Fig. 4. Logic diagram

5. Pinning information

5.1. Pinning

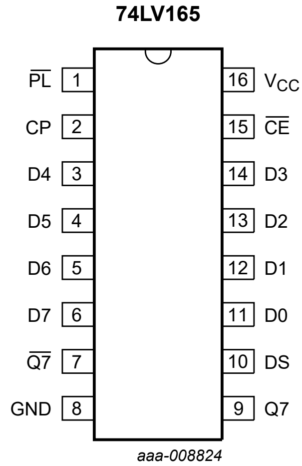


Fig. 5. Pin configuration SOT109-1 (SO16) and SOT403-1 (TSSOP16)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{PL}$	1	parallel enable input (active LOW)
CP	2	clock input (LOW-to-HIGH edge-triggered)
$\overline{Q7}$	7	complementary serial output from the last stage
GND	8	ground (0 V)
Q7	9	serial output from the last stage
DS	10	serial data input
D0, D1, D2, D3, D4, D5, D6, D7	11, 12, 13, 14, 3, 4, 5, 6	parallel data inputs
$\overline{CE}$	15	clock enable input (active LOW)
V_{CC}	16	positive supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
q = state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition;
X = don't care; ↑ = LOW-to-HIGH clock transition.

Operating modes	Inputs					Qn registers		Output	
	$\overline{PL}$	$\overline{CE}$	CP	DS	D0 to D7	Q0	Q1 to Q6	Q7	$\overline{Q7}$
parallel load	L	X	X	X	L	L	L to L	L	H
	L	X	X	X	H	H	H to H	H	L
serial shift	H	L	↑	l	X	L	q0 to q5	q6	$\overline{q6}$
	H	L	↑	h	X	H	q0 to q5	q6	$\overline{q6}$
hold "do nothing"	H	H	X	X	X	q0	q1 to q6	q7	q7

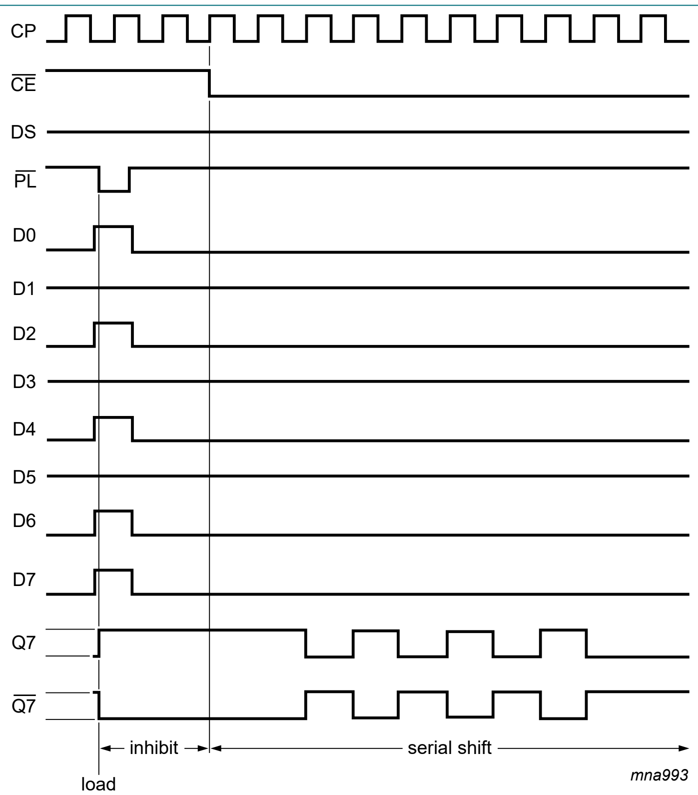


Fig. 6. Timing diagram

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V) [1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	20	mA
V_I	input voltage		-0.5	+7	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$	-	±50	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V	-	±25	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.0	3.3	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.0 V to 2.0 V	0	-	500	ns/V
		V_{CC} = 2.0 V to 2.7 V	0	-	200	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	-	100	ns/V
		V_{CC} = 3.6 V to 5.5 V	0	-	50	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	0.9	-	-	0.9	-	V
		V_{CC} = 2.3 V to 2.7 V	1.4	-	-	1.4	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V_{CC} = 4.5 V to 5.5 V	$0.7V_{CC}$	-	-	$0.7V_{CC}$	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.3	-	0.3	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.6	-	0.6	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	$0.3V_{CC}$	-	$0.3V_{CC}$	
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; I_O = -100 μA						
		V_{CC} = 1.2 V	-	1.2		-		
		V_{CC} = 2.0 V	1.8	2.0	-	1.8	-	V
		V_{CC} = 2.7 V	2.5	2.7	-	2.5	-	V
		V_{CC} = 3.0 V	2.8	3.0	-	2.8	-	V
		V_{CC} = 4.5 V	4.3	4.5	-	4.3	-	V
		standard outputs: $V_I = V_{IH}$ or V_{IL}						
		V_{CC} = 3.0 V; I_O = -6 mA	2.40	2.82	-	2.20	-	V
		V_{CC} = 4.5 V; I_O = -12 mA	3.60	4.20	-	3.50	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; I_O = 100 μA						
		V_{CC} = 1.2 V	-	0	-	-	-	
		V_{CC} = 2.0 V	-	0	0.2	1.8	0.2	V
		V_{CC} = 2.7 V	-	0	0.2	2.5	0.2	V
		V_{CC} = 3.0 V	-	0	0.2	2.8	0.2	V
		V_{CC} = 4.5 V	-	0	0.2	4.3	0.2	V
		standard outputs: $V_I = V_{IH}$ or V_{IL}						
		V_{CC} = 3.0 V; I_O = 6 mA	-	0.25	0.40	-	0.50	V
		V_{CC} = 4.5 V; I_O = 12 mA	-	0.35	0.55	-	0.65	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±1	-	±1	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	20	-	160	μA
ΔI_{CC}	additional supply current	$V_I = V_{CC} - 0.6$ V; V_{CC} = 2.7 V to 3.6 V	-	-	500	-	850	μA
C_I	input capacitance		-	3.5	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V); for test circuit, see Fig. 12

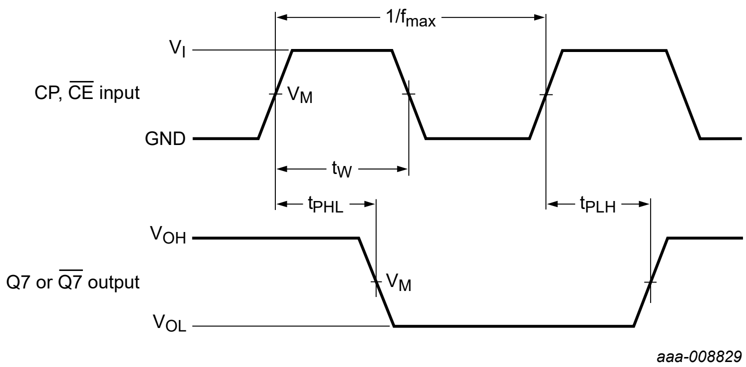
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	$\overline{CE}$, CP to Q7, $\overline{Q7}$; see Fig. 7 and Fig. 8 [2]						
		V_{CC} = 1.2 V	-	115	-	-	-	ns
		V_{CC} = 2.0 V	-	38	61	-	76	ns
		V_{CC} = 2.7 V	-	27	43	-	54	ns
		V_{CC} = 3.0 V to 3.6 V [3]	-	22	36	-	45	ns
		V_{CC} = 3.3 V; C_L = 15 pF	-	18	-	-	-	ns
		V_{CC} = 4.5 V to 5.5 V [4]	-	15	24	-	30	ns
		$\overline{PL}$ to Q7, $\overline{Q7}$; see Fig. 8						
		V_{CC} = 1.2 V	-	110	-	-	-	ns
		V_{CC} = 2.0 V	-	35	56	-	70	ns
		V_{CC} = 2.7 V	-	24	39	-	49	ns
		V_{CC} = 3.0 V to 3.6 V [3]	-	20	33	-	41	ns
		V_{CC} = 3.3 V; C_L = 15 pF	-	18	-	-	-	ns
		V_{CC} = 4.5 V to 5.5 V [4]	-	14	22	-	27	ns
		D7 to Q7, $\overline{Q7}$; see Fig. 9						
		V_{CC} = 1.2 V	-	90	-	-	-	ns
		V_{CC} = 2.0 V	-	28	45	-	56	ns
		V_{CC} = 2.7 V	-	20	32	-	40	ns
		V_{CC} = 3.0 V to 3.6 V [3]	-	17	27	-	33	ns
		V_{CC} = 3.3 V; C_L = 15 pF	-	14	-	-	-	ns
		V_{CC} = 4.5 V to 5.5 V [4]	-	11	18	-	22	ns
t_W	pulse width	CP input HIGH to LOW; see Fig. 7						
		V_{CC} = 2.0 V	34	10	-	41	-	ns
		V_{CC} = 2.7 V	25	8	-	30	-	ns
		V_{CC} = 3.0 V to 3.6 V [3]	20	7	-	24	-	ns
		V_{CC} = 4.5 V to 5.5 V [4]	15	5	-	18	-	ns
		$\overline{PL}$ input LOW; see Fig. 8						
		V_{CC} = 2.0 V	34	10	-	41	-	ns
		V_{CC} = 2.7 V	25	8	-	30	-	ns
		V_{CC} = 3.0 V to 3.6 V [3]	20	7	-	24	-	ns
		V_{CC} = 4.5 V to 5.5 V [4]	15	5	-	18	-	ns
t_{rec}	recovery time	$\overline{PL}$ to CP, $\overline{CE}$; see Fig. 8						
		V_{CC} = 1.2 V	-	40	-	-	-	ns
		V_{CC} = 2.0 V	24	15	-	30	-	ns
		V_{CC} = 2.7 V	18	11	-	23	-	ns
		V_{CC} = 3.0 V to 3.6 V [3]	17	10	-	21	-	ns
		V_{CC} = 4.5 V to 5.5 V [4]	12	7	-	15	-	ns

Symbol	Parameter	Conditions		-40 °C to +85 °C			-40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{su}	set-up time	DS to CP, $\overline{CE}$; see Fig. 10							
		V_{CC} = 1.2 V		-	-8	-	-	-	ns
		V_{CC} = 2.0 V		22	-2	-	26	-	ns
		V_{CC} = 2.7 V		16	-1	-	19	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	13	-1	-	15	-	ns
		V_{CC} = 4.5 V to 5.5 V	[4]	9	0	-	10	-	ns
		$\overline{CE}$ to CP, CP to $\overline{CE}$; see Fig. 10							
		V_{CC} = 1.2 V		-	20	-	-	-	ns
		V_{CC} = 2.0 V		22	7	-	26	-	ns
		V_{CC} = 2.7 V		16	5	-	19	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	13	4	-	15	-	ns
		V_{CC} = 4.5 V to 5.5 V	[4]	9	3	-	10	-	ns
		Dn to $\overline{PL}$; see Fig. 11							
		V_{CC} = 1.2 V		-	25	-	-	-	ns
		V_{CC} = 2.0 V		22	8	-	26	-	ns
		V_{CC} = 2.7 V		16	6	-	19	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	13	5	-	15	-	ns
		V_{CC} = 4.5 V to 5.5 V	[4]	9	4	-	10	-	ns
t_h	hold time	DS to CP, $\overline{CE}$; Dn to $\overline{PL}$; see Fig. 10 and Fig. 11							
		V_{CC} = 1.2 V		-	20	-	-	-	ns
		V_{CC} = 2.0 V		22	7	-	26	-	ns
		V_{CC} = 2.7 V		16	5	-	19	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	13	4	-	15	-	ns
		V_{CC} = 4.5 V to 5.5 V	[4]	9	3	-	10	-	ns
		$\overline{CE}$ to CP, CP to $\overline{CE}$; see Fig. 10							
		V_{CC} = 1.2 V		-	-30	-	-	-	ns
		V_{CC} = 2.0 V		5	-8	-	5	-	ns
		V_{CC} = 2.7 V		5	-6	-	5	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	5	-5	-	5	-	ns
		V_{CC} = 4.5 V to 5.5 V	[4]	5	-4	-	5	-	ns
f_{max}	maximum frequency	see Fig. 7							
		V_{CC} = 2.0 V		14	40	-	12	-	MHz
		V_{CC} = 2.7 V		19	60	-	16	-	MHz
		V_{CC} = 3.0 V to 3.6 V	[3]	24	65	-	20	-	MHz
		V_{CC} = 3.3 V; C_L = 15 pF		-	78	-	-	-	MHz
		V_{CC} = 4.5 V to 5.5 V	[4]	36	75	-	30	-	MHz

Symbol	Parameter	Conditions		-40 °C to +85 °C			-40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}; V_{CC} = 3.3 V	[5]	-	35	-	-	-	pF

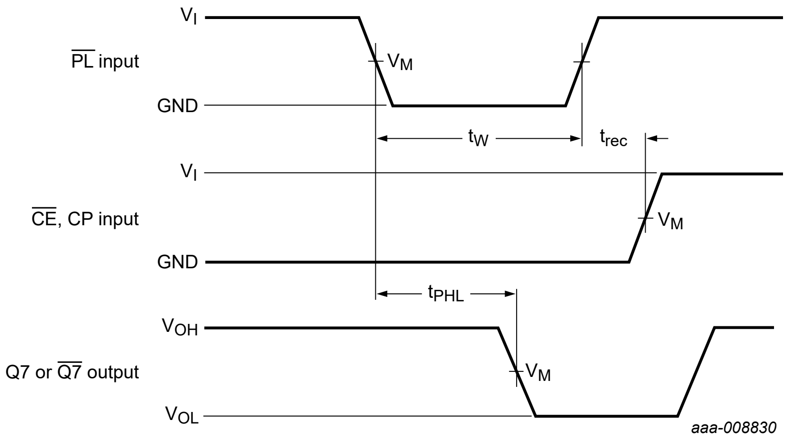
[1] Typical values are measured at T_{amb} = 25 °C.
[2] t_{pd} is the same as t_{PHL} and t_{PLH}.
[3] Typical values are measured at V_{CC} = 3.3 V.
[4] Typical values are measured at V_{CC} = 5.0 V.
[5] C_{PD} is used to determine the dynamic power dissipation $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ (P_D in μW), where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V.

10.1. Waveforms and test circuit



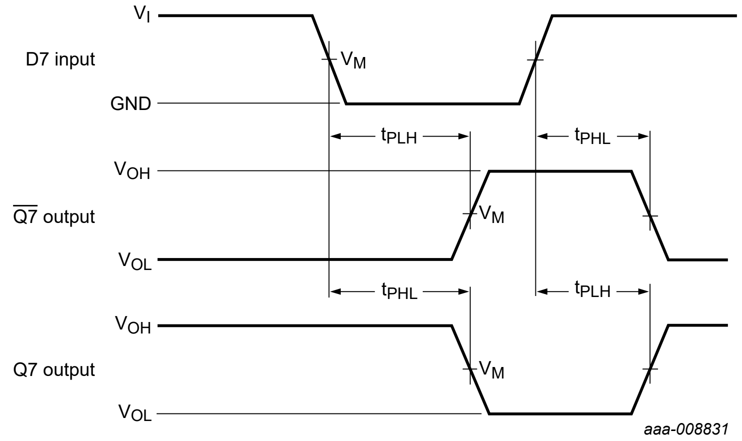
Measurement points are given in Table 8.
The changing to output assumes that internal Q6 is opposite state from Q7.

Fig. 7. Clock pulse (CP) and clock enable (CE) to output (Q7 or Q7) propagation delays, clock pulse width and maximum clock frequency



Measurement points are given in Table 8.
The changing to output assumes that internal Q6 is opposite state from Q7.

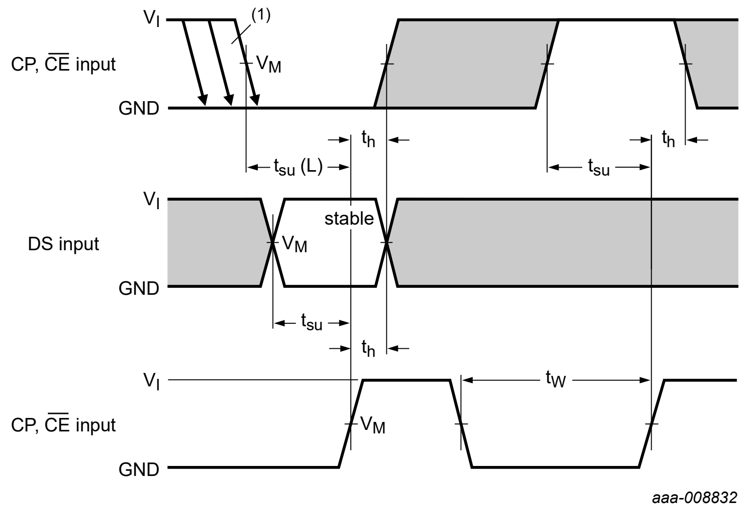
Fig. 8. Parallel load (PL) pulse width, parallel load to output (Q7 or Q7) propagation delays, parallel load to clock (CP) and clock enable (CE) recovery time



Measurement points are given in Table 8.

The changing to output assumes that internal Q6 is opposite state from Q7.

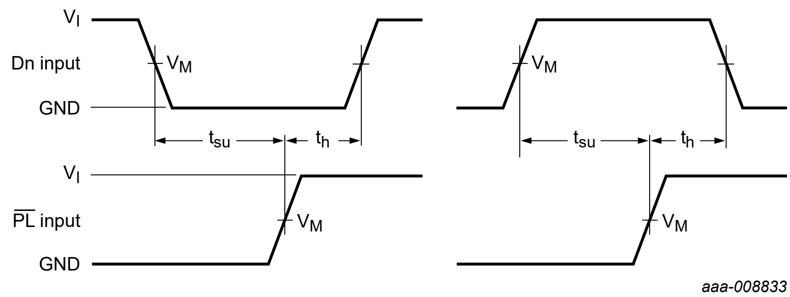
Fig. 9. Data input (Dn) to output (Q7 or Q̄7) propagation delays when P̄L̄ is LOW



Measurement points are given in Table 8.

(1) CE may change only from HIGH-to-LOW while CP is LOW. The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 10. Set-up and hold times

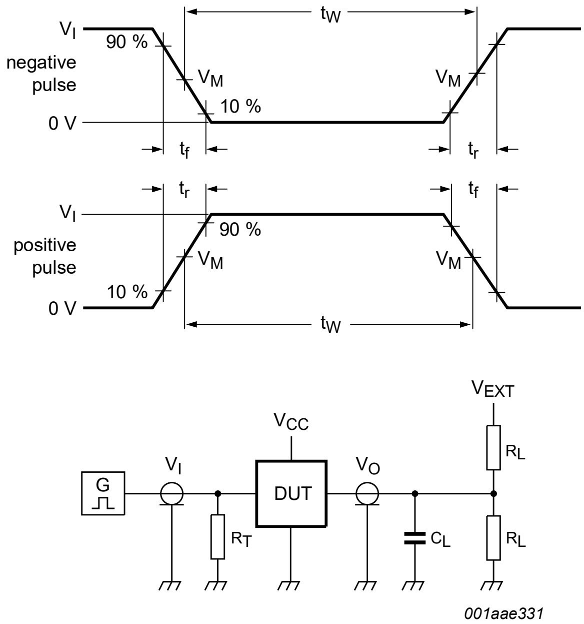


Measurement points are given in Table 8.

Fig. 11. Set-up and hold times from the data inputs (Dn) to the parallel load input (P̄L̄)

Table 8. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V
≥ 4.5 V	$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

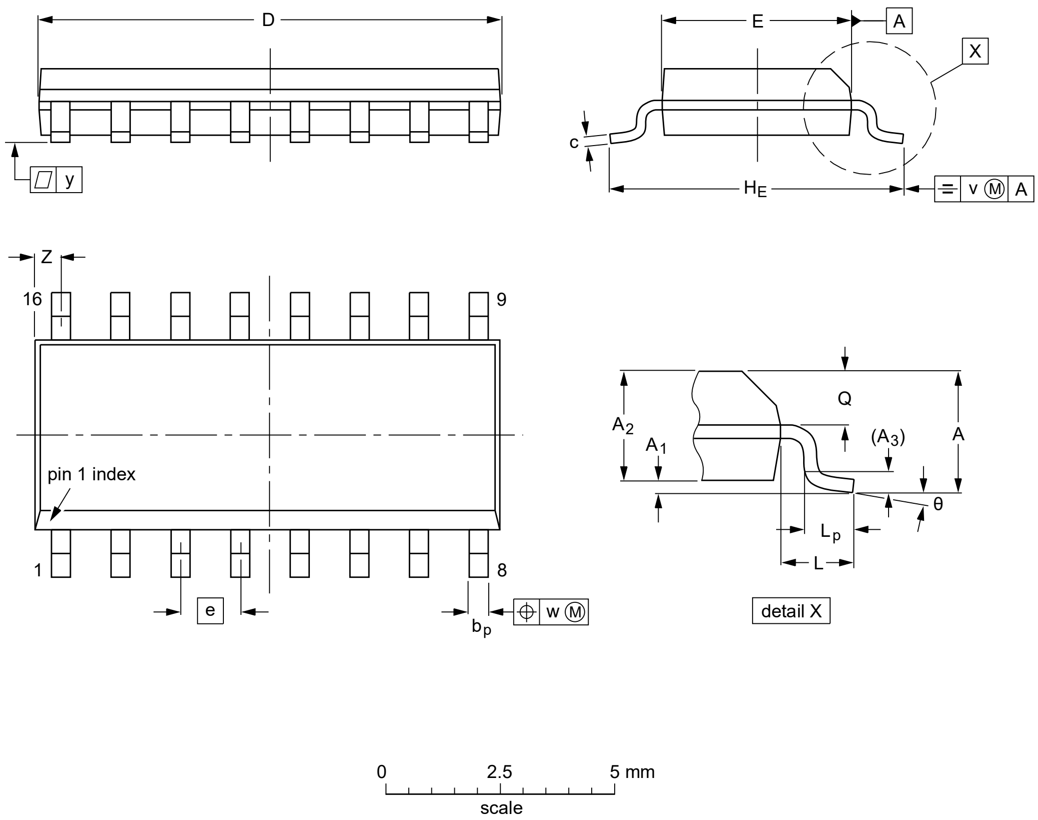
Fig. 12. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
< 2.7 V	V_{CC}	2.5 ns	50 pF	1 kΩ	open
2.7 V to 3.6 V	2.7 V	2.5 ns	50 pF, 15 pF	1 kΩ	open
≥ 4.5 V	V_{CC}	2.5 ns	50 pF	1 kΩ	open

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

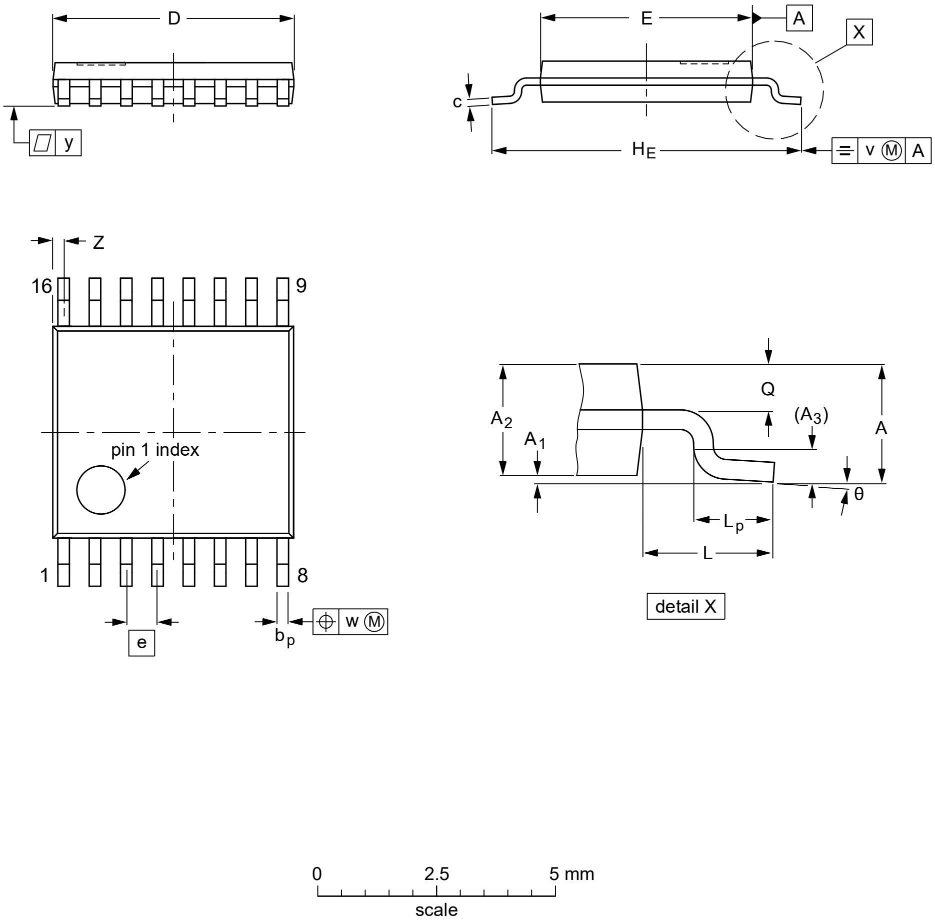
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig. 13. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig. 14. Package outline SOT403-1 (TSSOP16)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV165_Q100 v.3	20210921	Product data sheet	-	74LV165_Q100 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 and Section 2 updated. • Section 7: Derating values for P_{tot} total power dissipation updated.			
74LV165_Q100 v.2	20140224	Product data sheet	-	74LV165_Q100 v.1
Modifications:	• Typo corrected in Table 2			
74LV165_Q100 v.1	20131111	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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