

# 74HC107; 74HCT107

Dual JK flip-flop with reset; negative-edge trigger

Rev. 6 — 7 July 2021

Product data sheet

## 1. General description

The 74HC107; 74HCT107 is a dual negative edge triggered JK flip-flop featuring individual J and K inputs, clock ( $\overline{CP}$ ) and reset ( $\overline{R}$ ) inputs and complementary Q and  $\overline{Q}$  outputs. The reset is an asynchronous active LOW input and operates independently of the clock input. The J and K inputs control the state changes of the flip-flops as described in the mode select function table. The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

## 2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- Input levels:
  - The 74HC107: CMOS levels
  - The 74HCT107: TTL levels
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC107D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HCT107D				
74HC107PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

4. Functional diagram

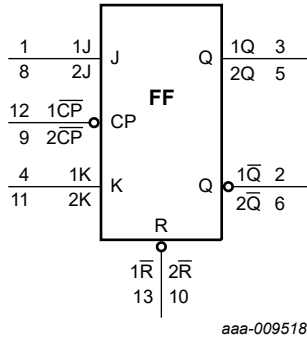


Fig. 1. Logic symbol

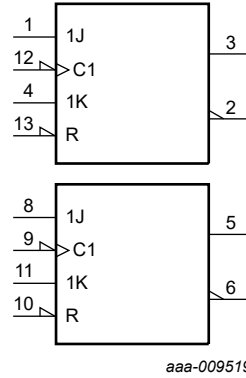


Fig. 2. IEC logic symbol

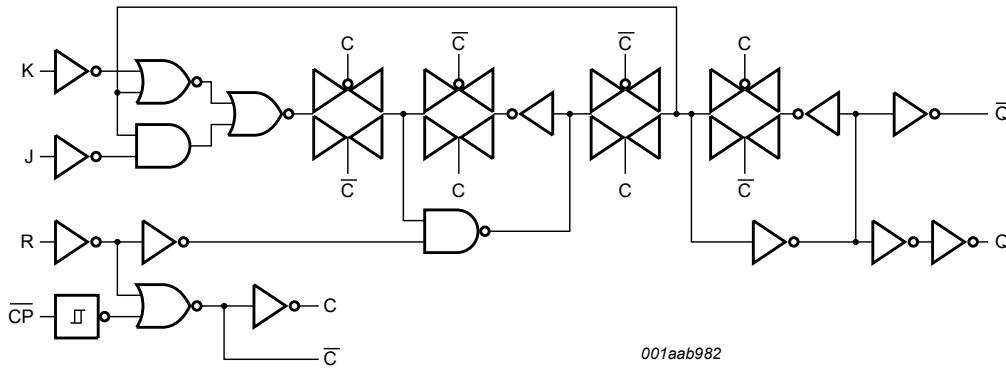


Fig. 3. Logic diagram (one flip-flop)

## 5. Pinning information

### 5.1. Pinning

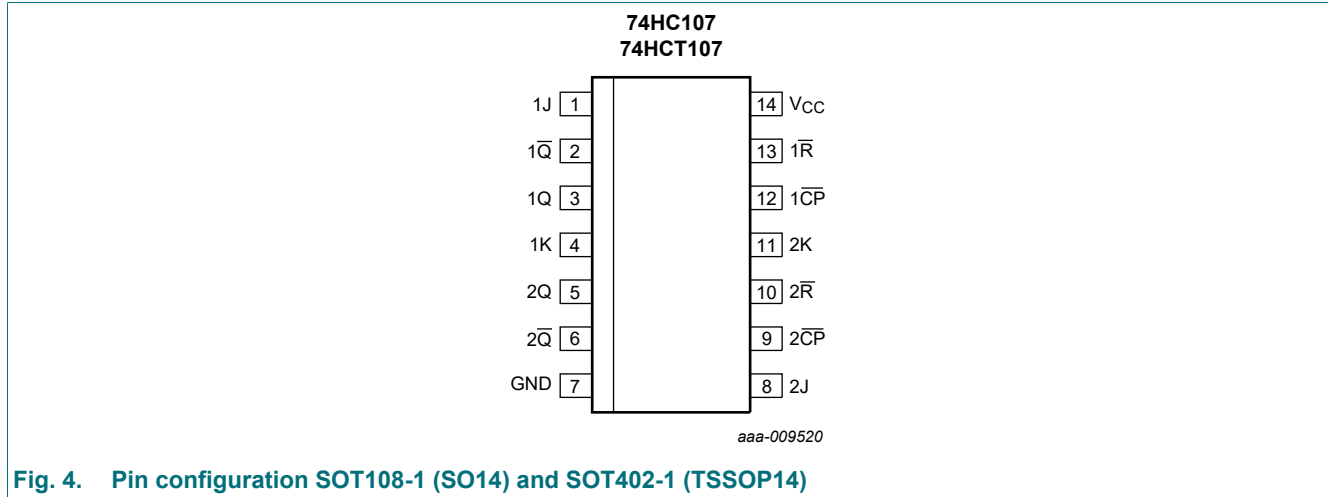


Fig. 4. Pin configuration SOT108-1 (SO14) and SOT402-1 (TSSOP14)

### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1J, 2J	1, 8	synchronous J input
1 $\bar{Q}$ , 2 $\bar{Q}$	2, 6	complement output
1Q, 2Q	3, 5	true output
1K, 2K	4, 11	synchronous K input
1 $\bar{C}P$ , 2 $\bar{C}P$	12, 9	clock input (HIGH-to-LOW edge-triggered)
1 $\bar{R}$ , 2 $\bar{R}$	13, 10	asynchronous reset input (active LOW)
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the HIGH-to-LOW clock transition;

L = LOW voltage level; l = LOW voltage level one set-up time prior to the HIGH-to-LOW clock transition;

q = state of referenced output one set-up time prior to the HIGH-to-LOW clock transition; X = don't care;

↓ = HIGH-to-LOW clock transition.

Input				Output		Operating mode
R	CP	J	K	Q	$\bar{Q}$	
L	X	X	X	L	H	asynchronous reset
H	↓	h	h	$\bar{q}$	q	toggle
H	↓	l	h	L	H	load 0 (reset)
H	↓	h	l	H	L	load 1 (set)
H	↓	l	l	q	$\bar{q}$	hold (no change)

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ [1]	-	$\pm 20$	mA
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ [1]	-	$\pm 20$	mA
$I_O$	output current	$V_O = -0.5\text{ V}$ to $V_{CC} + 0.5\text{ V}$	-	$\pm 25$	mA
$I_{CC}$	supply current		-	50	mA
$I_{GND}$	ground current		-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package:  $P_{tot}$  derates linearly with 10.1 mW/K above 100 °C.  
For SOT402-1 (TSSOP14) package:  $P_{tot}$  derates linearly with 7.3 mW/K above 81 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC107			74HCT107			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC107</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
		V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	4.0	-	40	-	80	μA
C <sub>I</sub>	input capacitance		-	3.5	-					pF
<b>74HCT107</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4 mA	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 20 μA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA	-	0.16	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	4.0	-	40	-	80	μA

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$\Delta I_{CC}$	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}$ ; $I_O = 0 \text{ A}$ ; other inputs at $V_{CC}$ or GND; $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$								
		pin $\overline{nCP}$ , nJ	-	100	360	-	450	-	490	$\mu\text{A}$
		pin $\overline{nR}$	-	65	234	-	293	-	319	$\mu\text{A}$
		pin nK	-	60	216	-	270	-	294	$\mu\text{A}$
$C_I$	input capacitance		-	3.5	-	-	-	-	-	pF

## 10. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V);  $C_L = 50 \text{ pF}$  unless otherwise specified; for test circuit, see Fig. 7

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC107</b>										
$t_{pd}$	propagation delay	$\overline{nCP}$ to nQ; see Fig. 5 [1]								
		$V_{CC} = 2.0 \text{ V}$	-	52	160	-	200	-	240	ns
		$V_{CC} = 4.5 \text{ V}$	-	19	32	-	40	-	48	ns
		$V_{CC} = 5.0 \text{ V}$ ; $C_L = 15 \text{ pF}$	-	16	-	-	-	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	-	15	27	-	34	-	41	ns
		$\overline{nCP}$ to $\overline{nQ}$ ; see Fig. 5								
		$V_{CC} = 2.0 \text{ V}$	-	52	160	-	200	-	240	ns
		$V_{CC} = 4.5 \text{ V}$	-	19	32	-	40	-	48	ns
		$V_{CC} = 5.0 \text{ V}$ ; $C_L = 15 \text{ pF}$	-	16	-	-	-	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	-	15	27	-	34	-	41	ns
		$\overline{nR}$ to nQ, $\overline{nQ}$ ; see Fig. 6								
		$V_{CC} = 2.0 \text{ V}$	-	52	155	-	195	-	235	ns
		$V_{CC} = 4.5 \text{ V}$	-	19	31	-	39	-	47	ns
		$V_{CC} = 5.0 \text{ V}$ ; $C_L = 15 \text{ pF}$	-	16	-	-	-	-	-	ns
$V_{CC} = 6.0 \text{ V}$	-	15	26	-	33	-	40	ns		
$t_t$	transition time	nQ, $\overline{nQ}$ ; see Fig. 5 [2]								
		$V_{CC} = 2.0 \text{ V}$	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5 \text{ V}$	-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0 \text{ V}$	-	6	13	-	16	-	19	ns

## Dual JK flip-flop with reset; negative-edge trigger

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$t_w$	pulse width	$\overline{nCP}$ input, HIGH or LOW; see Fig. 5								
		$V_{CC} = 2.0\text{ V}$	80	22	-	100	-	120	-	ns
		$V_{CC} = 4.5\text{ V}$	16	8	-	20	-	24	-	ns
		$V_{CC} = 6.0\text{ V}$	14	6	-	17	-	20	-	ns
		$\overline{nR}$ input, HIGH or LOW; see Fig. 6								
		$V_{CC} = 2.0\text{ V}$	80	22	-	100	-	120	-	ns
		$V_{CC} = 4.5\text{ V}$	16	8	-	20	-	24	-	ns
		$V_{CC} = 6.0\text{ V}$	14	6	-	17	-	20	-	ns
$t_{rec}$	recovery time	$\overline{nR}$ to $\overline{nCP}$ ; see Fig. 6								
		$V_{CC} = 2.0\text{ V}$	60	19	-	75	-	90	-	ns
		$V_{CC} = 4.5\text{ V}$	12	7	-	15	-	18	-	ns
		$V_{CC} = 6.0\text{ V}$	20	6	-	13	-	15	-	ns
$t_{su}$	set-up time	$nJ, nK$ to $\overline{nCP}$ ; see Fig. 5								
		$V_{CC} = 2.0\text{ V}$	100	22	-	125	-	150	-	ns
		$V_{CC} = 4.5\text{ V}$	20	8	-	25	-	30	-	ns
		$V_{CC} = 6.0\text{ V}$	17	6	-	21	-	26	-	ns
$t_h$	hold time	$nJ, nK$ to $\overline{nCP}$ ; see Fig. 5								
		$V_{CC} = 2.0\text{ V}$	3	-6	-	3	-	3	-	ns
		$V_{CC} = 4.5\text{ V}$	3	-2	-	3	-	3	-	ns
		$V_{CC} = 6.0\text{ V}$	3	-2	-	3	-	3	-	ns
$f_{max}$	maximum frequency	$\overline{nCP}$ input; see Fig. 5								
		$V_{CC} = 2.0\text{ V}$	6	23	-	4.8	-	4.0	-	MHz
		$V_{CC} = 4.5\text{ V}$	30	70	-	24	-	20	-	MHz
		$V_{CC} = 5.0\text{ V}; C_L = 15\text{ pF}$	-	78	-	-	-	-	-	MHz
		$V_{CC} = 6.0\text{ V}$	35	85	-	28	-	24	-	MHz
$C_{PD}$	power dissipation capacitance	per flip-flop; $V_I = \text{GND to } V_{CC}$ [3]	-	30	-	-	-	-	-	pF
<b>74HCT107</b>										
$t_{pd}$	propagation delay	$\overline{nCP}$ to $nQ$ ; see Fig. 5 [1]								
		$V_{CC} = 4.5\text{ V}$	-	19	36	-	45	-	54	ns
		$V_{CC} = 5.0\text{ V}; C_L = 15\text{ pF}$	-	16	-	-	-	-	-	ns
		$\overline{nCP}$ to $\overline{nQ}$ ; see Fig. 5								
		$V_{CC} = 4.5\text{ V}$	-	21	36	-	45	-	54	ns
		$V_{CC} = 5.0\text{ V}; C_L = 15\text{ pF}$	-	18	-	-	-	-	-	ns
		$\overline{nR}$ to $nQ, \overline{nQ}$ ; see Fig. 6								
		$V_{CC} = 4.5\text{ V}$	-	20	38	-	48	-	57	ns
$t_t$	transition time	$nQ, \overline{nQ}$ ; see Fig. 5 [2]								
		$V_{CC} = 4.5\text{ V}$	-	7	15	-	19	-	22	ns

## Dual JK flip-flop with reset; negative-edge trigger

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t <sub>w</sub>	pulse width	nCP̄ input, HIGH or LOW; see Fig. 5								
		V <sub>CC</sub> = 4.5 V	16	9	-	20	-	24	-	ns
		nR̄ input, HIGH or LOW; see Fig. 6								
		V <sub>CC</sub> = 4.5 V	20	11	-	25	-	30	-	ns
t <sub>rec</sub>	recovery time	nR̄ to nCP̄; see Fig. 6								
		V <sub>CC</sub> = 4.5 V	14	8	-	18	-	21	-	ns
t <sub>su</sub>	set-up time	nJ, nK to nCP̄; see Fig. 5								
		V <sub>CC</sub> = 4.5 V	20	7	-	25	-	30	-	ns
t <sub>h</sub>	hold time	nJ, nK to nCP̄; see Fig. 5								
		V <sub>CC</sub> = 4.5 V	5	-2	-	5	-	5	-	ns
f <sub>max</sub>	maximum frequency	nCP̄ input; see Fig. 5								
		V <sub>CC</sub> = 4.5 V	30	66	-	24	-	20	-	MHz
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	73	-	-	-	-	-	MHz
C <sub>PD</sub>	power dissipation capacitance	per flip-flop; V <sub>I</sub> = GND to V <sub>CC</sub> - 1.5 V [3]	-	30	-	-	-	-	-	pF

[1] t<sub>pd</sub> is the same as t<sub>PHL</sub>, t<sub>PLH</sub>.

[2] t<sub>i</sub> is the same as t<sub>THL</sub>, t<sub>TLH</sub>.

[3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs.



10.1. Waveforms and test circuit

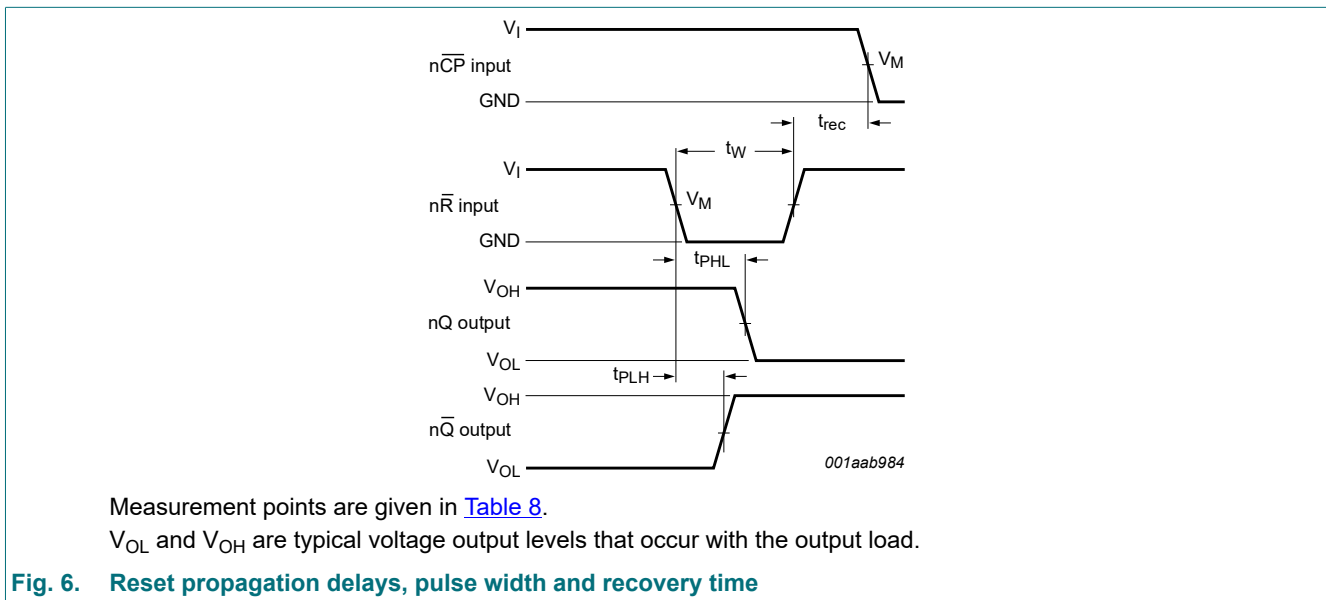
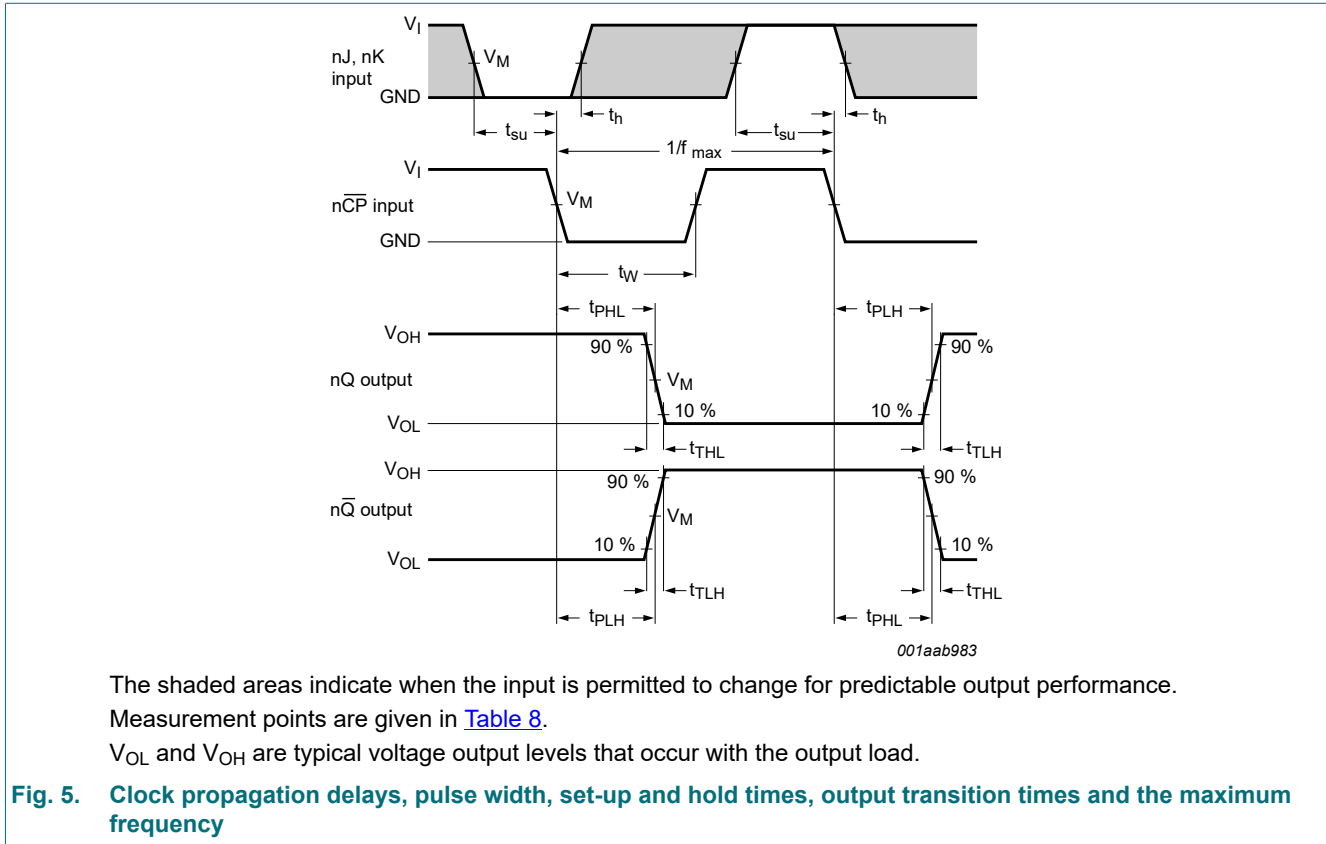


Table 8. Measurement points

Type	Input		Output
	$V_I$	$V_M$	$V_M$
74HC107	$V_{CC}$	$0.5V_{CC}$	$0.5V_{CC}$
74HCT107	3 V	1.3 V	1.3 V

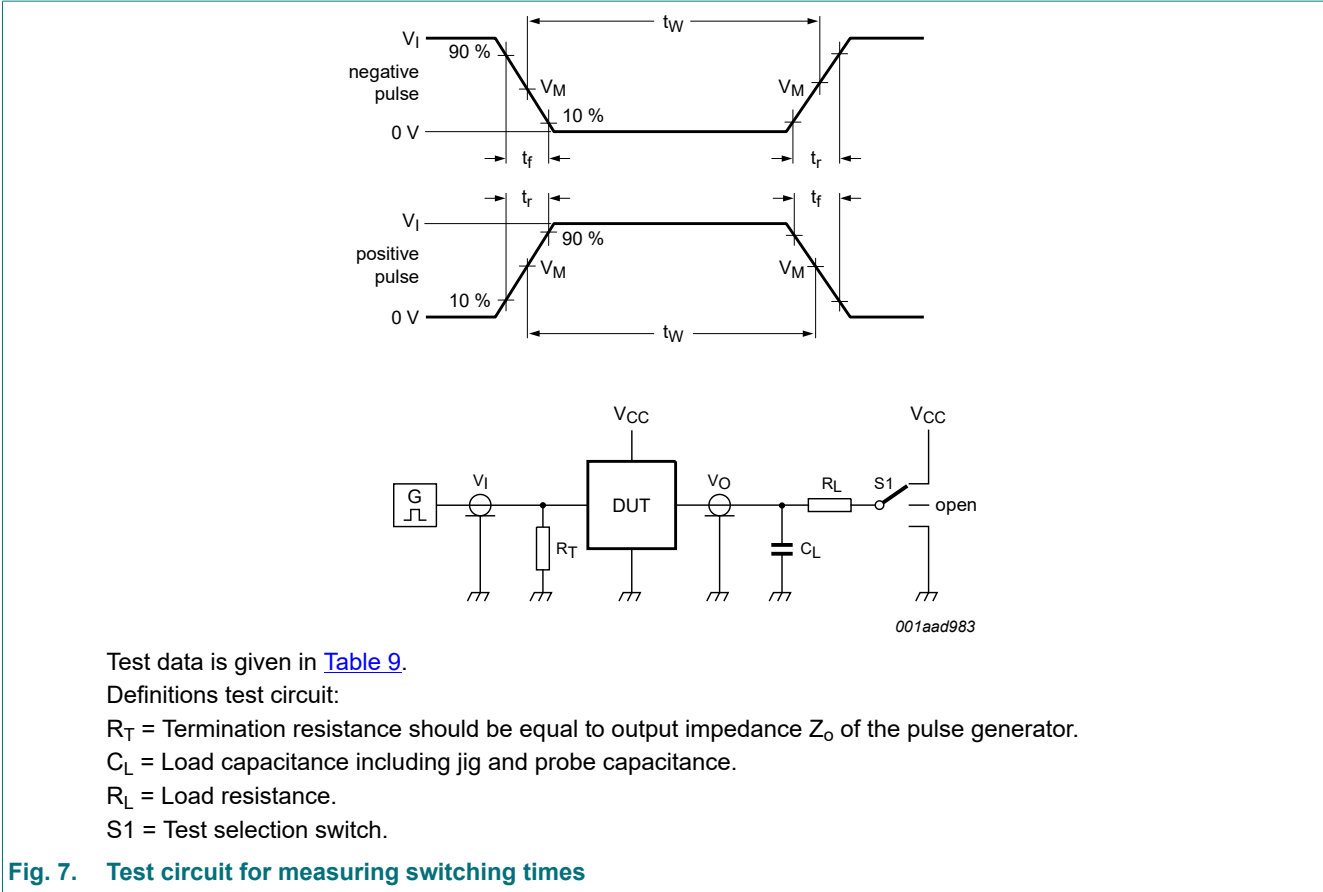


Fig. 7. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
74HC107	$V_{CC}$	6 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$
74HCT107	3 V	6 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

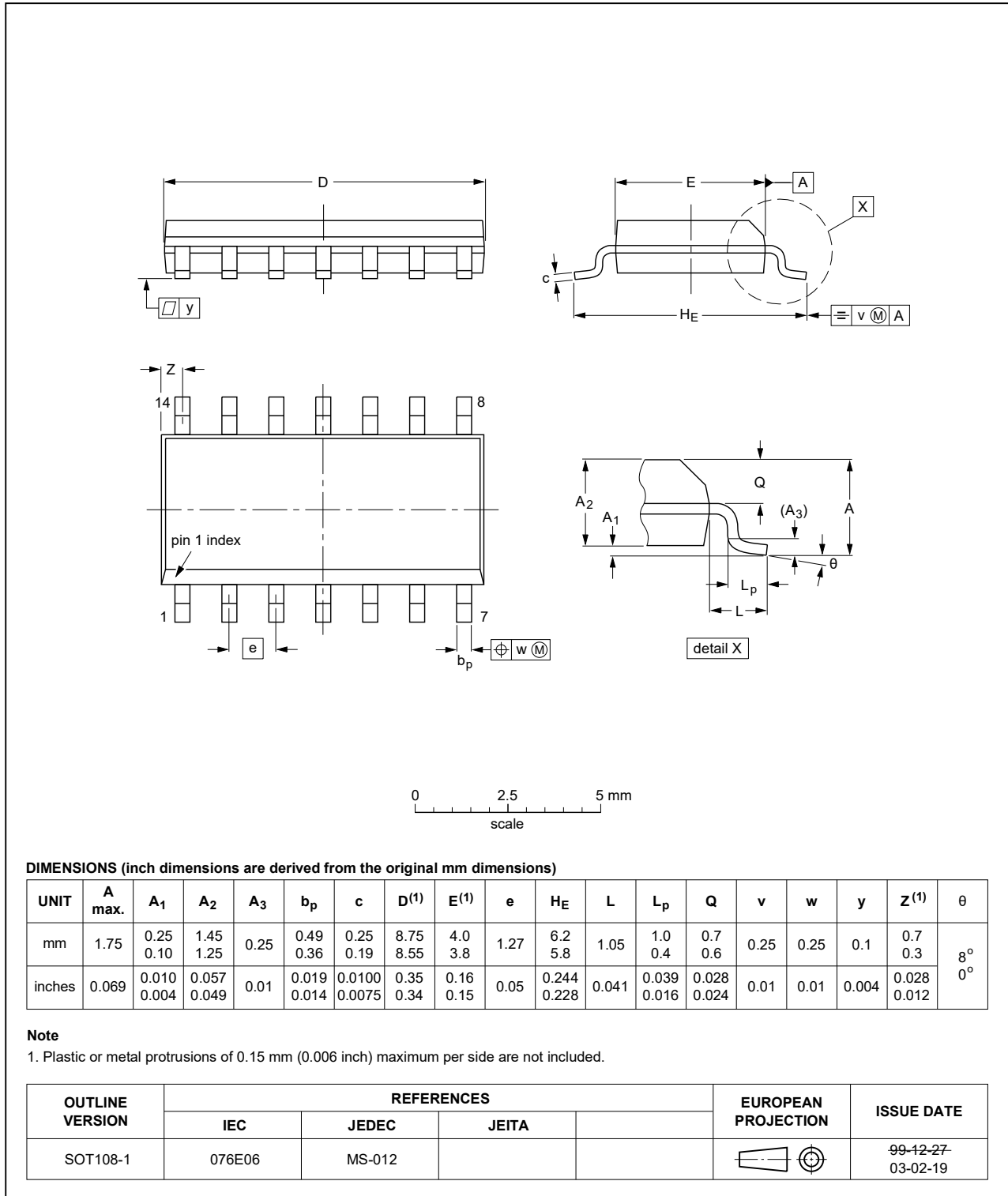


Fig. 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

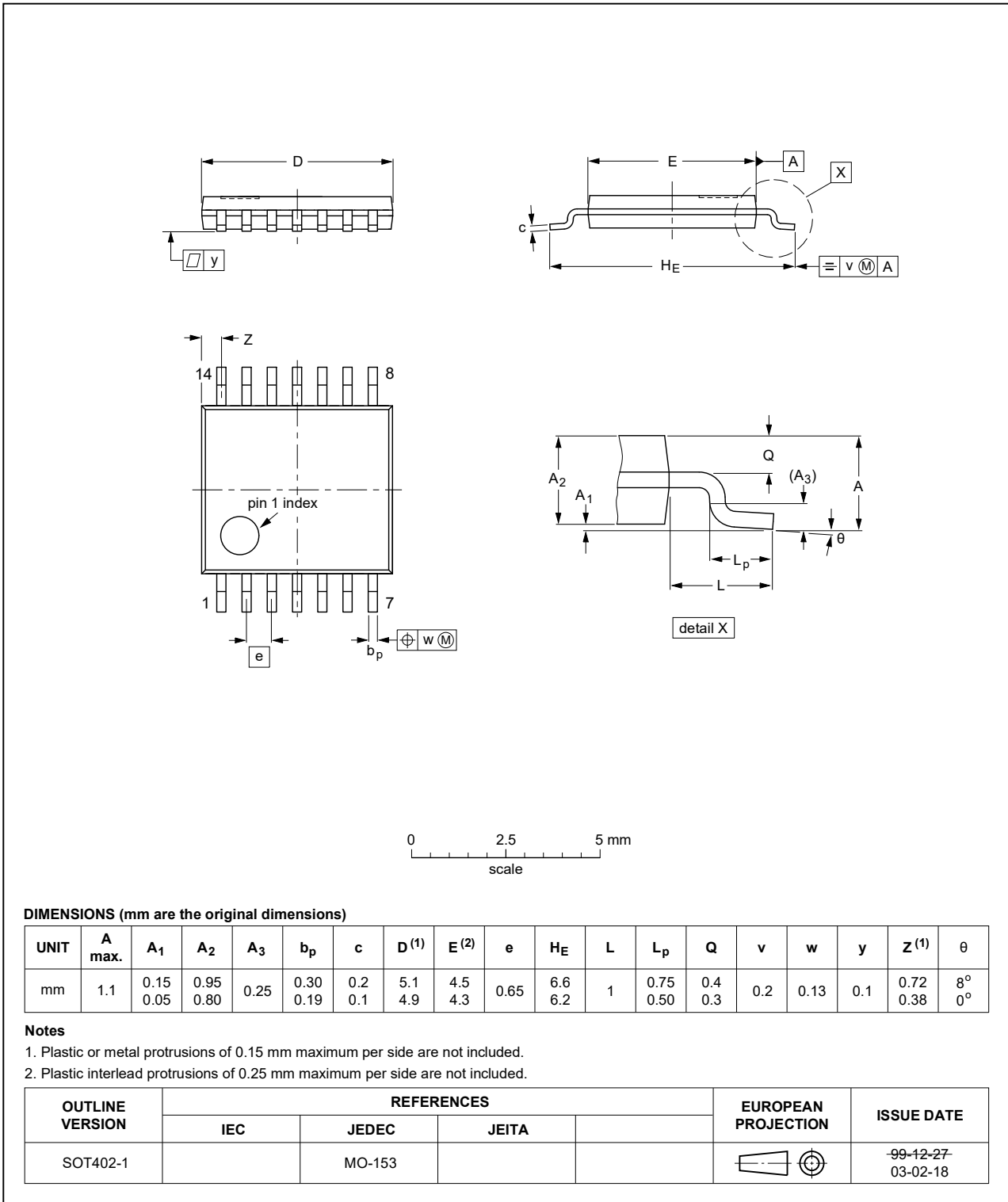


Fig. 9. Package outline SOT402-1 (TSSOP14)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT107 v.6	20210707	Product data sheet	-	74HC_HCT107 v.5
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 2</a> updated.</li> <li><a href="#">Section 7</a>: Derating values for <math>P_{tot}</math> total power dissipation have changed.</li> <li>Type number 74HC107DB (SOT337-1/SSOP14) removed.</li> </ul>			
74HC_HCT107 v.5	20151130	Product data sheet	-	74HC_HCT107 v.4
Modifications:	<ul style="list-style-type: none"> <li>Type numbers 74HC107N and 74HCT107N (SOT27-1) removed.</li> </ul>			
74HC_HCT107 v.4	20150126	Product data sheet	-	74HC_HCT107 v.3
Modifications:	<ul style="list-style-type: none"> <li>Table 7: Power dissipation capacitance condition for 74HCT107 is corrected.</li> </ul>			
74HC_HCT107 v.3	20131118	Product data sheet	-	74HC_HCT107_CNV v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74HC_HCT107_CNV v.2	19901201	Product specification	-	-

## Dual JK flip-flop with reset; negative-edge trigger

## 14. Legal information

## Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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## Contents

<b>1. General description</b> .....	<b>1</b>
<b>2. Features and benefits</b> .....	<b>1</b>
<b>3. Ordering information</b> .....	<b>1</b>
<b>4. Functional diagram</b> .....	<b>2</b>
<b>5. Pinning information</b> .....	<b>3</b>
5.1. Pinning.....	3
5.2. Pin description.....	3
<b>6. Functional description</b> .....	<b>3</b>
<b>7. Limiting values</b> .....	<b>4</b>
<b>8. Recommended operating conditions</b> .....	<b>4</b>
<b>9. Static characteristics</b> .....	<b>5</b>
<b>10. Dynamic characteristics</b> .....	<b>6</b>
10.1. Waveforms and test circuit.....	9
<b>11. Package outline</b> .....	<b>11</b>
<b>12. Abbreviations</b> .....	<b>13</b>
<b>13. Revision history</b> .....	<b>13</b>
<b>14. Legal information</b> .....	<b>14</b>

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