

# 74ABT244

Octal buffer/line driver; 3-state

Rev. 3 — 6 October 2017

Product data sheet

## 1 General description

The 74ABT244 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT244 device is an octal buffer that is ideal for driving bus lines. The device features two output enables ( $1\overline{OE}$  and  $2\overline{OE}$ ), each controlling four of the 3-state outputs.

## 2 Features and benefits

- Octal bus interface
- 3-State buffers
- Output capability: +64 mA/–32 mA
- Power-up 3-State
- Live insertion capability
- Inputs are disabled during 3-state mode
- Latch-up protection exceeds 500 mA per JESD78 class II level A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C

## 3 Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ABT244D	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74ABT244DB	-40 °C to +85 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74ABT244PW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4 Functional diagram

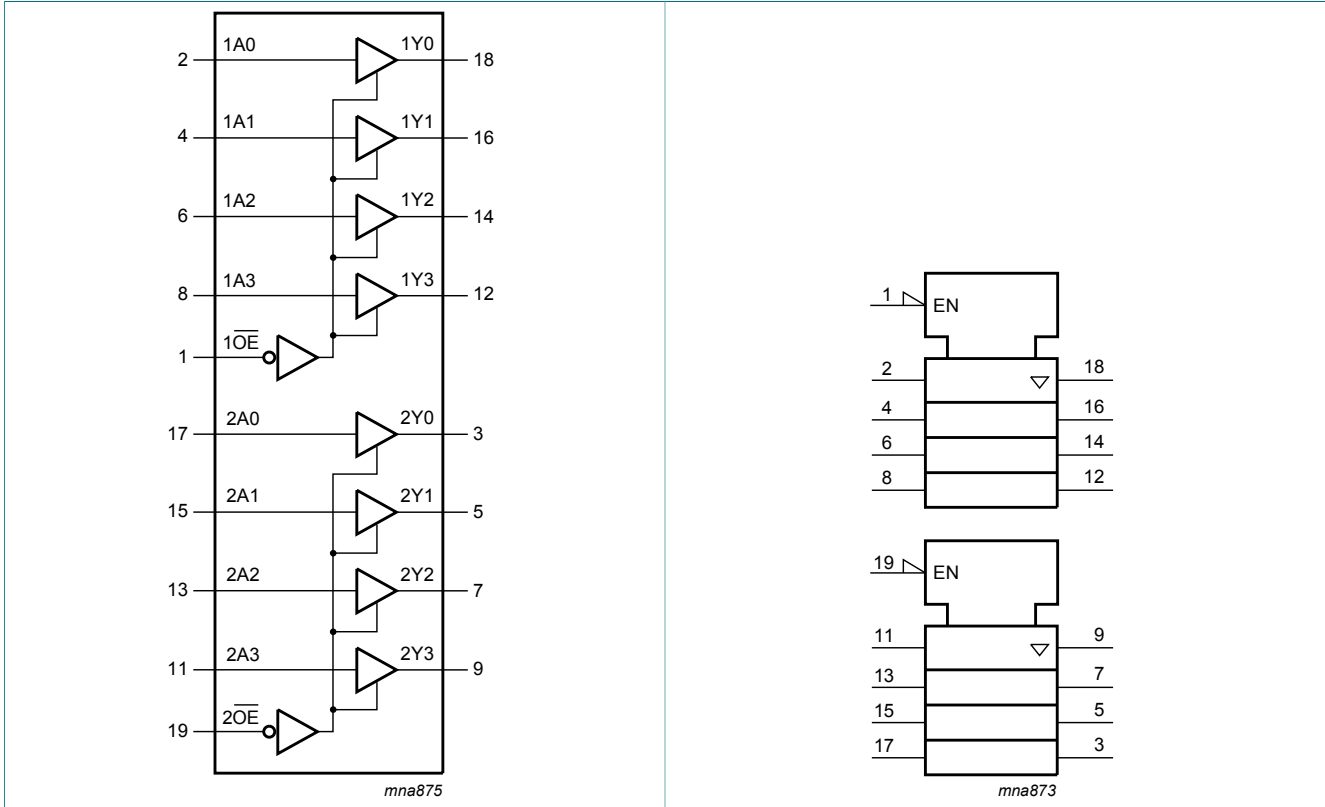


Figure 1. Logic symbol

Figure 2. IEC logic symbol

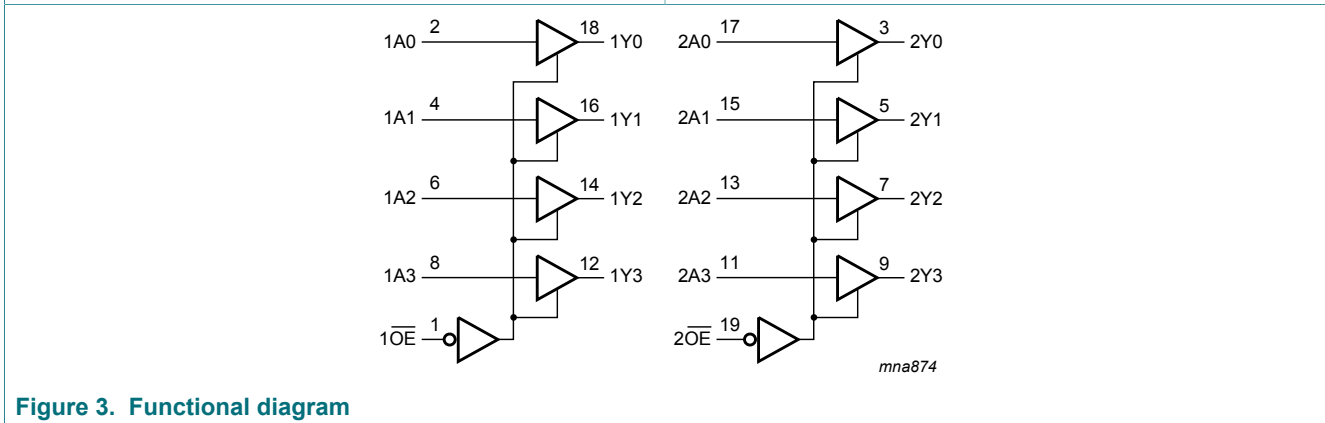


Figure 3. Functional diagram

## 5 Pinning information

### 5.1 Pinning

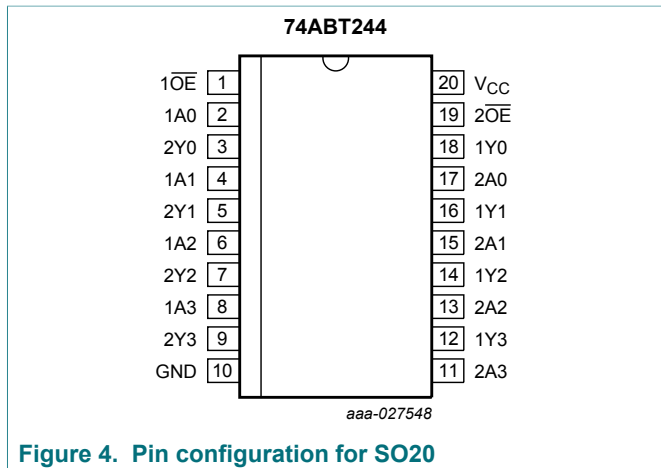


Figure 4. Pin configuration for SO20

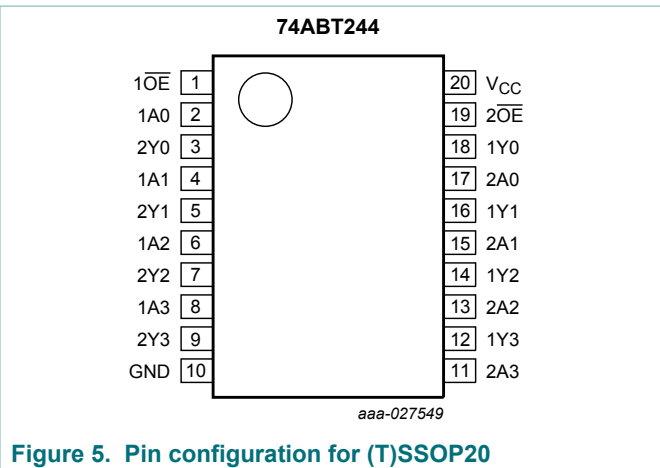


Figure 5. Pin configuration for (T)SSOP20

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A0, 1A1, 1A2, 1A3	2, 4, 6, 8	data input
1Y0, 1Y1, 1Y2, 1Y3	18, 16, 14, 12	data output
2A0, 2A1, 2A2, 2A3	17, 15, 13, 11	data input
2Y0, 2Y1, 2Y2, 2Y3	3, 5, 7, 9	data output
1OE, 2OE	1, 19	output enable input (active LOW)
GND	10	ground (0 V)
V <sub>CC</sub>	20	supply voltage

## 6 Functional description

Table 3. Function table <sup>[1]</sup>

Input		Output
nOE	nAn	nYn
L	L	L
L	H	H
H	X	Z

[1] H = HIGH voltage level;  
 L = LOW voltage level;  
 X = don't care;  
 Z = high-impedance OFF-state.

## 7 Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		[1] -1.2	+7.0	V
$V_O$	output voltage	output in OFF-state or HIGH-state	[1] -0.5	+5.5	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-18	-	mA
$I_{OK}$	output clamping current	$V_O < 0$ V	-50	-	mA
$I_O$	output current	output in LOW-state	-	128	mA
$T_j$	junction temperature		[2] -	150	°C
$T_{stg}$	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

## 8 Recommended operating conditions

**Table 5. Operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		4.5	-	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$I_{OH}$	HIGH-level output current		-32	-	-	mA
$I_{OL}$	LOW-level output current		-	-	64	mA
$\Delta t/\Delta V$	input transition rise and fall rate		0	-	5	ns/V
$T_{amb}$	ambient temperature	in free air	-40	-	+85	°C

## 9 Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T <sub>amb</sub> = 25 °C			T <sub>amb</sub> = -45 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
V <sub>IK</sub>	input clamping voltage	V <sub>CC</sub> = 4.5 V; I <sub>IK</sub> = -18 mA	-1.2	-0.9	-	-1.2	-	V
V <sub>IH</sub>	HIGH-level input voltage		2.0	-	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage		-	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>						
		I <sub>OH</sub> = -3 mA	2.5	2.9	-	2.5	-	V
		I <sub>OH</sub> = -32 mA	2.0	2.4	-	2.0	-	V
		V <sub>CC</sub> = 5.0 V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>						
		I <sub>OH</sub> = -3 mA	3.0	3.4	-	3.0	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub> ; I <sub>OL</sub> = 64 mA	-	0.42	0.55	-	0.55	V
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or 5.5 V	-	±0.01	±1.0	-	±1.0	μA
I <sub>OFF</sub>	power-off leakage current	V <sub>CC</sub> = 0 V; V <sub>O</sub> or V <sub>I</sub> ≤ 4.5 V	-	±5.0	±100	-	±100	μA
I <sub>O(pu/pd)</sub>	power-up/ power-down output current	V <sub>CC</sub> = 2.0 V; V <sub>O</sub> = 0.5 V; V <sub>I</sub> = GND or V <sub>CC</sub> ; n <sub>OE</sub> = don't care <sup>[1]</sup>	-	±5.0	±50	-	±50	μA
I <sub>OZ</sub>	OFF-state output current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>						
		output HIGH-state at V <sub>O</sub> = 2.7 V	-	5.0	50	-	50	μA
		output LOW-state at V <sub>O</sub> = 0.5 V	-	-5.0	-50	-	-50	μA
I <sub>CEX</sub>	output high leakage current	V <sub>CC</sub> = 5.5 V; V <sub>O</sub> = 5.5 V; V <sub>I</sub> = GND or V <sub>CC</sub>	-	5.0	50	-	50	μA
I <sub>O</sub>	output current	V <sub>CC</sub> = 5.5 V; V <sub>O</sub> = 2.5 V <sup>[2]</sup>	-40	-100	-180	-40	-180	mA
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or V <sub>CC</sub>						
		outputs HIGH-state	-	50	250	-	250	μA
		outputs LOW-state	-	24	30	-	30	mA
		outputs disabled	-	50	250	-	250	μA

Symbol	Parameter	Conditions	T <sub>amb</sub> = 25 °C			T <sub>amb</sub> = -45 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 5.5 V						
		outputs enabled; one data input at 3.4 V and other inputs at V <sub>CC</sub> or GND <sup>[3]</sup>	-	0.5	1.5	-	1.5	mA
		outputs disabled; one data input at 3.4 V and other inputs at V <sub>CC</sub> or GND <sup>[3]</sup>	-	50	250	-	250	μA
		outputs disabled; one enable input at 3.4 V and other inputs at V <sub>CC</sub> or GND <sup>[3]</sup>	-	0.5	1.5	-	1.5	mA
C <sub>I</sub>	input capacitance	V <sub>I</sub> = 0 V or V <sub>CC</sub>	-	4	-	-	-	pF
C <sub>O</sub>	output capacitance	outputs disabled; V <sub>O</sub> = 0 V or V <sub>CC</sub>	-	7	-	-	-	pF

[1] This parameter is valid for any V<sub>CC</sub> between 0 V and 2.1 V, with a transition time of up to 10 ms.

From V<sub>CC</sub> = 2.1 V to V<sub>CC</sub> = 5 V ± 10 % a transition time of up to 100 μs is permitted.

[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[3] This is the increase in supply current for each input at 3.4 V.

## 10 Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	T <sub>amb</sub> = 25 °C; V <sub>CC</sub> = 5.0 V			T <sub>amb</sub> = -40 °C to 85 °C; V <sub>CC</sub> = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	LOW to HIGH propagation delay	nAn to nYn; see <a href="#">Figure 6</a>	1.0	2.6	4.1	1.0	4.6	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	nAn to nYn; see <a href="#">Figure 6</a>	1.0	2.9	4.2	1.0	4.6	ns
t <sub>PZH</sub>	OFF-state to HIGH propagation delay	nOE to nYn; see <a href="#">Figure 7</a>	1.1	3.1	4.6	1.1	5.1	ns
t <sub>PZL</sub>	OFF-state to LOW propagation delay	nOE to nYn; see <a href="#">Figure 7</a>	2.1	4.1	5.6	2.1	6.1	ns
t <sub>PHZ</sub>	HIGH to OFF-state propagation delay	nOE to nYn; see <a href="#">Figure 7</a>	2.1	4.1	5.6	2.1	6.6	ns
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	nOE to nYn; see <a href="#">Figure 7</a>	1.7	2.7	5.2	1.7	5.7	ns

10.1 Waveforms and test circuit

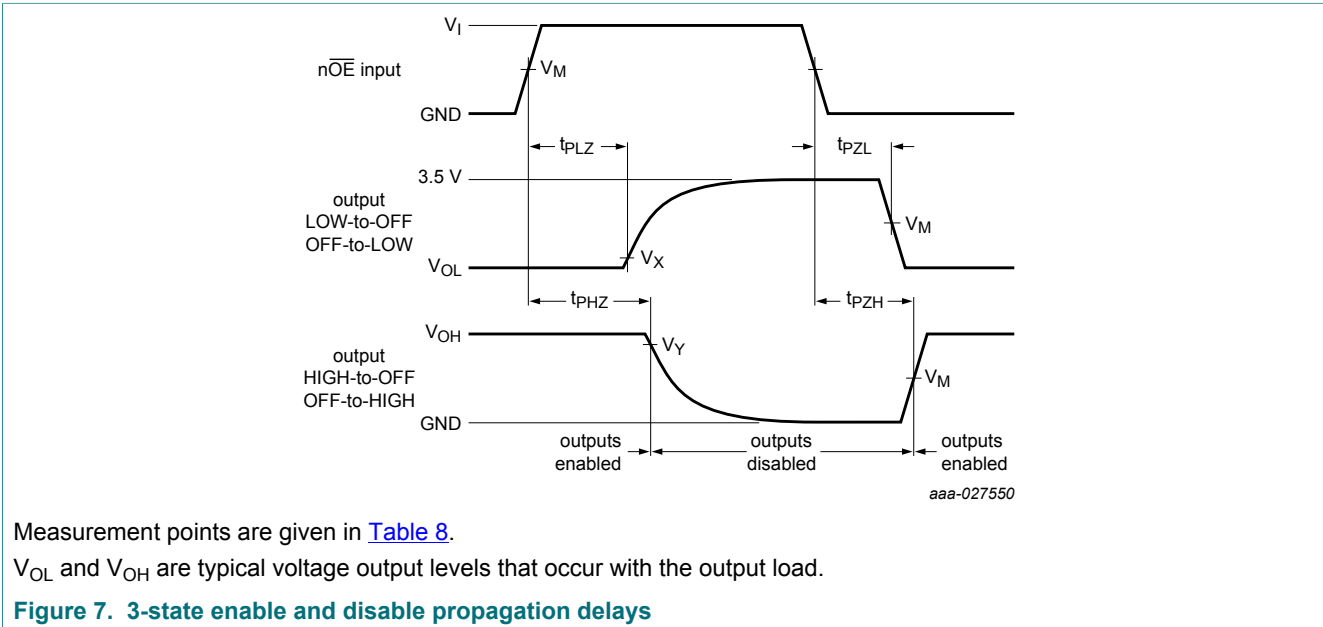
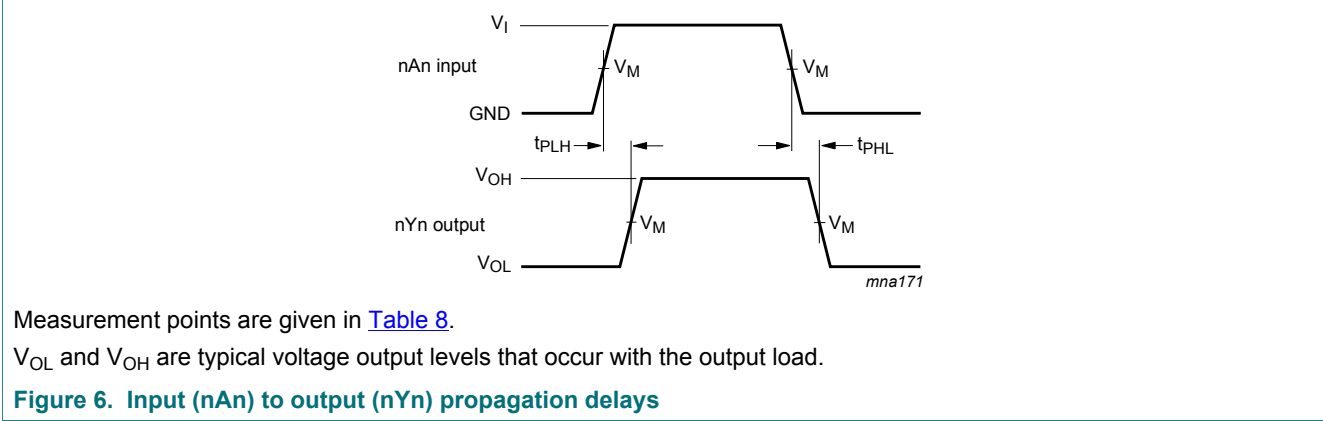
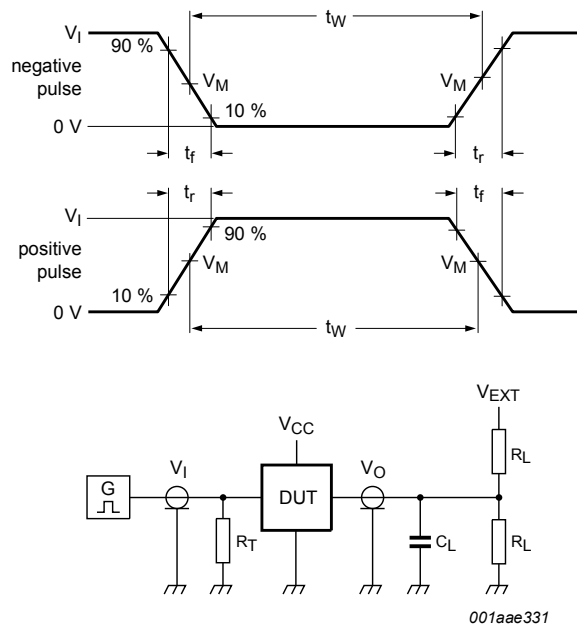


Table 8. Measurement points

Input	Output		
$V_M$	$V_M$	$V_X$	$V_Y$
1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$



Test data is given in [Table 9](#).

Definitions test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = Test voltage for switching times.

**Figure 8. Test circuit for measuring switching times**

**Table 9. Test data**

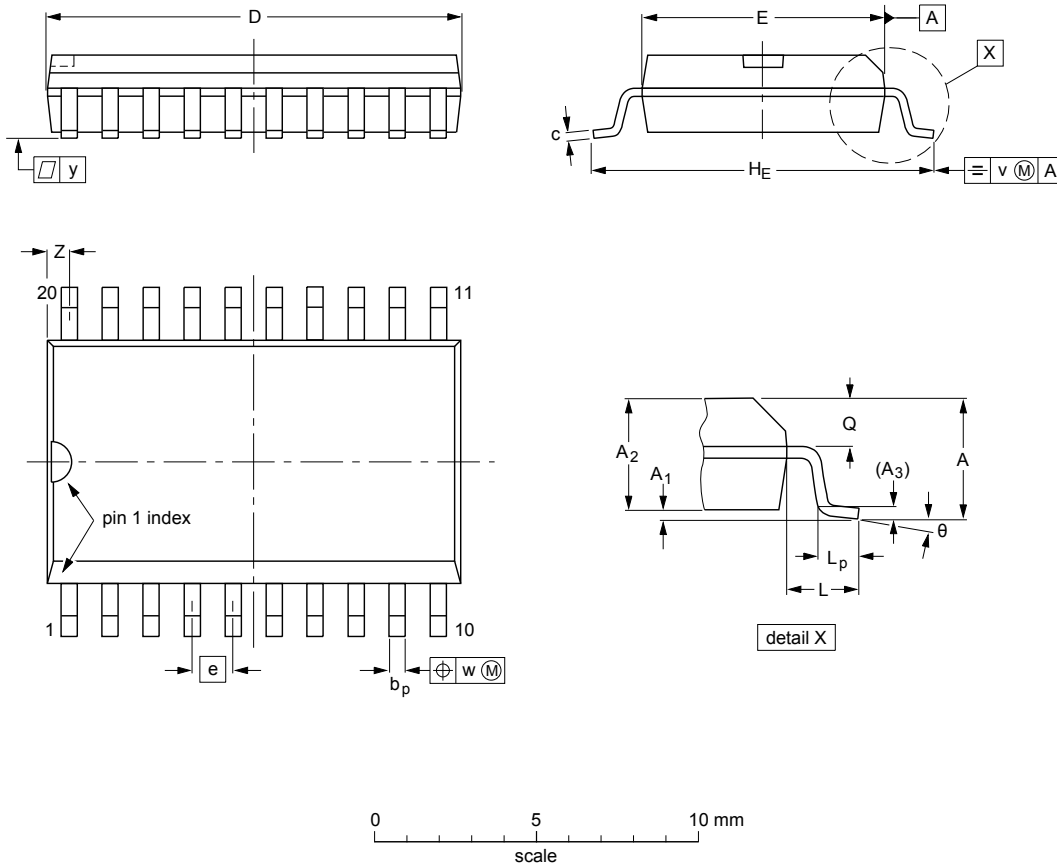
Input				Load		$V_{EXT}$		
$V_I$	$f_i$	$t_W$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHZ}, t_{PZH}$	$t_{PLZ}, t_{PZL}$	$t_{PLH}, t_{PHL}$
3.0 V	$\leq 1$ MHz	500 ns	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	7 V	open



11 Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

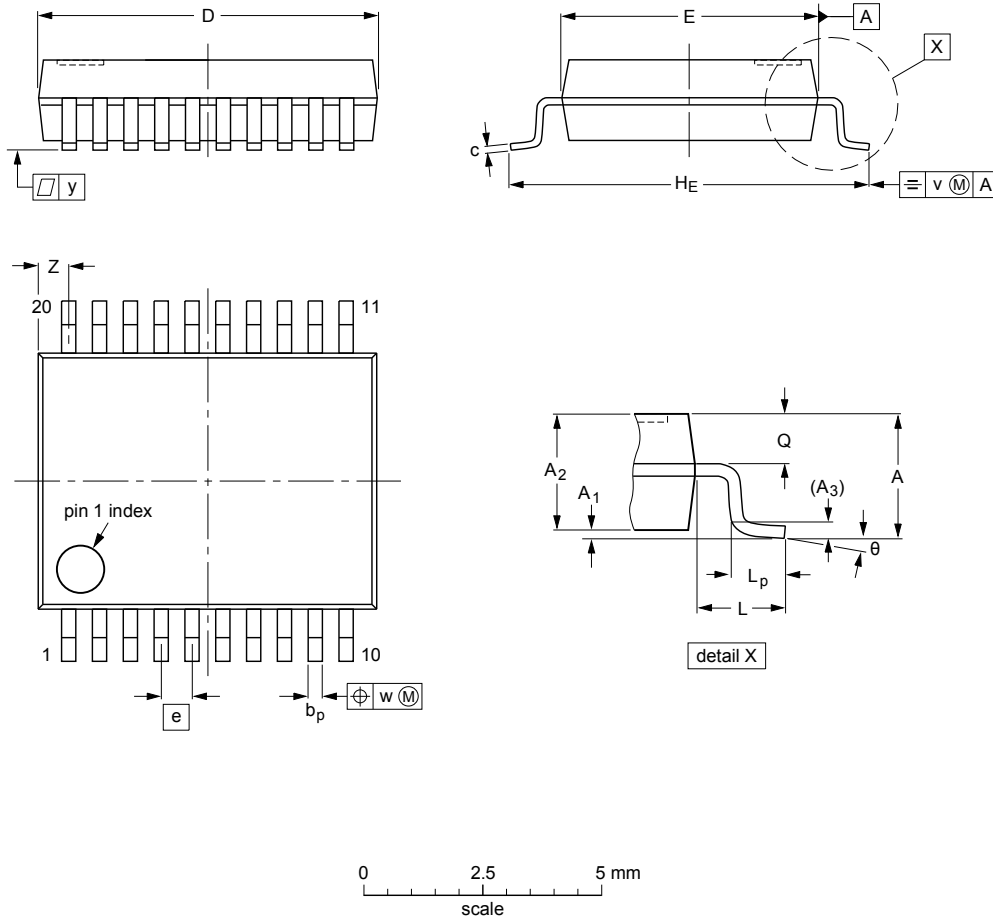
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT163-1	075E04	MS-013			99-12-27 03-02-19

Figure 9. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A <sub>max.</sub>	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

**Note**

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT339-1		MO-150				99-12-27 03-02-19

Figure 10. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

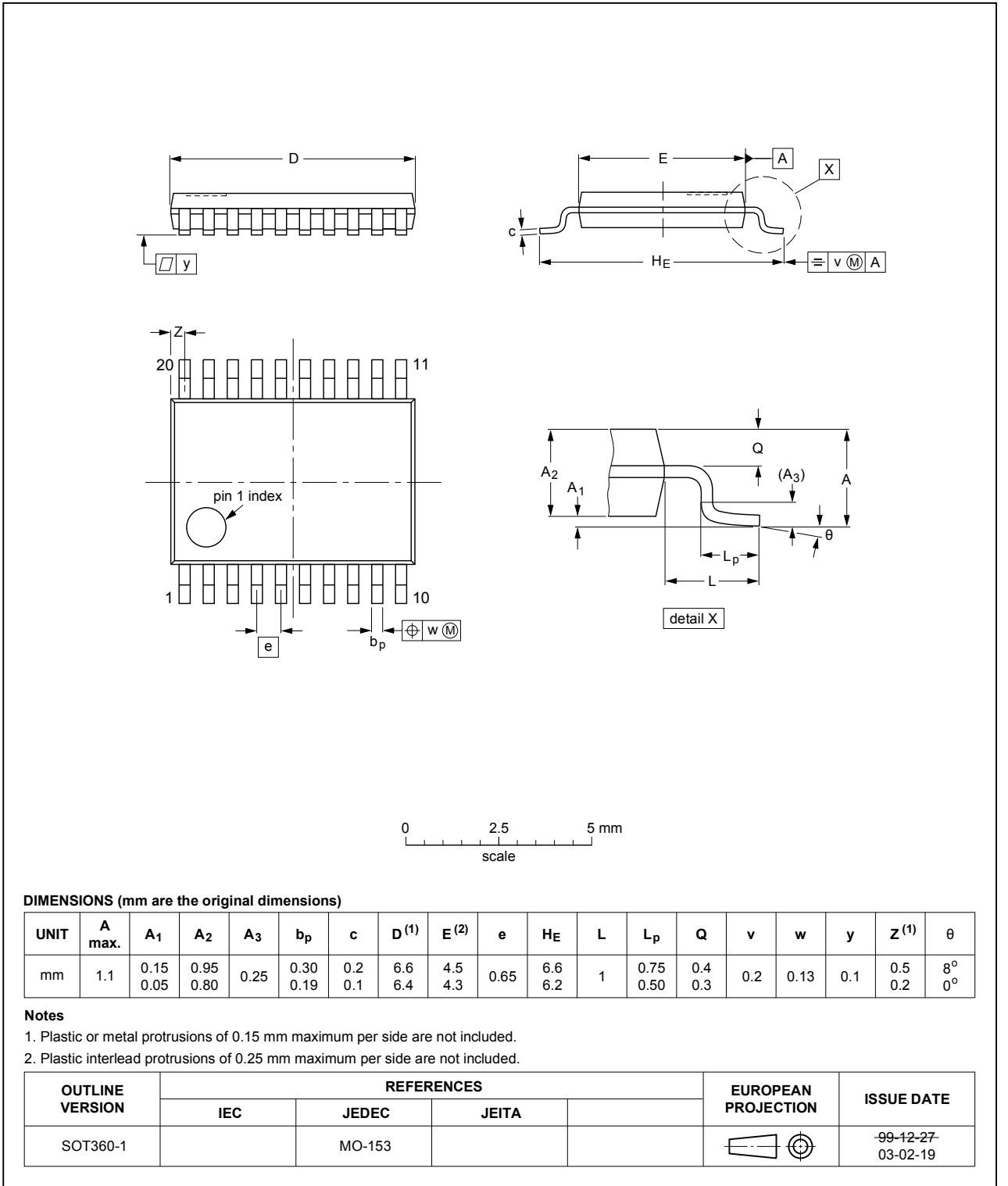


Figure 11. Package outline SOT360-1 (TSSOP20)

## 12 Abbreviations

Table 10. Abbreviations

Acronym	Description
BICMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
MIL	Military
MM	Machine Model

## 13 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT244 v.3	20171006	Product data sheet	-	74ABT244 v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type number 74ABT244N removed from data sheet.</li> </ul>			
74ABT244 v.2	19980116	Product specification	-	74ABT244 v.1
74ABT244 v.1	19950906	Product specification	-	-

## 14 Legal information

### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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