Product data sheet

1. General description

The 74ABT04 is a hex inverter. This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Supply voltage range from 4.5 V to 5.5 V
- BiCMOS high speed and output drive
- · Direct interface with TTL levels
- I_{OFF} circuitry provides partial Power-down mode operation
- · Latch-up protection exceeds 500 mA per JESD78B class II level A
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C

3. Ordering information

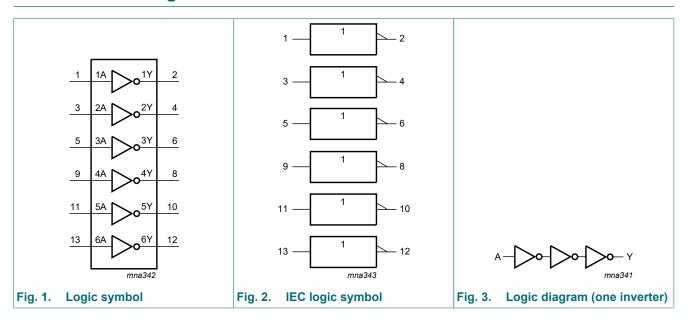
Table 1. Ordering information

Type number	Package									
	Temperature range	Version								
74ABT04D	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1						
74ABT04PW	-40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1						



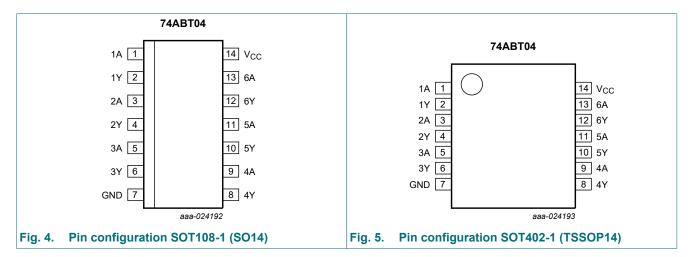
Hex inverter

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
Vcc	14	supply voltage

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6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level

Input	Output
nA	nY
L	Н
Н	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
VI	input voltage	[1]	-1.2	+7.0	V
Vo	output voltage	output HIGH or LOW [1]	-0.5	+5.5	V
I _{IK}	input clamping current	V _I < 0 V	-18	-	mA
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
Io	output current	output in LOW-state	-	40	mA
Tj	junction temperature		-	150	°C
T _{stg}	storage temperature		-65	+150	°C

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 5. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
VI	input voltage		0	-	V _{CC}	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I _{OH}	HIGH-level output current		-15	-	-	mA
I _{OL}	LOW-level output current		-	-	20	mA
Δt/ΔV	input transition rise and fall rate		0	-	5	ns/V
T _{amb}	ambient temperature	in free air	-40	-	+85	°C

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9. Static characteristics

Table 6. Static characteristics

Symbol Parameter		Conditions		25 °C		-40 °C t	Unit	
			Min	Тур	Max	Min	Max	
V _{IK}	input clamping voltage	V _{CC} = 4.5 V; I _{IK} = -18 mA	-1.2	-0.9	-	-1.2	-	V
V _{OH}	HIGH-level output voltage	V_{CC} = 4.5 V; I_{OH} = -15 mA; V_I = V_{IL} or V_{IH}	2.5	2.9	-	2.5	-	V
V _{OL}	LOW-level output voltage	V_{CC} = 4.5 V; I_{OL} = 20 mA; V_{I} = V_{IL} or V_{IH}	-	0.35	0.5	-	0.5	V
l _l	input leakage current	V _{CC} = 5.5 V; V _I = GND or 5.5 V	-	±0.01	±1.0	-	±1.0	μΑ
I _{OFF}	power-off leakage current	$V_{CC} = 0 \text{ V}; V_{I} \text{ or } V_{O} \le 4.5 \text{ V}$	-	±5.0	±100	-	±100	μΑ
I _{CEX}	output high leakage current	HIGH-state; $V_O = 5.5 \text{ V}$; $V_{CC} = 5.5 \text{ V}$; $V_I = \text{GND or } V_{CC}$	-	5.0	50	-	50	μΑ
Io	output current	$V_{CC} = 5.5 \text{ V}; V_{O} = 2.5 \text{ V}$ [1] -50	-75	-180	-50	-180	mA
I _{CC}	supply current	V_{CC} = 5.5 V; V_I = GND or V_{CC}	-	2	50	-	50	μΑ
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 5.5 V; one input at 3.4 V; other inputs at V _{CC} or GND	2] -	0.25	500	-	500	μА
Cı	input capacitance	V _I = 0 V or V _{CC}	-	3	-	-	-	pF

^[1] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; for test circuit, see Fig. 7.

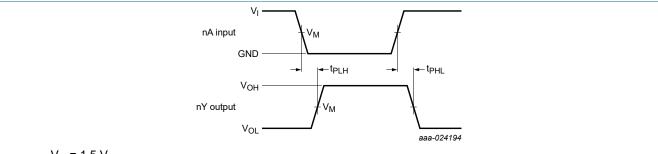
Symbol	Parameter	Conditions	25 °C; V _{CC} = 5.0 V			-40 °C to V _{CC} = 5.0	Unit	
			Min	Тур	Max	Min	Max	
t _{PLH}	LOW to HIGH propagation delay	nA to nY; see Fig. 6	1.0	2.2	3.4	1.0	4.1	ns
t _{PHL}	HIGH to LOW propagation delay	nA to nY; see Fig. 6	1.0	1.6	2.5	1.0	3.0	ns
t _{sk(o)}	output skew time	[1]	-	0.4	0.5	-	0.5	ns

^[1] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

^[2] This is the increase in supply current for each input at 3.4 V.

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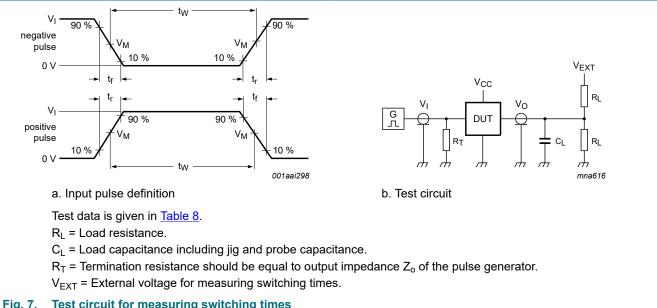
10.1. Waveforms and test circuit



 $V_{M} = 1.5 V$

 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Propagation delay input (nA) to output (nY) and output skew time



Test circuit for measuring switching times Fig. 7.

Table 8. Test data

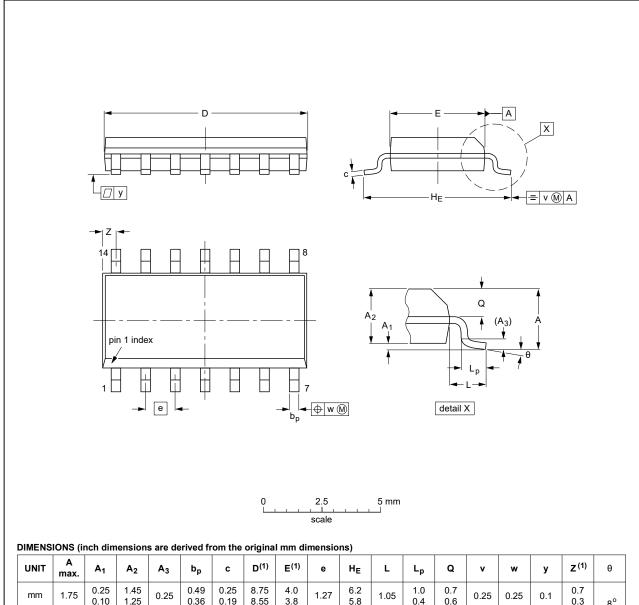
Input				Load	V _{EXT}	
V _I	f _i	t _W	t _r , t _f	CL	R_L	t _{PHL} , t _{PLH}
3.0 V	1 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	open

Hex inverter

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	0°

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE	
SOT108-1	076E06	MS-012			99-12-27 03-02-19	

Fig. 8. Package outline SOT108-1 (SO14)

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

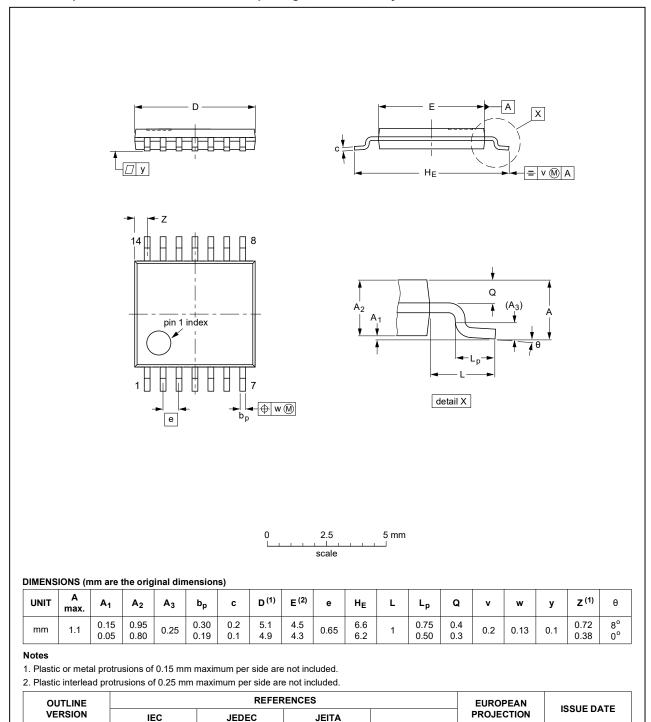


Fig. 9. Package outline SOT402-1 (TSSOP14)

MO-153

99-12-27

03-02-18

SOT402-1

Hex inverter

12. Abbreviations

Table 9. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes				
74ABT04 v.4	20201006	Product data sheet	-	74ABT04 v.3				
Modifications:	guidelines of Legal texts Section 1 a	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 1 and Section 2 updated. Type number 74ABT04DB (SOT337-1 / SSOP14) removed. 						
74ABT04 v.3	20160812	Product data sheet	-	74ABT04 v.2				
Modifications:	guidelines o	 The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. 						
74ABT04 v.2	19950918	Product specification	-	-				

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14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
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74ABT04

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