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Thank you for your cooperation and understanding,

Ampleon

UHF power LDMOS transistor

BLF1046

FEATURES

- High power gain
- Easy power control
- Excellent ruggedness
- Source on underside eliminates DC isolators, reducing common mode inductance
- Designed for broadband operation (HF to 1 GHz).

APPLICATIONS

- Communication transmitter applications in the UHF frequency range.

DESCRIPTION

Silicon N-channel enhancement mode lateral D-MOS transistor encapsulated in a 2-lead flange package (SOT467C) with a ceramic cap. The common source is connected to the mounting flange.

PINNING - SOT467C

PIN	DESCRIPTION
1	drain
2	gate
3	source, connected to flange

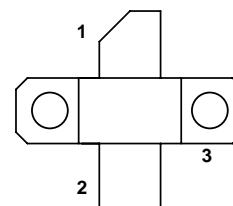


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at $T_h = 25^\circ\text{C}$ in the common source broadband test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
CW, class-AB (2-tone)	$f_1 = 960; f_2 = 960.1$	26	45 (PEP)	>14	>35	≤ -26
CW, class-AB (1-tone)	960	26	45	>14	>46	—

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage	—	65	V
V_{GS}	gate-source voltage	—	± 20	V
I_D	drain current (DC)	—	4.5	A
T_{stg}	storage temperature	−65	+150	$^\circ\text{C}$
T_j	junction temperature	—	200	$^\circ\text{C}$

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-h}$	thermal resistance from junction to heatsink	$T_h = 25\ ^\circ\text{C}$; $P_{dis} = 97\ \text{W}$; note 1	1.87	K/W

Note

1. Determined under specified RF operating conditions, based on maximum peak junction temperature.

CHARACTERISTICS

$T_j = 25\ ^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = 0.7\ \text{mA}$	65	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = 10\ \text{V}$; $I_D = 70\ \text{mA}$	4	–	5	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0$; $V_{DS} = 26\ \text{V}$	–	–	1	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GSth} + 9\ \text{V}$; $V_{DS} = 10\ \text{V}$	12.5	–	–	A
I_{GSS}	gate leakage current	$V_{GS} = \pm 20\ \text{V}$; $V_{DS} = 0$	–	–	125	nA
g_{fs}	forward transconductance	$V_{DS} = 10\ \text{V}$; $I_D = 3.5\ \text{A}$	–	2	–	S
R_{DSon}	drain-source on-state resistance	$V_{GS} = V_{GSth} + 9\ \text{V}$; $I_D = 3.5\ \text{A}$	–	300	–	$\text{m}\Omega$
C_{is}	input capacitance	$V_{GS} = 0$; $V_{DS} = 26\ \text{V}$; $f = 1\ \text{MHz}$	–	46	–	pF
C_{os}	output capacitance	$V_{GS} = 0$; $V_{DS} = 26\ \text{V}$; $f = 1\ \text{MHz}$	–	37	–	pF
C_{rs}	feedback capacitance	$V_{GS} = 0$; $V_{DS} = 26\ \text{V}$; $f = 1\ \text{MHz}$	–	1.5	–	pF

APPLICATION INFORMATION

RF performance in the common source class-AB broadband test circuit. $T_h = 25\ ^\circ\text{C}$; $R_{th\ j-h} = 1.87\ \text{K/W}$, unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
CW, class-AB (2-tone)	$f_1 = 960$; $f_2 = 960.1$	26	300	45 (PEP)	>14	>35	≤ -26
CW, class-AB (1-tone)	960	26	300	45	>14	>46	–

Ruggedness in class-AB operation

The BLF1046 is capable of withstanding a load mismatch corresponding to $V_{SWR} = 10 : 1$ through all phases under the following conditions: $V_{DS} = 26\ \text{V}$; $f = 960\ \text{MHz}$ at rated load power.

Tuning Procedure

For high gain and efficiency:

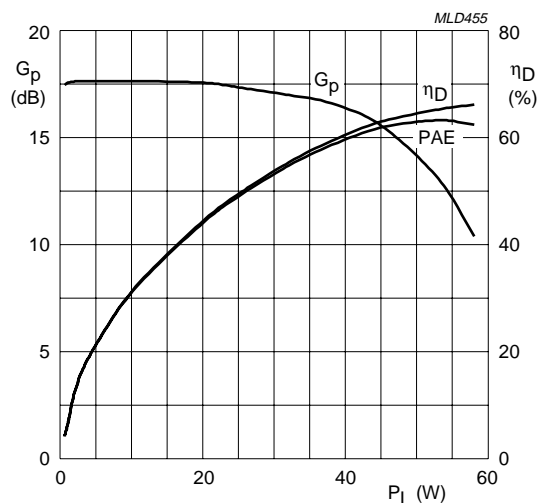
In CW mode ($P_D = 1\ \text{W}$; $f = 960\ \text{MHz}$) tune C2 and C16 (see Figs. 13 and 14) until $IRL < -15\ \text{dB}$, then adjust C6 and C8 for high gain until $G_p > 14\ \text{dB}$ at $P_L = 50\ \text{W}$.

For linear mode:

Tune for high gain and efficiency mode, then apply two tone signal ($f_1 = 960\ \text{MHz}$; $f_2 = 960.1\ \text{MHz}$) at $P_L = 45\ \text{W}$ (PEP) and tune first C2 and then C6 and C8 for lowest d_3 (below $-28\ \text{dBc}$).

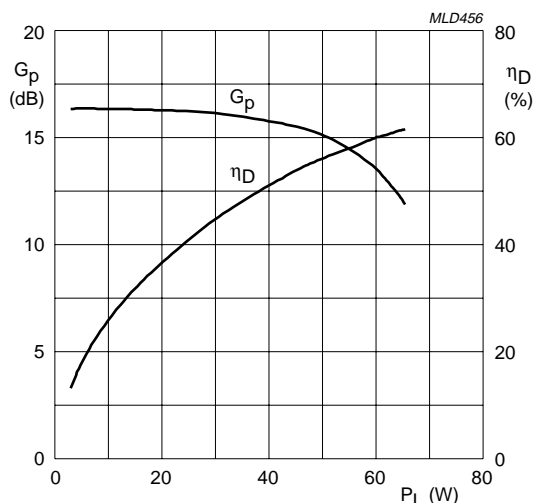
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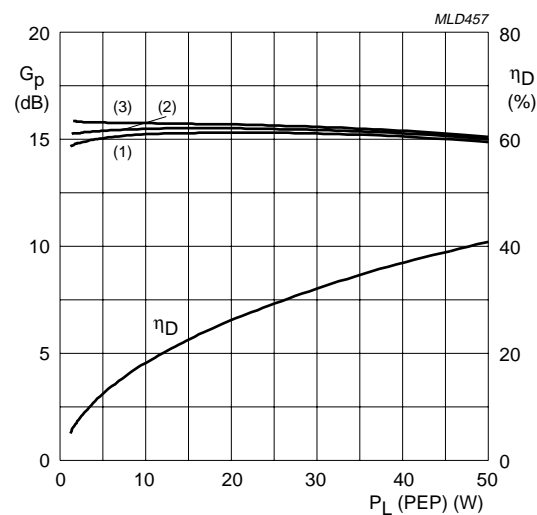
$V_{DS} = 26 \text{ V}$; $I_{DQ} = 330 \text{ mA}$; $T_h \leq 25^\circ\text{C}$; $f = 960 \text{ MHz}$;
tuned for high efficiency; see tuning procedure.

Fig.2 Power gain and drain efficiency as functions of load power; typical values.



$V_{DS} = 26 \text{ V}$; $I_{DQ} = 330 \text{ mA}$; $T_h \leq 25^\circ\text{C}$; $f = 960 \text{ MHz}$;
tuned for high linearity; see tuning procedure

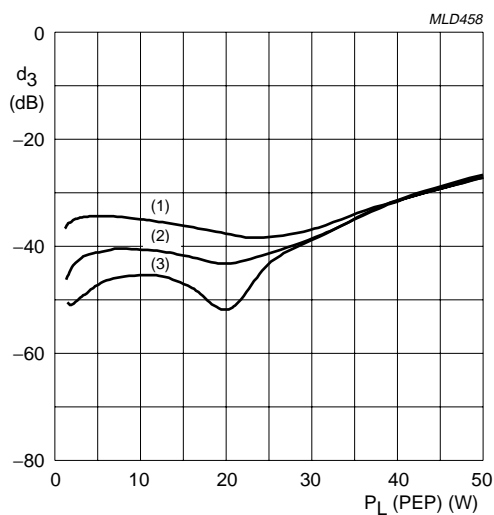
Fig.3 Power gain and drain efficiency as functions of load power; typical values.



$V_{DS} = 26 \text{ V}$; $T_h \leq 25^\circ\text{C}$; $f_1 = 960 \text{ MHz}$; $f_2 = 960.1 \text{ MHz}$;
tuned for high linearity; see tuning procedure.

- (1) $I_{DQ} = 240 \text{ mA}$.
- (2) $I_{DQ} = 300 \text{ mA}$.
- (3) $I_{DQ} = 400 \text{ mA}$.

Fig.4 Power gain and drain efficiency as functions of peak envelope power; typical values.



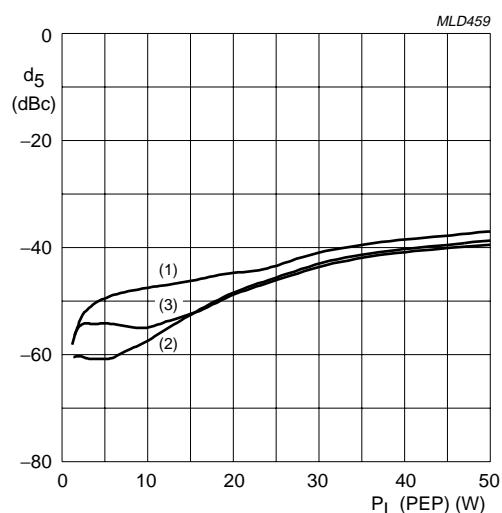
$V_{DS} = 26 \text{ V}$; $T_h \leq 25^\circ\text{C}$; $f_1 = 960 \text{ MHz}$; $f_2 = 960.1 \text{ MHz}$;
tuned for high linearity; see tuning procedure.

- (1) $I_{DQ} = 240 \text{ mA}$.
- (2) $I_{DQ} = 300 \text{ mA}$.
- (3) $I_{DQ} = 400 \text{ mA}$.

Fig.5 Third order intermodulation distortion as a function of peak envelope load power; typical values.

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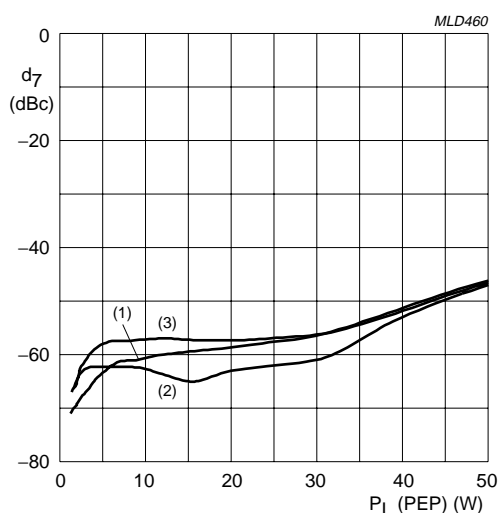
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$V_{DS} = 26\text{ V}$; $T_h \leq 25\text{ }^\circ\text{C}$; $f_1 = 960\text{ MHz}$; $f_2 = 960.1\text{ MHz}$; tuned for high linearity; see tuning procedure.

- (1) $I_{DQ} = 240\text{ mA}$.
- (2) $I_{DQ} = 300\text{ mA}$.
- (3) $I_{DQ} = 400\text{ mA}$.

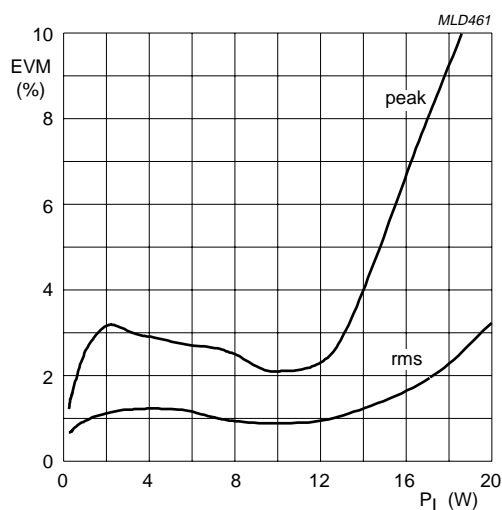
Fig.6 Fifth order intermodulation distortion as a function of peak envelope load power; typical values.



$V_{DS} = 26\text{ V}$; $T_h \leq 25\text{ }^\circ\text{C}$; $f_1 = 960\text{ MHz}$; $f_2 = 960.1\text{ MHz}$; tuned for high linearity; see tuning procedure.

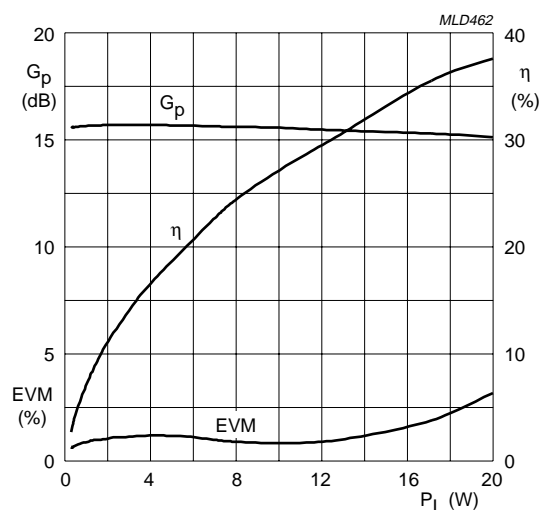
- (1) $I_{DQ} = 240\text{ mA}$.
- (2) $I_{DQ} = 300\text{ mA}$.
- (3) $I_{DQ} = 400\text{ mA}$.

Fig.7 Seventh order intermodulation distortion as a function of peak envelope load power; typical values.



$V_{DS} = 26\text{ V}$; $I_{DQ} = 300\text{ mA}$; $T_h \leq 25\text{ }^\circ\text{C}$; $f = 960\text{ MHz}$; tuned for high linearity; see tuning procedure.

Fig.8 Error vector magnitude (EVM) / EDGE 8PSK as a functions of load power; typical values.

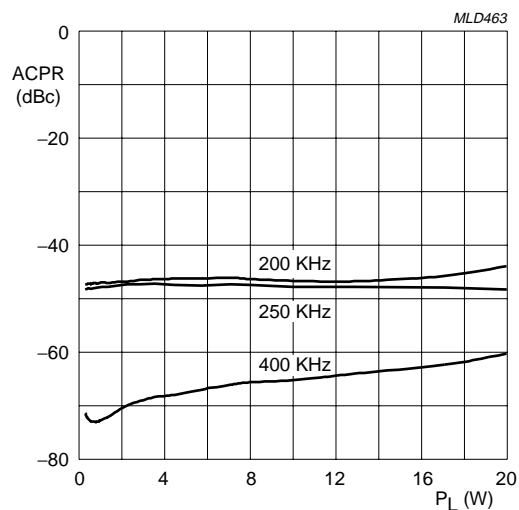


$V_{DS} = 26\text{ V}$; $I_{DQ} = 300\text{ mA}$; $T_h \leq 25\text{ }^\circ\text{C}$; $f = 960\text{ MHz}$; tuned for high linearity; see tuning procedure.

Fig.9 EDGE 8PSK EVM, gain and efficiency as functions of load power; typical values.

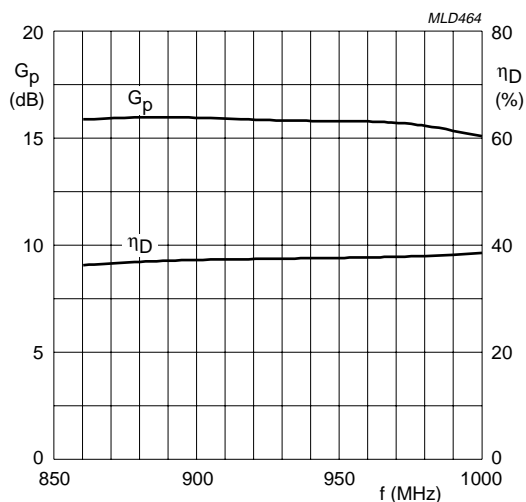
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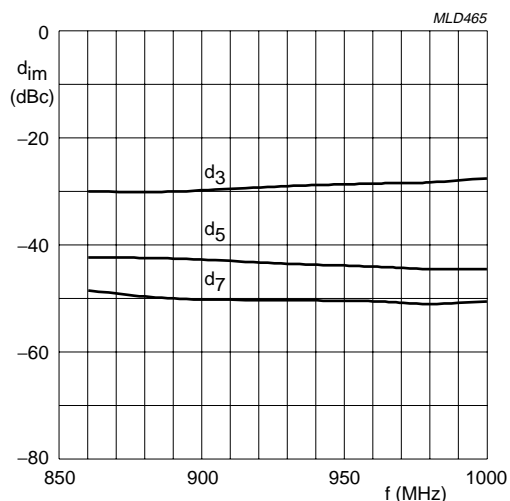
$V_{DS} = 26$ V; $I_{DQ} = 300$ mA; $T_h \leq 25$ °C; $f = 960$ MHz; tuned for high linearity; see tuning procedure.
Measured EDGE channel bandwidth 270 kHz and adjacent channels bandwidth 30 kHz.

Fig.10 EDGE 8PSK adjacent channel power as a function of load power; typical values.



$V_{DS} = 28$ V; $I_{DQ} = 300$ mA; $P_L = 45$ W (PEP); $T_h \leq 25$ °C; tuned for high linearity; see tuning procedure.
Measured in broadband test circuit; see Figs. 15 and 16.

Fig.11 Power gain and drain efficiency as functions of frequency; typical values.

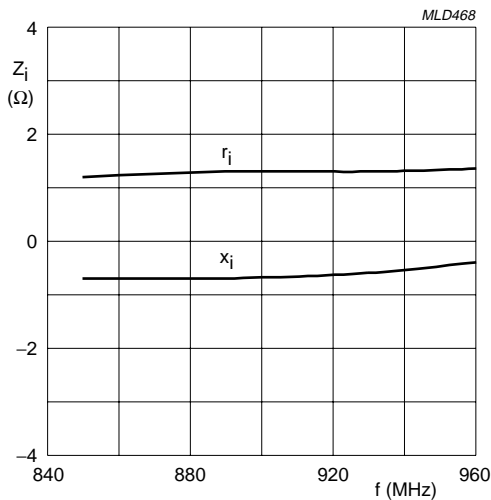


$V_{DS} = 28$ V; $I_{DQ} = 300$ mA; $P_L = 45$ W (PEP); $T_h \leq 25$ °C; tuned for high linearity; see tuning procedure.
Measured in broadband test circuit; see Figs. 15 and 16.

Fig.12 Intermodulation distortion as a function of frequency; typical values.

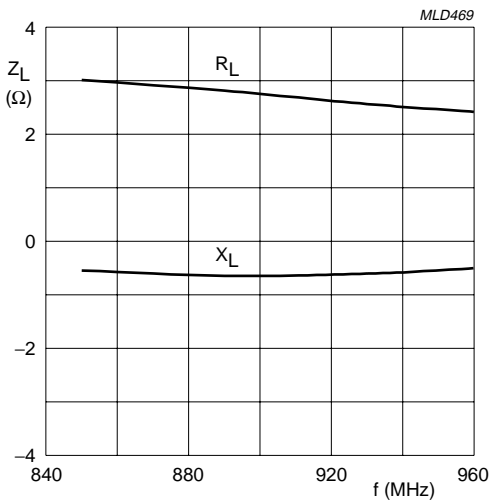
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$V_{DS} = 26\text{ V}$; $I_{DQ} = 300\text{ mA}$; $P_L = 45\text{ W}$; $T_h \leq 25\text{ }^\circ\text{C}$;
tuned for high linearity; see tuning procedure.

Fig.13 Optimal source impedance as a function of frequency (series components); typical values.

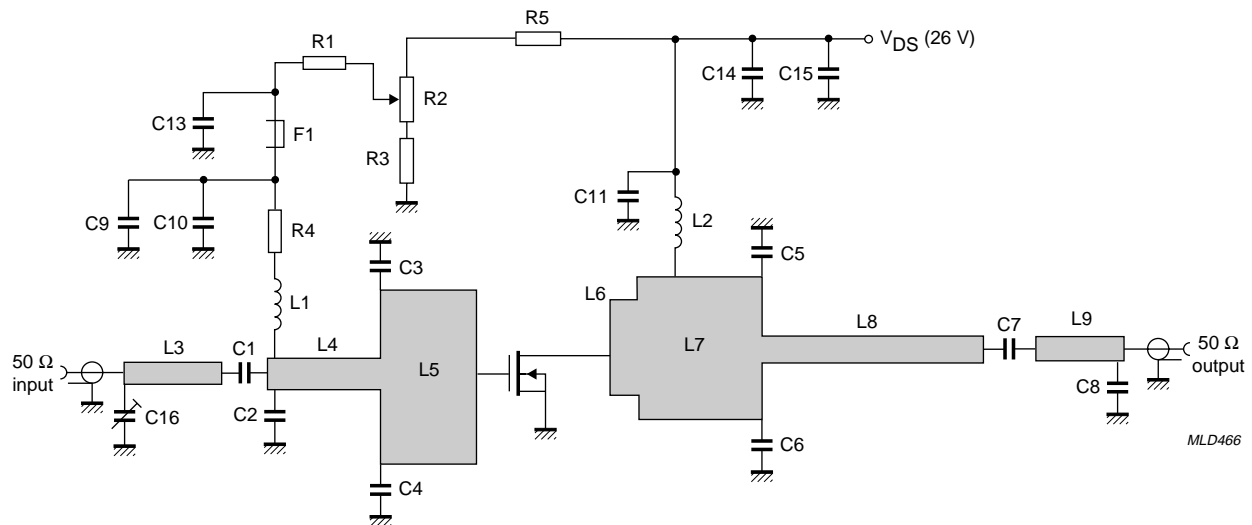
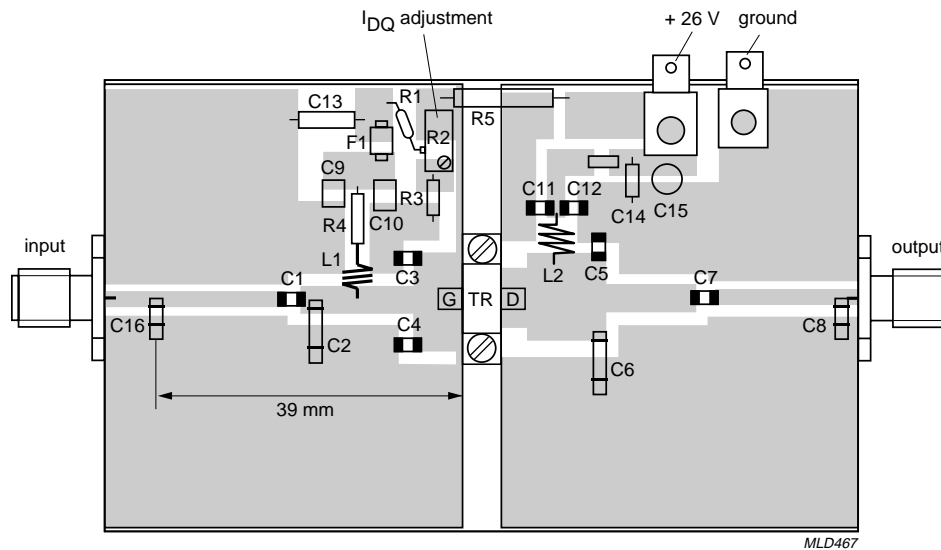


$V_{DS} = 26\text{ V}$; $I_{DQ} = 300\text{ mA}$; $P_L = 45\text{ W}$; $T_h \leq 25\text{ }^\circ\text{C}$;
tuned for high linearity; see tuning procedure.

Fig.14 Optimal load impedance as a function of frequency (series components); typical values.

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Fig.15 Class-AB broadband test circuit at $f = 800$ to 1000 MHz.

Dimensions in mm.

The components are situated on one side of the copper-clad printed-circuit board with Teflon dielectric ($\epsilon_r = 2.2$), thickness 0.79 mm. The other side is unetched and serves as a ground plane.

Fig.16 Component layout for 800 to 1000 MHz class-AB broadband test circuit.

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List of components (see Figs 15 and 16)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C7	multilayer ceramic chip capacitor; note 1	33 pF		
C2, C6	Tekelec variable capacitor	0.8 to 8.2 pF		
C3, C4	multilayer ceramic chip capacitor; note 1	13 pF		
C5	multilayer ceramic chip capacitor; note 1	7.5 pF		
C8, C16	Tekelec variable capacitor	0.5 to 4.6 pF		
C9, C11	multilayer ceramic chip capacitor; note 1	33 pF		
C10, C12	multilayer ceramic chip capacitor; note 1	150 pF		
C13, C14	multilayer ceramic chip capacitor	33 nF		
C15	electrolytic capacitor	47 μ F; 63 V		
F1	Ferroxcube chip-bead 8DS3/3/8/9-4S2			4330 030 36301
L1	5 turns enamelled 0.6 mm copper wire		int. dia. = 4 mm; length = 5 mm	
L2	2 turns enamelled 0.6 mm copper wire		int. dia. = 4 mm; length = 1.6 mm	
L3	stripline; note 2	50 Ω	16 \times 2.36 mm	
L4	stripline; note 2	42.5 Ω	16 \times 3.1 mm	
L5	stripline; note 2	14.3 Ω	6 \times 12 mm	
L6	stripline; note 2	20.2 Ω	3 \times 8 mm	
L7	stripline; note 2	14.3 Ω	14 \times 12 mm	
L8	stripline; note 2	40 Ω	17 \times 3.4 mm	
L9	stripline; note 2	50 Ω	7 \times 2.36 mm	
R1, R5	metal film resistor	10 k Ω , 0.6 W		
R2	variable resistor	10 k Ω		
R3	metal film resistor	1 k Ω , 0.6 W		
R4	metal film resistor	10 Ω , 0.6 W		

Notes

1. American Technical Ceramics type 100B or capacitor of same quality.
2. The striplines are on a double copper-clad printed-circuit board with Teflon dielectric ($\epsilon_r = 2.2$); thickness 0.79 mm.

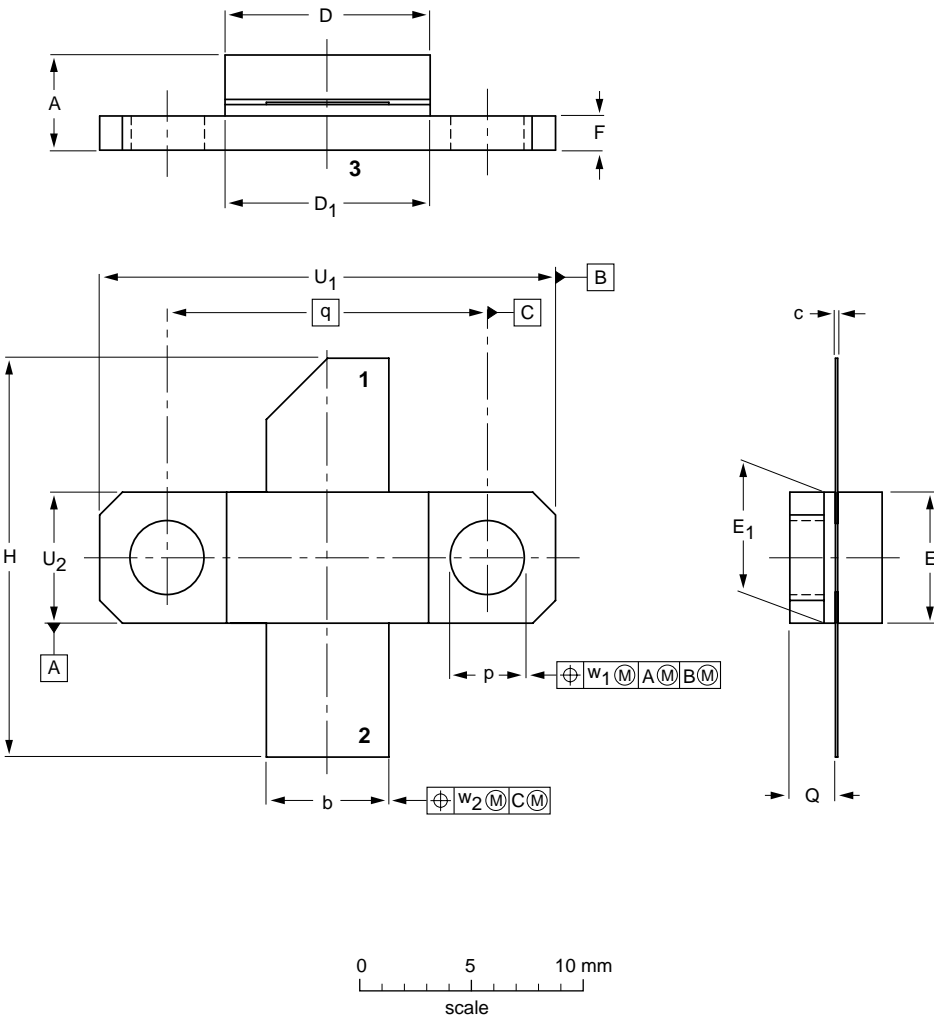
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PACKAGE OUTLINE

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads

SOT467C



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D ₁	E	E ₁	F	H	p	Q	q	U ₁	U ₂	w ₁	w ₂
mm	4.67 3.94	5.59 5.33	0.15 0.10	9.25 9.04	9.27 9.02	5.92 5.77	5.97 5.72	1.65 1.40	18.54 17.02	3.43 3.18	2.21 1.96	14.27	20.45 20.19	5.97 5.72	0.25	0.51
inch	0.184 0.155	0.220 0.210	0.006 0.004	0.364 0.356	0.365 0.355	0.233 0.227	0.235 0.225	0.065 0.055	0.73 0.67	0.135 0.125	0.087 0.077	0.562	0.805 0.795	0.235 0.225	0.010	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT467C						99-12-06 99-12-28

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DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS ⁽¹⁾
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device.

These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 3 Figtree Drive, HOMEBUSH, NSW 2140,
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoprojekt, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),
Tel. +39 039 203 6838, Fax +39 039 203 6800

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Al. Jerozolimskie 195 B, 02-222 WARSAW,
Tel. +48 22 5710 000, Fax. +48 22 5710 001

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,
Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 5F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2451, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
60/14 MOO 11, Bangna Trad Road KM. 3, Bangna, BANGKOK 10260,
Tel. +66 2 361 7910, Fax. +66 2 398 3447

Turkey: Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 3341 299, Fax. +381 11 3342 553

For all other countries apply to: Philips Semiconductors,
Marketing Communications, Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN,
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Internet: <http://www.semiconductors.philips.com>

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