M52221DEMO

Demonstration Board for Freescale MCF52221 Hardware User Guide

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REVISION

Date	Rev	Comments
January 18, 2007	Α	Initial Release.

CAUTIONARY NOTES

- 1) Electrostatic Discharge (ESD) prevention measures should be used when handling this product. ESD damage is not a warranty repair item.
- Axiom Manufacturing does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under patent rights or the rights of others.
- 3) EMC Information on the M52221DEMO board:
 - a) This product, as shipped from the factory with associated power supplies and cables, has been verified to meet with FCC requirements as a **CLASS A** product.
 - b) This product is designed and intended for use as a development platform for hardware or software in an educational or professional laboratory.
 - c) In a domestic environment, this product may cause radio interference in which case the user may be required to take adequate prevention measures.
 - d) Attaching additional wiring to this product or modifying the product operation from the factory default as shipped may effect its performance and cause interference with other apparatus in the immediate vicinity. If such interference is detected, suitable mitigating measures should be taken.

TERMINOLOGY

This development board uses option selection jumpers. A jumper is a plastic shunt that connects 2 terminals electrically. Terminology for application of the option jumpers is as follows:

Jumper on, in, or installed - jumper is installed such that 2 pins are connected together.

Jumper off, out, or idle - jumper is installed on 1 pin only. It is recommended that jumpers be idled by installing on 1 pin so they will not be lost.

Cut-Trace – a circuit trace connection between component pads. The circuit trace may be cut using a knife to break the default connection. To reconnect the circuit, simply install a suitably sized 0-ohm resistor or attach a wire across the pads.

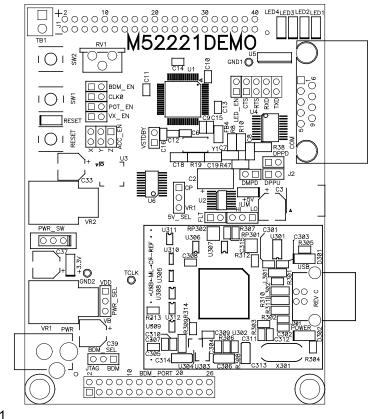
Signal names in this document that are followed by an asterisk (*) denotes active-low signals.

FEATURES

The M52221DEMO is a low-cost development board for the Freescale MCF52221 ColdFire microcontroller. Application development is quick and easy with the included DB9 serial cable, integrated BDM, and USB cable. A 128 MB flash-drive and 6-in-1 USB cable provide support for the integrated USB PHY. CodeWarrior Development Tools provide application development and debug support. The integrated BDM allows easy application development and debugging. An optional BDM port compatible with standard ColdFire BDM / JTAG interface cables and hosting software is also provided but not installed.

Features:

- MCF52221 CPU, 80 LQFP
 - 128 Byte Flash
 - 16K Byte Ram
 - USB On-The-Go (OTG) Phy
 - 4ch, DMA Controller w/ Timers
 - 2ea. Programmable Interrupt Timer
 - 4 GPT Timers
 - 8ch, 12b ADC
 - UART Serial Ports with DMA capability
 - QSPI and IIC Ports
 - 3.3V operation
- Integrated USB BDM
- 48 MHz XTAL
- 40 pin I/O port
- miniUSB Port
- BDM / JTAG Port (not installed)
- RS-232 Serial Port w/ DB9-S Connector
- ON/OFF Power Switch w/ LED indicator
- RESET switch w/ indicator
- Power Input Selection Jumper
 - Power Input from USB BDM
 - Power Input from on-board regulator
 - Power Input from terminal block
 - Power from connector J1
 - Optional Power output through connector J1
- User Features
 - 3-axis Accelerometer
 - 4 User LED's w/ enable
 - 2 User Push Switches
 - 5k ohm POT w/ enable
- Option Jumpers
 - Power Input Select
 - Optional Power Output Enable
 - BDM_EN
 - XTAL EN
 - POT EN
 - COM EN
 - LED EN
- Connectors
 - RJ-45 Ethernet Connector



- Type B USB connector
- DB9 Serial Connector
- 2.0mm Barrel Power Input
- 2pos, screw type, terminal block
- Supplied with DB9 Serial Cable, USB cable, Ethernet Cable, Support CD, and CodeWarrior Development Studio CD

Specifications:

Board Size 3.0" x 4.0"

Power Input: +5 to +16 VDC, 9VDC typical

REFERENCES

Reference documents are provided on the support CD in Acrobat Reader format.

M52221DEMO_UG.pdf M52221DEMO_SCH_C.pdf M52221DEMO_Silk_C.pdf M52221DEMO_Assy_C.pdf CFPRM.pdf USB 20 05122006.zip M52221DEMO User Guide (this document)
M52221DEMO Schematic, Rev C
M52221DEMO Top Silkscreen, Rev C
M52221DEMO Default Shunt Placement
ColdFire Programmers Reference Manual
USB2.0 Specification and OTG Supplement
with errata

OVERVIEW

The target MCU features an on-board USB On-the-Go (OTG) physical layer (Phy). The OTG Phy may be configured for either Host or Peripheral mode depending on the target application. The OTG protocol also allows mode switching under software control. Access to the OTG Phy is gained through the mini-AB (MAB) connector at J2. The OTG connection may be configured as either a standard USB bus connection or an OTG USB bus connection.

The MAB USB port connector at J2 should not be confused with the integrated USB BDM circuit. These are 2 separate circuits and do not interact in any way. The USB port provides access to the OTG Phy on the target MCU. The USB BDM allows the user to communicate with the target MCU using either CodeWarrior or P&E Microcomputer Systems debugger tools and a USB2.0 cable. This distinction must be understood and comprehended while reading this document.

The M52221DEMO board utilizes 2 separate voltage rails. The regulator at VR1 energizes the +3.3V rail for use by the target MCU and on-board logic. The regulator at VR2 energizes the +5Vrail for use by the OTG USB port. A charge-pump at U6 energizes the OTG USB rail when the board is powered from the USB BDM.

GETTING STARTED

To get started quickly, please refer to the M52221demo Quick Start Guide. This quick start will illustrate connecting the board to a PC, installing the correct version of CodeWarrior Development Studio, and running a simple HID test program.

SOFTWARE DEVELOPMENT

Software development requires a ColdFire assembler, or compiler, and a host PC running a ColdFire BDM interface. CodeWarrior Special Edition, supplied with this board, allows the user to develop and debug application code and to program flash.

One method to ensure successful application development is to load and debug application code from internal RAM. The application can be ported to FLASH after development is complete. However, this method limits code size to the 16 KB internal RAM size. When programmed into FLASH, the application will execute from Power-On or RESET if the RESET vector is programmed.

OPERATING MODES

The M52221DEMO board operates in two basic modes Run Mode, or Debug Mode. Run Mode executes user application code from Power-On or Reset, if the RESET vector is programmed. Debug Mode supports the development and debug of applications via the integrated USB BDM. An optional BDM_PORT provides access for any ColdFire compatible debug cable. The BDM_PORT is not installed in default configurations. See the related sections below for quickly starting the board in the desired mode of operation.

RUN Mode

Run mode executes the user application out of FLASH when power is applied to the board or the RESET button is pressed. The RESET vector must be programmed to allow application code to execute. Use the following settings to configure the M52221DEMO for RUN Mode using the USB bus to power the board. See the POWER section below for details on configuring the board for alternate power input.

- 1. Connect auxiliary cables and equipment to board if required.
- 2. Configure the board option jumpers as shown.

Table 1: Run Mode Setup

PWR_SEL	Set to VB		
BDM_EN	ON		
COM_EN	ALL ON (if required)		
VX_EN	ON (if required)		
LED_EN	ON (if required)		

3. Connect the A/B type USB cable to an open USB port on the host PC and attach to the USB BDM port on the target board. LED's D301 and D302 located adjacent to the USB connector, and the VDD LED will light and the loaded application will begin to execute, if the RESET vector has been programmed.

Debug Mode

Debug Mode supports application development and debug using the ColdFire background debug module (BDM). Background mode is accessible using either the integrated USB BDM or an external ColdFire compatible BDM cable. Using the integrated BDM requires a host PC with an available USB port and an A/B USB cable and appropriate hosting software. The USB cable must be USB 2.0 compliant. An external BDM cable can be attached to the 26-pin BDM_PORT header. This header is not installed in default configurations. The steps below describe using the integrated USB BDM. See the POWER section below for details on configuring the board for alternate power input.

- 1. Connect auxiliary cable and equipment to board if required.
- 2. Install and launch CodeWarrior 6.1 Special Edition. This will load the drivers necessary to support the USB connection.
- 3. Configure the board option jumpers as shown.

Table 2: Debug Mode Setup

PWR_SEL	Set to VB
BDM_EN	ON
COM_EN	ALL ON (if required)
VX_EN	ON (if required)
LED_EN	ON (if required)

4. Connect the supplied USB cable between an available USB port on the host PC and the USB BDM connector on the board. LED's D301 and D302 located adjacent to the USB connector, and the VDD LED will light. Hosting development software will establish background communication.

MEMORY MAP

Refer to the MCF52223 Integrated Microcontroller Reference Manual (RM) for details. The RM may be downloaded from the Freescale web site at www.freescale.com.

DEVELOPMENT SUPPORT

Application development and debug for the target MCF52221 is supported through the BDM interface. The debug interface consists of an optional 26-pin header (BDM_PORT) and an integrated USB BDM debugger. The BDM_PORT header is not installed in default configuration and may be installed by the user if needed. Refer to the MCF52223 RM for details on using the Background Debug Module

Optional JTAG access is also supported through the BDM_PORT header. To use this optional JTAG access, open the cut-trace between pin 1 and pin 2 of the BDM_SEL option header. Install a standard 1x3, 0.1", header at location BDM_SEL and install a shunt from pin 2 to pin 3. Refer to the MCF52223 RM (www.freescale.com) for details on using the JTAG port access.

BDM_PORT Header

A ColdFire compatible BDM cable may be attached to the 26-pin BDM_PORT port header. This header is not installed in default configuration. To use this feature, simply install a 2x13, 0.1" center, pin-header. Refer to the BDM documentation, in the RM, for details on using the BDM cable. The BDM_PORT header pin-out is shown below.

Figure 1: BDM PORT

NC	1	2	BKPT*
GND	3	4	DSCLK
GND	5	6	TCLK (JTAG)
RSTI*	7	8	DSI
VDD	9	10	DSO
GND	11	12	ALLPST
ALLPST	13	14	ALLPST
ALLPST	15	16	NC
NC	17	18	NC
NC	19	20	GND
NC	21	22	NC
GND	23	24	TCLK (BDM)
VDD	25	26	TA*

Refer to the MCF522235 Integrated Microcontroller Reference Manual for details on using the BDM PORT

NOTE: This header is not installed in default configuration.

Integrated BDM_PORT

The M52221DEMO board features an integrated USB BDM debugger. The integrated debugger supports application development and debugging via the background debug mode. A type B, USB connector provides connectivity between the target board and the host PC.

NOTE: Using the integrated USB BDM requires CodeWarrior 6.1 Special Edition or later. Development tools from P&E Microcomputer Systems also support the target MCF52221.

The integrated debugger provides power and ground to the target, thereby eliminating the need to power the board externally. Power from the integrated USB BDM is derived from the USB bus; therefore, current consumption is limited by the USB specification. Total current consumption for the target board, and any connected circuitry, must not exceed **500mA**. Excessive current drain will violate the USB specification causing the bus to disconnect. This will force a target POR.

CAUTION: Violating the USB specification will cause the USB bus to disconnect forcing the target to reset. Damage to the board or host PC may also result.

POWER

The M52221DEMO utilizes 2 separate voltage rails. The regulator at VR1 energizes the +3.3V rail and provides power to the target MCU and all on-board logic. The regulator at VR2 energizes the +5V rail and provides power the OTG USB bus when the board is configured for host mode applications.

The M52221DEMO is designed to allow application development while powered from the USB BDM. A 2.0mm barrel connector and a 2-position, screw-type, terminal block (BATT) has been applied to support stand-alone operation. The board may also be powered through connector J1. Additionally, the board may be configured to supply power through connector J1 to external circuitry.

An ON/OFF switch allows the user to quickly and easily connect and disconnect the +3.3V logic voltage rail. The +5V voltage rail supplies power to the USB bus through the MAB connector at J2 only and is not affected by the position of the ON/OFF switch.

When using the integrated USB BDM, the board draws power from the USB bus. Excessive current drain will violate the USB specification causing the USB bus to disconnect forcing a POR. Total current consumption of the board and any connected circuitry, therefore, must be less than **500mA**.

CAUTION: Violating the USB specification will cause the USB bus to disconnect. This will force a hard reset on the target.

The installed barrel connector accepts a center-positive, 2.1mm barrel plug. The terminal block accepts wire sizes ranging from 28ga to 16ga. Voltage input must be in the range between +6V and +15V. At no time should input voltage exceed +15V as damage to the board may result. The terminal block input is connected directly to the upper voltage rail. Input pro-

tection is not applied on this voltage input. The user must exercise caution when using the terminal block to input power to the board.

Voltage supplied through connector J1 is also connected directly to the board voltage rails. No protection is applied on this input and the user must exercise caution when powering the board from connector J1.

CAUTION: Input protection is **NOT** applied to the J1 or BATT power inputs. Excessive input voltage or current will damage the board.

Power Jack

The PWR power jack consists of a 2.1mm, center-positive, barrel connector. Voltage applied at this connector should range between +6V and +15V.

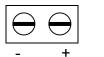
Figure 2: PWR Jack



Terminal Block

The BATT terminal block is a 3.5mm, screw-type terminal block connected directly to the VDD voltage rail. This allows the use of 2 AA batteries to supply power to the board. Exercise caution when using this input since input protection is not applied. This input requires a regulated +3.3V voltage source.

Figure 3: TB1 Terminal Block



Accepts wire size 28AWG – 16AWG Applied voltage must be +3.3V.

Connector J1

See the schematic for details on using this connection to supply power to the board or source power from the board. This input requires a regulated +3.3V voltage source.

CAUTION: Do not over drive either the J1 or TB1 inputs as damage to the board may result.

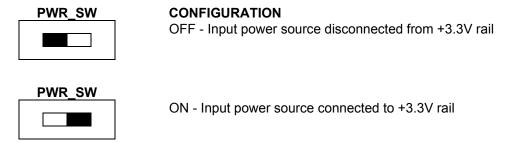
Power Indicators

The +3.3V LED shows when the +3.3V rail is energized. Located on the output of the ON/OFF switch, the +3.3V LED illuminates when the board is energized regardless of power input source. The +5V LED shows when the +5V rail is energized.

POWER SWITCH

The ON/OFF switch connects and disconnects all input sources to the +3.3V rail. In the OFF position, no voltage is present on the +3.3V rail. In the ON position, the input voltage source is connected to the +3.3V rail.

Figure 4: PWR_SW Switch



POWER SELECT

Two option headers control input power configuration for the M52221DEMO. The PWR_SEL header selects between the on-board, +3.3V, regulator and the USB BDM voltage input. The VX_EN header connects J1-1 directly to the +3.3V rail. The sections below show the different configuration for each option header.

PWR_SEL

Power from the integrated USB BDM is drawn from the USB bus and is limited to **500mA**. Excessive current drain will violate the USB specification causing the USB bus to disconnect.

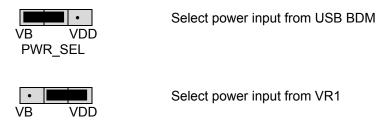
CAUTION: Violating the USB specification will cause the USB bus to disconnect. This will cause the board to reset.

Both on-board voltage regulators accept power input through a 2.1mm barrel connector (PWR). Input voltage may range from +6V to +15V. VR1 provides a +3.3V fixed voltage output (VDD) with output current limited to 800mA. Over-temperature and over-current limit built into the voltage regulator provides limited protection from damage due to excessive stresses.

The user should consider the maximum output current of the selected power source when attempting to power off-board circuitry through connector J1.

PWR SEL

Figure 5: PWR SEL Option Header

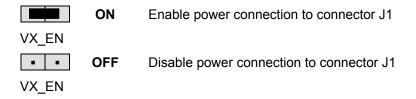


VX_EN

A 2-pin option header, VX_EN, connects input J1-1 directly to the +3.3V rail. J1-3 is connected directly to the ground plane. This input requires a regulated +3.3V voltage source. This power input is decoupled to minimize noise input but is not regulated. Also, no protection is applied on this input and damage to the target board may result if over-driven. Do not attempt to power the target board through this connector while also applying power through the USB BDM or the PWR connector as damage to the board may result.

Power may be sourced to off-board circuitry through the J1 connector. The current limitation of the USB bus or the on-board regulator must be considered when attempting to source power to external circuitry. Excessive current drain may damage the target board, the host PC USB hub, or the on-board regulator. The figure below details the VX_EN option header connections.

Figure 6. VX EN Option Header



CAUTION: Do not apply power to connector J1 while also sourcing power from either the PWR connector or the USB BDM circuit. Damage to the board may result.

NOTE: Do not exceed available current supply from USB BDM cable or on-board regulator when sourcing power through connector J1 to external circuitry.

USB OTG Power

The M52221DEMO is not designed to draw power from the USB cable connected to the MAB connector at J2. Power output to the USB MAB connector is provided by a high-side switch located at U2. This device provides the +5V output necessary for proper operation of the bus when the board is in host mode. The ILIM option header sets the output current limit. Current output is selectable between either 100 mA or 500 mA

Due to current limitations of the USB bus when powered from the USB BDM, the ILIM option header must be set to the LO position. Setting the ILIM option header to HI requires applying power to the board externally.

Figure 7: ILIM Option Header



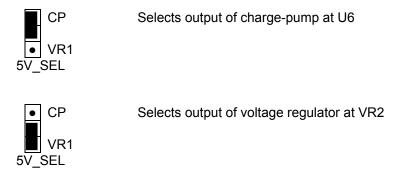
Sets output current limit to 500mA. This option should only be selected when the board is power externally.



Sets output current limit to 100mA. This option may be selected when the board is powered from the USB BDM or if powered externally.

A charge-pump located at U6 generates a +5V output for use when the board is power from the USB BDM. The USB BDM provides the +3.3V rail necessary to power on-board logic but does not provide the +5V rail necessary for USB OTG functionality. The 5V_SEL option header selects the power source for the +5V rail.

Figure 8: 5V_SEL Option Header



NOTE: The VR1 label at the 5V_SEL option header is incorrect and should read VR2. This option selects the output of the +5V regulator at VR2.

RESET

The M52221DEMO provides a RESET button, with indicator, to reset the target device. The MCF52221 also supports several internal resets. Consult the MCF522235 RM for details on all supported resets.

RESET SWITCH

The RESET switch provides a method to apply an asynchronous reset to the MCU and is connected directly to the RSTI* input on the MCU. Pressing the RESET switch holds RSTI* low until the switch is released. An external pull-up on the RSTI* line prevents spurious resets allowing normal operation.

RESET INDICATOR

The RESET LED is connected to the RSTO* output on the MCF52221. This LED lights when the MCU is in RESET and remains on for the duration of an asserted RSTO* signal. RSTO* may also be used as a general-purpose output to drive the RESET LED as needed.

LOW-POWER MODES

The MCF52221 supports several operational modes designed to reduce power consumption. Low-power modes include Wait, Doze, Stop, and Halt. Refer to the MCF52223 RM at www.freescale.com for details on configuring and using the various low-power modes.

TIMING

A 48MHz crystal oscillator (XTAL) provides timing for the M52221DEMO. Refer to the MCF52223 RM at www.freescale.com for details on use and configuration of the clock module.

COMMUNICATIONS

The M52221DEMO board provides 2 SCI ports, 1 QSPI port, and 1 IIC port. RS-232 communication is supported through a DB9 (COM) connector and through connector J1. QSPI and IIC communications are supported only through connector J1. The COM_EN option header enables SCI0 functionality between the MCU and the COM connector.

SCI Port

An RS-232 transceiver provides RS-232 to TTL/CMOS logic level translation between the COM connector and the MCU. The COM connector is a 9-pin Dsub, right-angle connector. A ferrite bead on shield ground provides conducted immunity protection. Communication signals TXD0 and RXD0 are routed from the transceiver to the MCU. These signals are also available on connector J1. Hardware flow control signals RTS0 and CTS0 are also routed from the transceiver to the MCU. RTS is biased for correct 2-wire operation.

SCI1 signals are available on connector J1 and route directly between the MCU and connector J1. No RS-232 logic-level translation is provided on SCI1 signals.

COM_EN

The COM_EN option header individually connects and disconnects SCI0 signals between the MCU and the SCI transceiver. Removing a shunt disconnects the associated signal. Installing a shunt connects the associated signal.

Figure 9: COM_EN Option Header

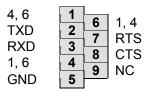
CTS	•	•
RTS	•	•
RXD	•	•
TXD	•	•

Shunt			
On	Off		
Enabled	Disabled		

COM Connector

A standard 9-pin Dsub connector provides external connections for the SCI0 port. The Dsub shell is connected to board ground through a ferrite bead. The ferrite bead provides noise isolation on the RS-232 connection. The DB9 connector pin-out is shown below.

Figure 10: COM Connector



Female DB9 connector that interfaces to the ColdFire internal SCI1 serial port via the RS232 transceiver.

Pins 1, 4, and 6 are connected together.

SPI Port

SPI signaling connects directly between connector J1 and the MCU. Refer to the MCF522235 RM at www.freescale.com for details on using the SPI interface.

IIC Port

IIC signaling connects directly between connector J1 and the MCU. Refer to the MCF522235 RM at www.freescale.com for details on using the IIC interface.

USB OTG

The M52221DEMO features an integrated USB On-the Go (OTG) physical layer (Phy) interface. The OTG Phy connects to an MAB connector at J2. Two option headers at DPPD and DMPD provide pull-down configuration for host mode if needed. Installing or removing both jumpers manually controls pull-down configuration. Pull-up configuration for device mode is integral to the MCF52221 MCU.

A high-side switch at U2 provides power to the USB bus when the board is configured for host mode. The ILIM option header sets the output current limit. See the USB OTG Power section above for further details.

Refer to the MCF52223 RM for additional information on using the OTG Phy. Also refer to the USB2.0 Specification and the On-the-Go Supplement to the USB2.0 Specification for additional information. The USB2.0 Specification and the OTG Supplement can be downloaded from the USB Implementers Forum (USB-IF) at www.usb.org. These documents are also available on the Axiom Manufacturing Support CD.

ACCELEROMETER

The M52221DEMO applies an MMA7260Q, 3-axis accelerometer for tilt and motion-sense applications. The accelerometer supports 4 user selectable sensitivities - 1.5g / 2g / 4g / 6g. The SLEEP* input allows the device to be placed in a low-power mode. Separate (X/Y/Z) axis readings are routed to the MCU

An option header at ACC_EN allows the user to disconnect the accelerometer if necessary. In default configurations, this option header is not installed and a cut-trace completes the signal path. To disconnect the accelerometer, simply open the cut-trace and install a 1x3 pin-header at ACC_EN. Install a shunt on each signal to reconnect the accelerometer. The table below shows the signal connections to the MCU.

Table 3: ACC_EN Option Header

Signal	MCU Input	
Χ	AN4	
Υ	AN5	
Z	AN6	

In default configuration, this option header is not installed. Cuttraces on the bottom of the PCB provide signal pathways. To isolate these analog inputs, simply open the cut-traces and install a 2x3, 0.1" pin header.

USER OPTIONS

The M52221DEMO includes various input and output devices to aid application development. User I/O devices include 2 pushbutton switches, 4 green LEDs, and 1 potentiometer. The table below summarizes user option connections on the development board.

Table 4: User Option Connections

OPTION	MCU PORT	MCU PIN
SW1	IRQ7	58
SW2	IRQ1	56
LED1	DTIN0	22
LED2	DTIN1	23
LED3	DTIN2	18
LED4	DTIN3	19
RV1	AN0	25

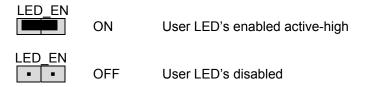
Pushbutton Switches

Two push button switches provide momentary, active-low input, for user applications. Pull-ups internal to the MCU must be enabled to provide error-free switch operation. Pushbutton switches SW1 and SW2 are connected to MCU I/O ports IRQ7* and IRQ1* respectively.

User LED's

Four green LED's are provided for use in application development and debug. Each LED is configured for active-high operation. An LED_EN option header enables indicators LED1 through LED4. A 3S buffer between the MCU port and the user LED's provides the drive current necessary to control the LED's.

Figure 11: LED_EN Option Header



Potentiometer

A 5k ohm, single-turn, thumb-wheel type, potentiometer at RV1 provides continuous, variable resistance input for user applications. The output is the result of a voltage divider that changes as the thumb-wheel is turned. The potentiometer is connected between VDD and GND with the center tap providing the divider output. This center tap is connected to the MCU on input ANO. The potentiometer may be disconnected from ANO by means of the POT_EN option header.

Figure 12: POT EN Option Header



I/O PORT CONNECTOR

Connector J1 provides access to M52221DEMO I/O signals. Signal positions not shown are not connected (NC).

Figure 13: Connector J1

VDD	1	2	IRQ4*
GND	3	4	RSTI*
UTXD1	5	6	RSTO*
URXD1	7	8	NC
URTS1*	9	10	AN0
UCTS1*	11	12	AN1
AN2	13	14	AN2
AN3	15	16	AN3
QSPI_DOUT	17	18	AN4
QSPI_DIN	19	20	AN5
QSPI_SCK	21	22	AN6
QSPI_CS0	23	24	AN7
UTXD0	25	26	SCL
URXD0	27	28	SDA
URTS0*	29	30	NC
UCTS0*	31	32	NC
IRQ1*	33	34	DTIN0
VRH	35	36	DTIN1
VRL	37	38	DTIN2
IRQ7*	39	40	DTIN3