

# CBT3257A

## Quad 1-of-2 multiplexer/demultiplexer

Rev. 8 — 16 March 2021

Product data sheet

### 1. General description

The CBT3257A is a quad single-pole, dual-throw bus switch. The device features an output enable input ( $\overline{OE}$ ) and a select input (S). When  $\overline{OE}$  is LOW the switch is enabled and the select input can be used to connect the nA terminals to either of the associated nB terminals.

### 2. Features and benefits

- 5  $\Omega$  switch connection between two ports
- Minimal propagation delay through the switch
- Direct interface with TTL levels
- Overvoltage tolerant control inputs to 5.5 V
- Latch-up protection exceeds 100 mA per JEDEC standard JESD78 class II level A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101E exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C

### 3. Ordering information

Table 1. Ordering information

Type number	Temperature range	Package		
		Name	Description	Version
CBT3257AD	-40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
CBT3257ADB	-40 °C to +85 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
CBT3257ADS	-40 °C to +85 °C	SSOP16 [1]	plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT519-1
CBT3257APW	-40 °C to +85 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
CBT3257ABQ	-40 °C to +85 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

[1] Also known as QSOP16.

### 4. Functional diagram

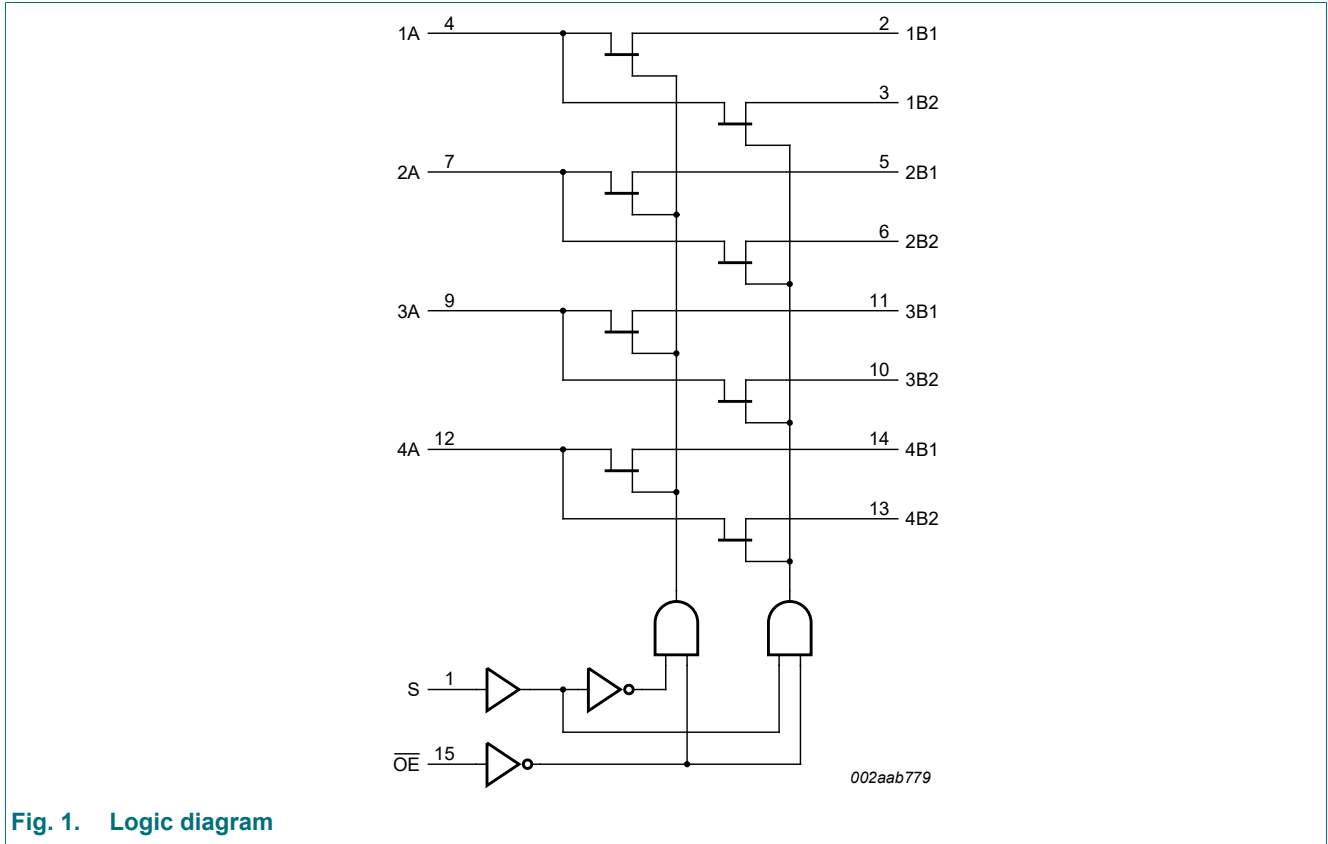
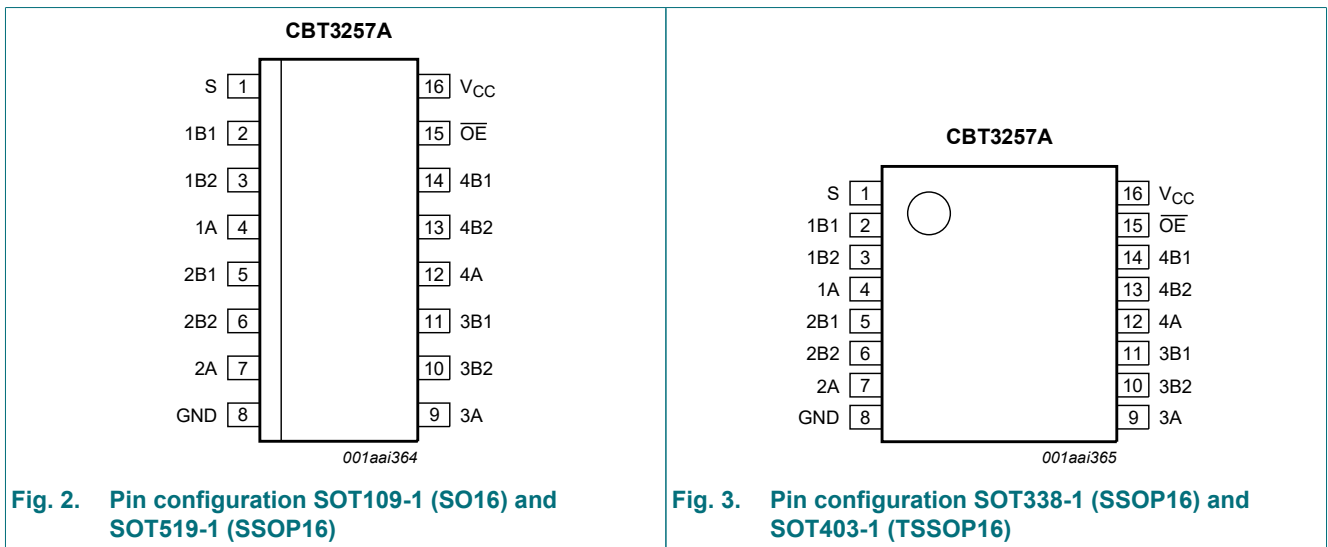
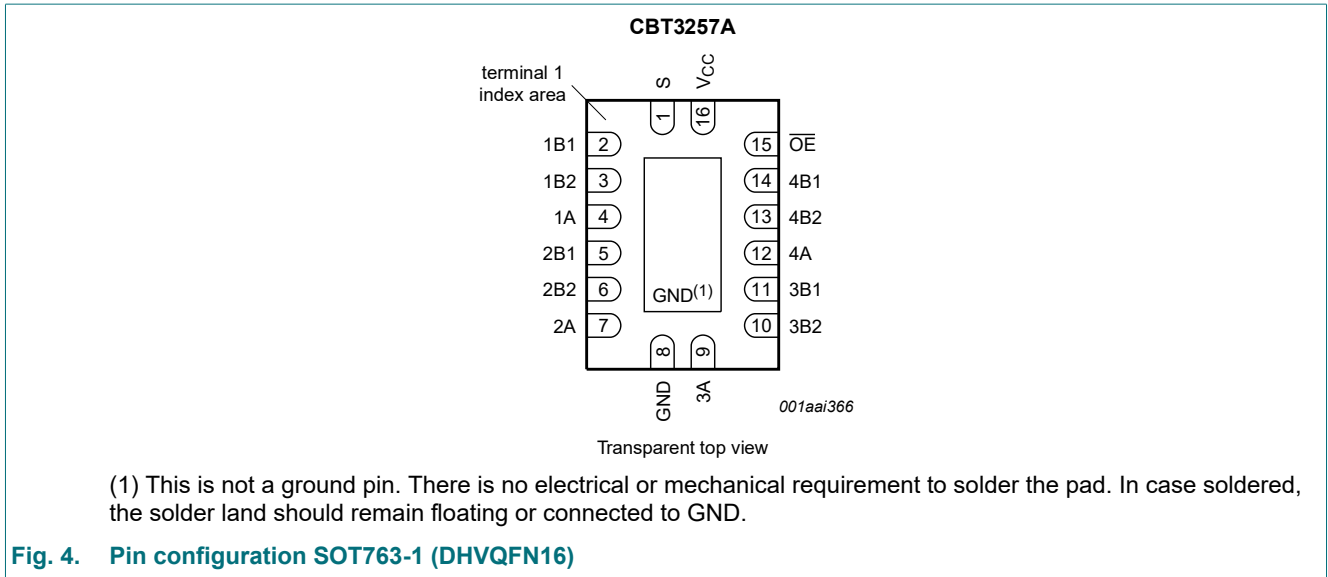


Fig. 1. Logic diagram

### 5. Pinning information

#### 5.1. Pinning





### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
S	1	select control input
1B1, 2B1, 3B1, 4B1,	2, 5, 11, 14	B1 outputs/inputs
1B2, 2B2, 3B2, 4B2	3, 6, 10, 13	B2 outputs/inputs
1A, 2A, 3A, 4A	4, 7, 9, 12	A inputs/outputs
GND	8	ground (0 V)
OE	15	output enable (active LOW)
V <sub>CC</sub>	16	positive supply voltage

## 6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; X = Don't care.

Inputs		Switch
OE	S	
L	L	nA to nB1
L	H	nA to nB2
H	X	switch off

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage	[1]	-0.5	+7.0	V
$I_{SW}$	switch current	continuous current through each switch	-	128	mA
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +85 °C	-	500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

## 8. Recommended operating conditions

**Table 5. Operating conditions**

All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		4.5	5.5	V
$V_{IH}$	HIGH-level input voltage		2.0	-	V
$V_{IL}$	LOW-level input voltage		-	0.8	V
$T_{amb}$	ambient temperature	operating in free-air	-40	+85	°C

## 9. Static characteristics

**Table 6. Static characteristics**

Symbol	Parameter	Conditions	$T_{amb} = -40$ °C to +85 °C.			Unit
			Min	Typ[1]	Max	
$V_{IK}$	input clamping voltage	$V_{CC} = 4.5$ V; $I_I = -18$ mA	-	-	-1.2	V
$V_{pass}$	pass voltage	$V_I = V_{CC} = 5.0$ V; $I_O = -100$ $\mu$ A	3.6	3.9	4.2	V
$I_I$	input leakage current	$V_{CC} = 5.5$ V; $V_I =$ GND or 5.5 V	-	-	$\pm 1$	$\mu$ A
$I_{CC}$	supply current	$V_{CC} = 5.5$ V; $I_O = 0$ mA; $V_I = V_{CC}$ or GND	-	-	3	$\mu$ A
$\Delta I_{CC}$	additional supply current	per input; $V_{CC} = 5.5$ V; one input at 3.4 V, other inputs at $V_{CC}$ or GND [2]	-	-	2.5	mA
$C_I$	input capacitance	control pins; $V_I = 3$ V or 0 V	-	3.3	-	pF
$C_{io(off)}$	off-state input/output capacitance	A port; $V_O = 3$ V or 0 V; $\overline{OE} = V_{CC}$	-	9.9	-	pF
		B port; $V_O = 3$ V or 0 V; $\overline{OE} = V_{CC}$	-	6.4	-	pF
$R_{ON}$	ON resistance	$V_{CC} = 4.5$ V [3]				
		$V_I = 0$ V; $I_I = 64$ mA	-	5	7	$\Omega$
		$V_I = 0$ V; $I_I = 30$ mA	-	5	7	$\Omega$
		$V_I = 2.4$ V; $I_I = 15$ mA	-	10	15	$\Omega$

[1] All typical values are measured at  $V_{CC} = 5$  V;  $T_{amb} = 25$  °C.

[2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

[3] Measured by the voltage drop between the nA and the nBn terminals at the indicated current through the switch. The lowest voltage of the two (nA or nBn) terminals determines the ON resistance.

## 10. Dynamic characteristics

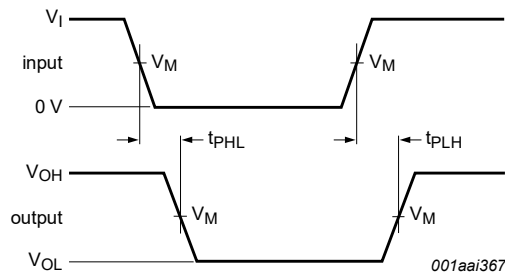
**Table 7. Dynamic characteristics**

$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ; for test circuit see [Fig. 7](#).

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ °C to }+85\text{ °C}$		Unit
			Min	Max	
$t_{pd}$	propagation delay	nA to nBn or nBn to nA; see <a href="#">Fig. 5</a> [1] [2]	-	0.25	ns
		S to nA; see <a href="#">Fig. 5</a> [1] [2]	1.4	5.0	ns
$t_{en}$	enable time	$\overline{OE}$ to nA or nBn; see <a href="#">Fig. 6</a> [2]	1.5	5.1	ns
		S to nBn; see <a href="#">Fig. 6</a> [2]	1.4	5.2	ns
$t_{dis}$	disable time	$\overline{OE}$ to nA or nBn; see <a href="#">Fig. 6</a> [2]	2.2	5.5	ns
		S to nBn; see <a href="#">Fig. 6</a> [2]	1.0	5.0	ns

- [1] This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical ON resistance of the switch and a load capacitance, when driven by an ideal voltage source (zero output impedance).
- [2]  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ ;  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ ;  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .

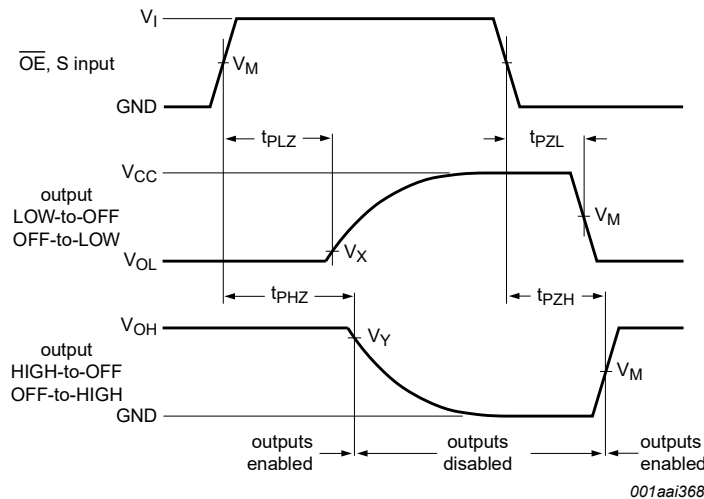
### 10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig. 5. The input (nA; nBn) to output (nBn; nA) or input (S) to output (nA) propagation delay times**



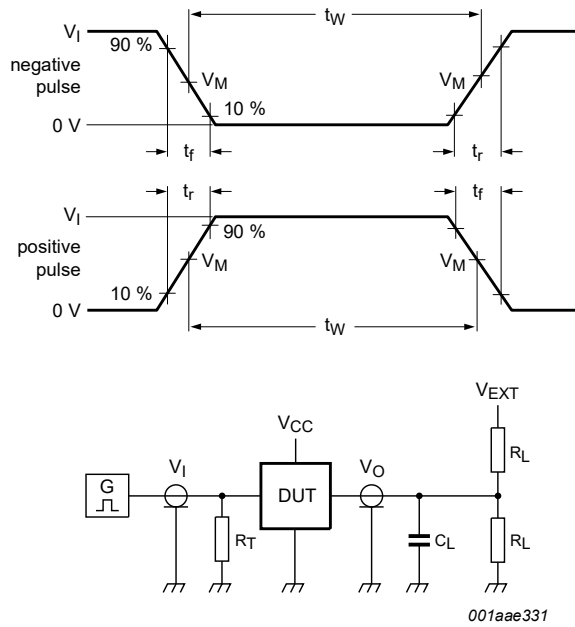
Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig. 6. Enable and disable times**

Table 8. Measurement points

Supply voltage	Input		Output		
$V_{CC}$	$V_I$	$V_M$	$V_M$	$V_X$	$V_Y$
4.5 V to 5.5 V	GND to 3.0 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$



Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

Fig. 7. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		$V_{EXT}$		
$V_{CC}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
4.5 V to 5.5 V	GND to 3.0 V	$\leq 2.5 \text{ ns}$	50 pF	500 $\Omega$	open	7.0 V	open

### 11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

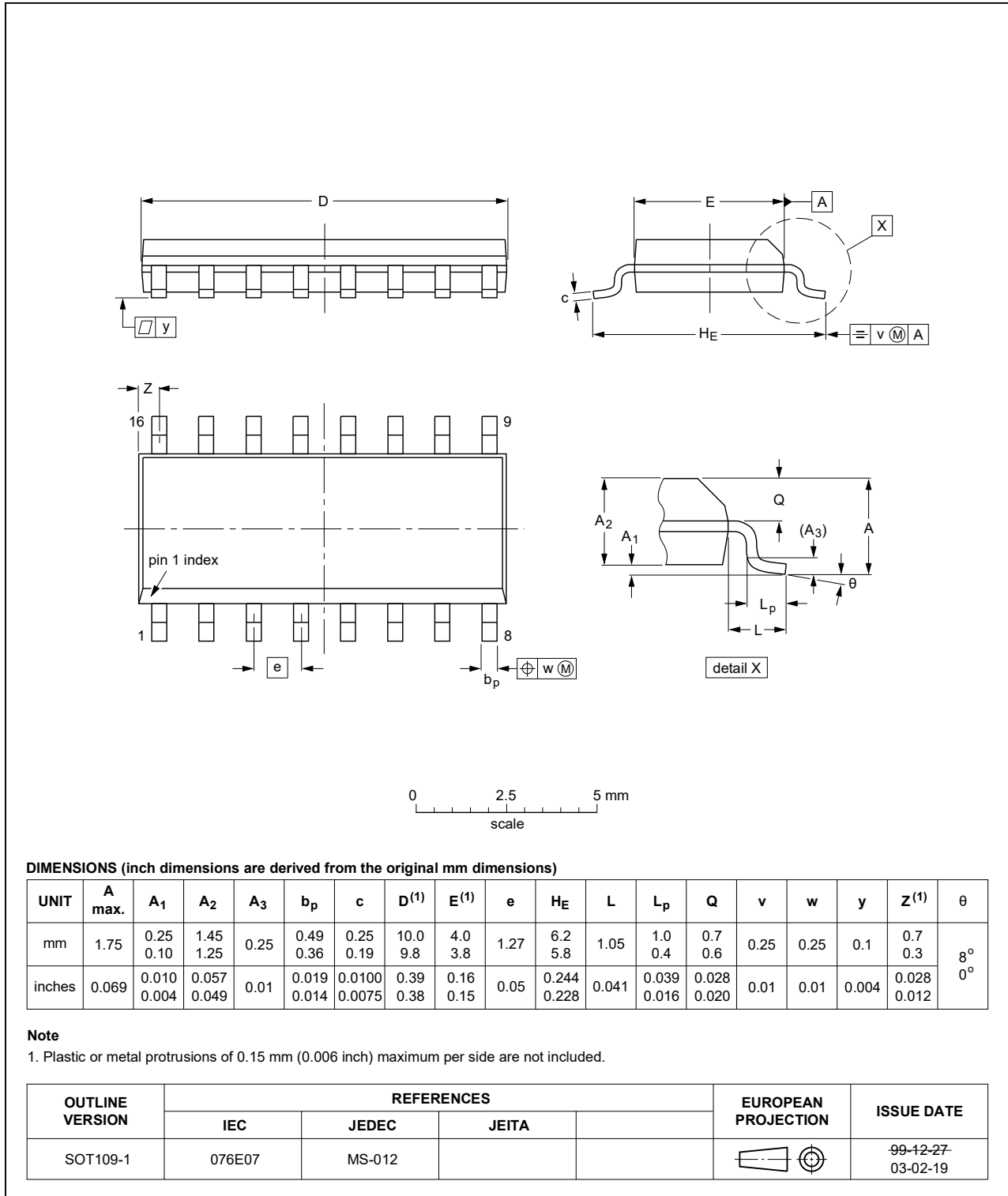


Fig. 8. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

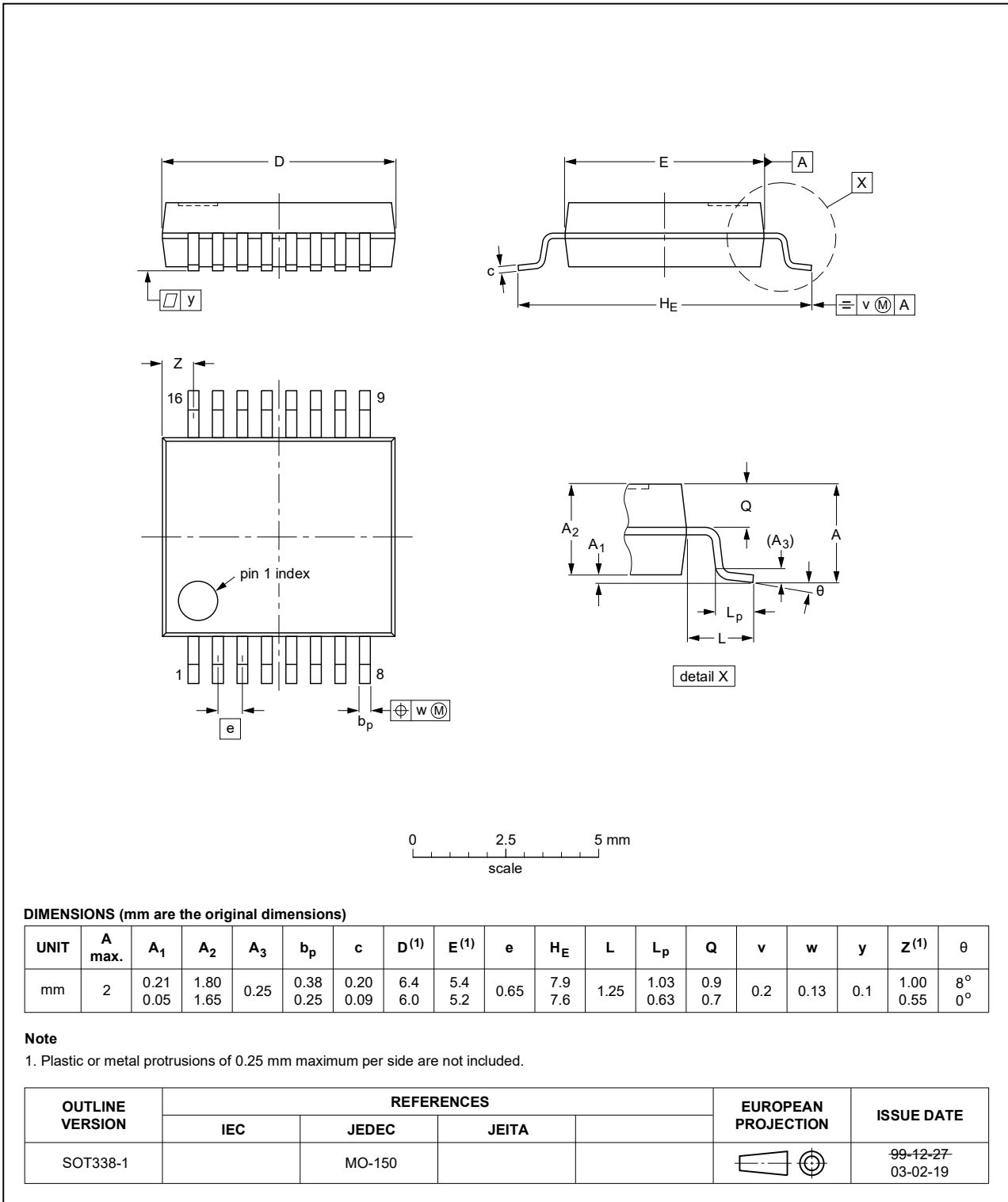


Fig. 9. Package outline SOT338-1 (SSOP16)



SSOP16: plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm SOT519-1

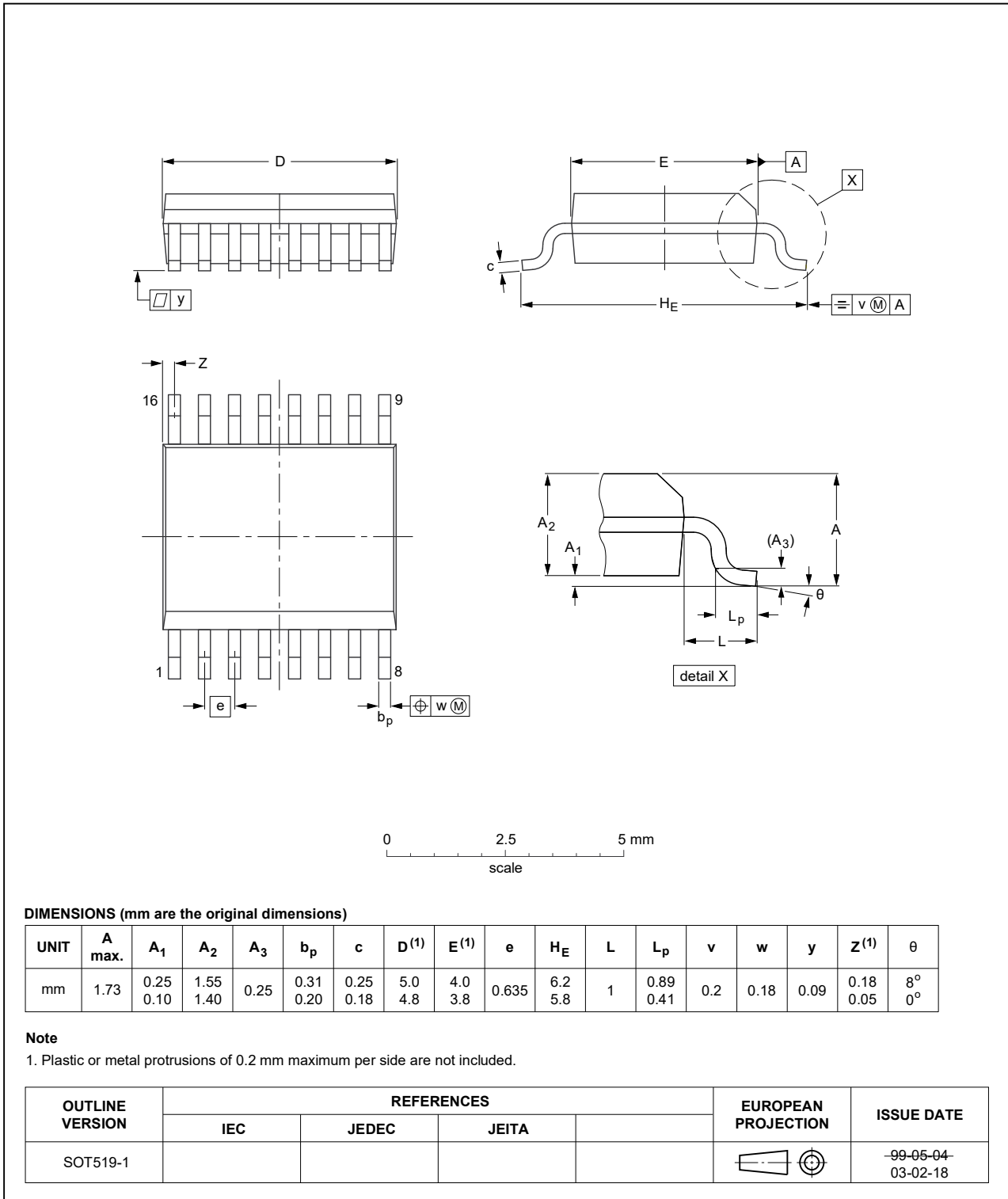


Fig. 10. Package outline SOT519-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

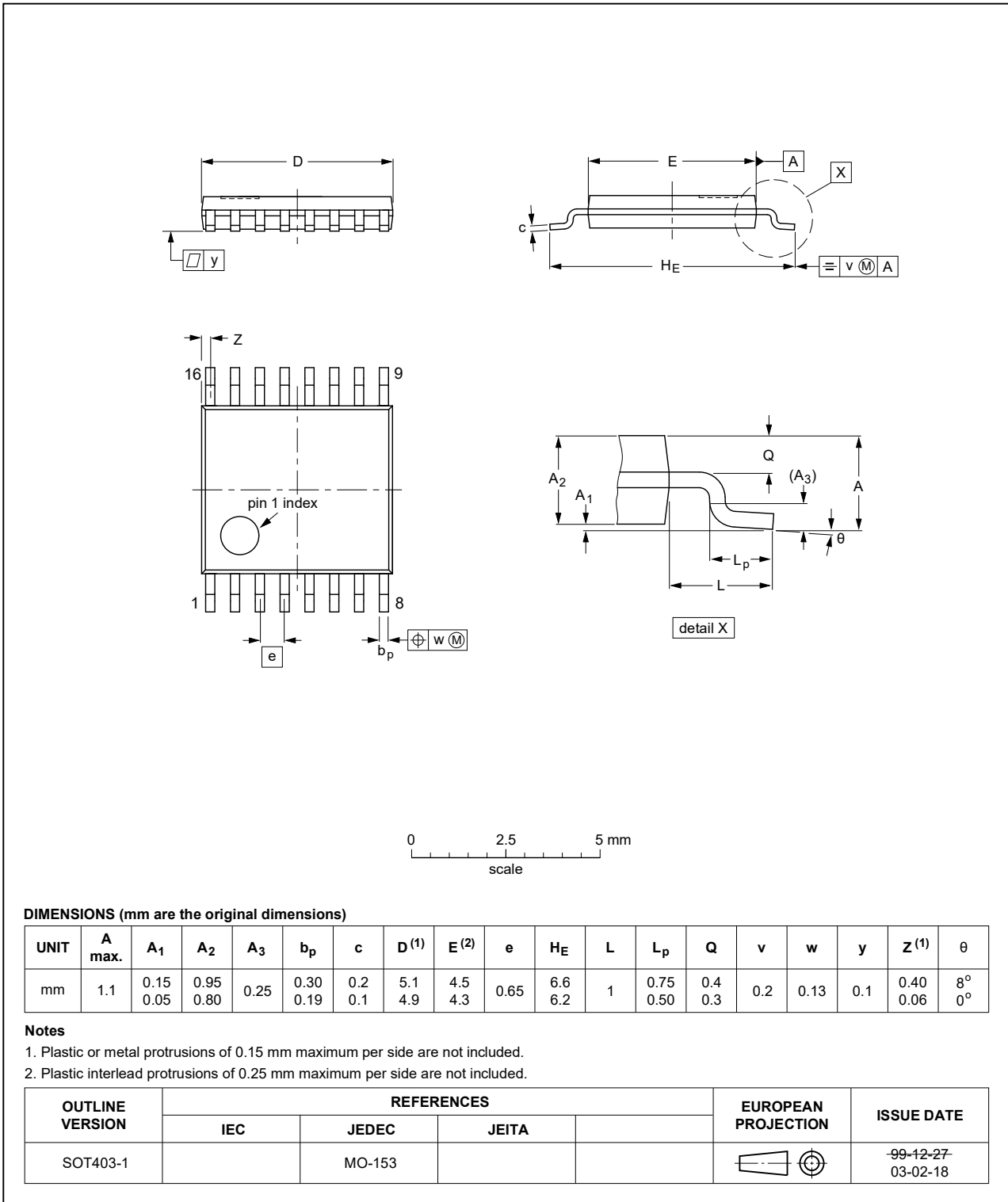


Fig. 11. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

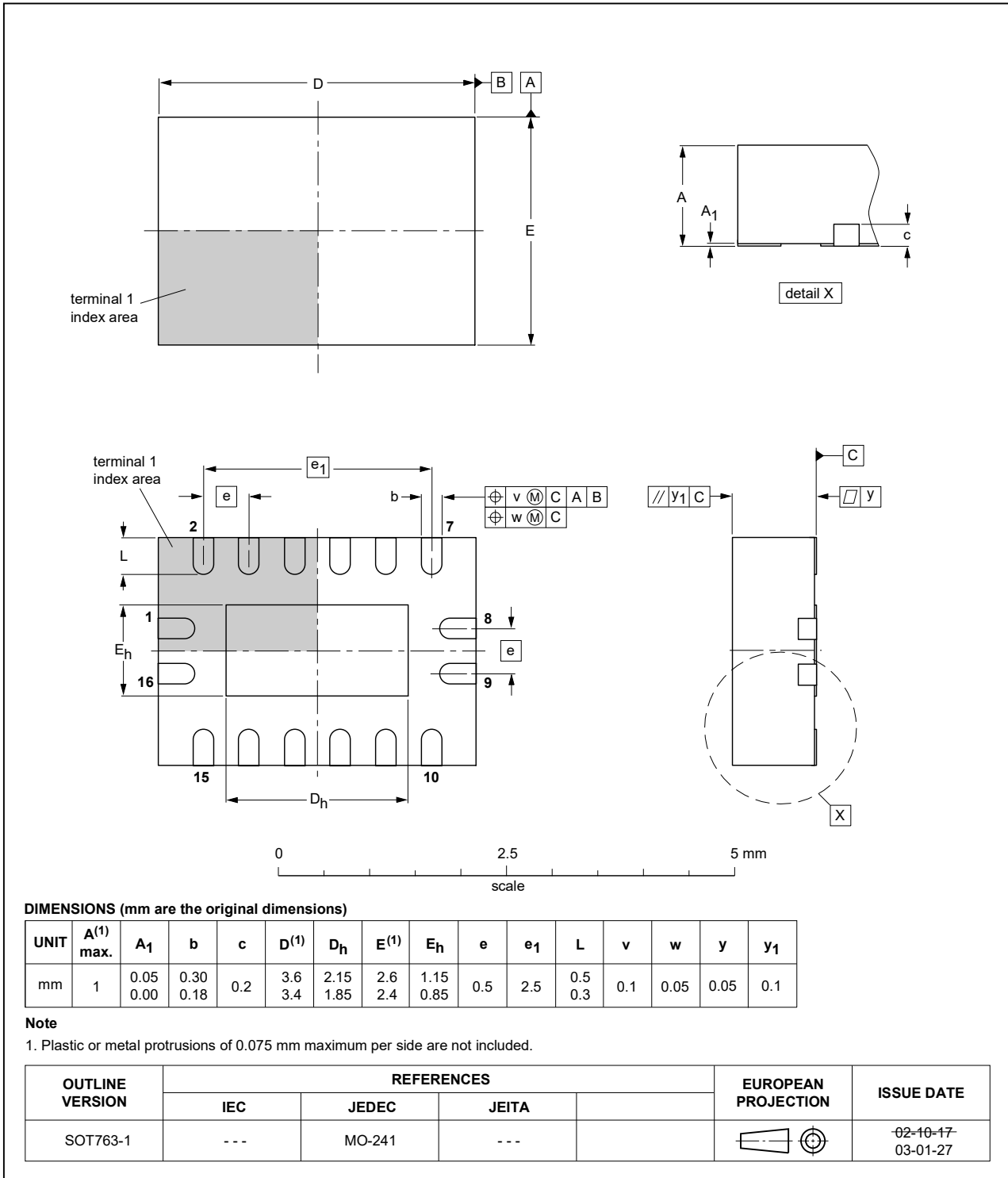


Fig. 12. Package outline SOT763-1 (DHVQFN16)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBT3257A v.8	20210316	Product data sheet	-	CBT3257A v.7
Modifications:	<ul style="list-style-type: none"> <li>Type number CBT3257ADB (SOT338-1 / SSOP16) added.</li> </ul>			
CBT3257A v.7	20210208	Product data sheet	-	CBT3257A v.6
Modifications:	<ul style="list-style-type: none"> <li>Type number CBT3257ADB (SOT338-1 / SSOP16) removed.</li> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> </ul>			
CBT3257A v.6	20190620	Product data sheet	-	CBT3257A v.5
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
CBT3257A v.5	20130404	Product data sheet	-	CBT3257A v.4
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 6</a>: values for pass voltage modified.</li> </ul>			
CBT3257A v.4	20090319	Product data sheet	-	CBT3257A v.3
CBT3257A v.3	20080704	Product data sheet	-	CBT3257A v.2
CBT3257A v.2	20070704	Product data sheet	-	CBT3257A v.1
CBT3257A v.1	20051027	Product data sheet	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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