

74ABT162244

16-bit buffer/line driver with 30 Ω series termination resistors;
3-state

Rev. 7 — 2 July 2021

Product data sheet

1. General description

The 74ABT162244 is a 16-bit buffer/line driver with 30 Ω termination resistors and 3-state outputs. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer. The device features four output enables (1OE, 2OE, 3OE and 4OE), each controlling four of the 3-state outputs. A HIGH on nOE causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Supply voltage range from 4.5 V to 5.5 V
- BiCMOS high speed and output drive
- Direct interface with TTL levels
- Power-up 3-state
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up protection exceeds 500 mA per JESD78B class II level A
- 16-bit bus interface
- Multiple V_{CC} and GND pins minimize switching noise
- 3-state buffers
- Output capability: +12 mA and -32 mA
- Live insertion and extraction permitted
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - CDM JESD22-C101-C exceeds 1000 V
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|----------------|-------------------|---------|--|----------|
| | Temperature range | Name | Description | Version |
| 74ABT162244DGG | -40 °C to +85 °C | TSSOP48 | plastic thin shrink small outline package; 48 leads; body width 6.1 mm | SOT362-1 |

4. Functional diagram

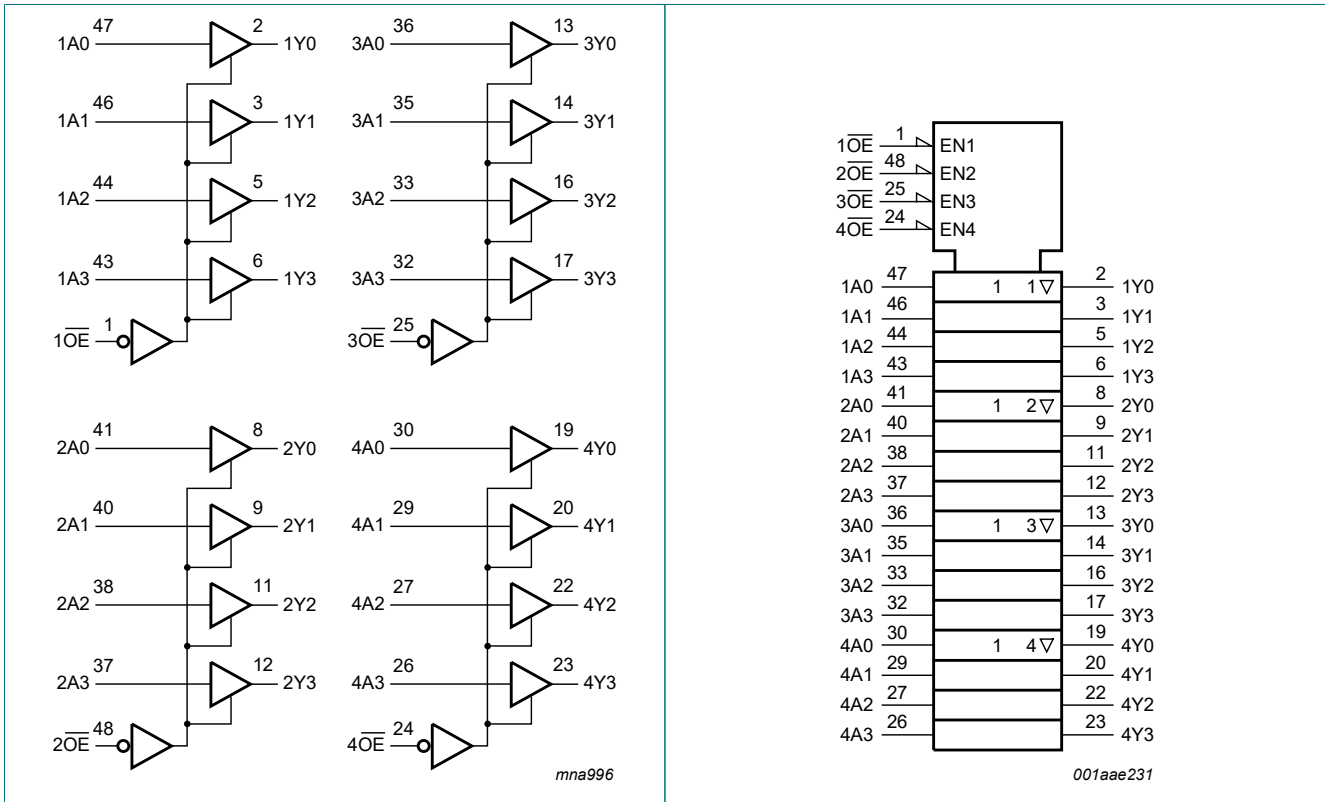


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

Fig. 3. Logic diagram one output

5. Pinning information

5.1. Pinning

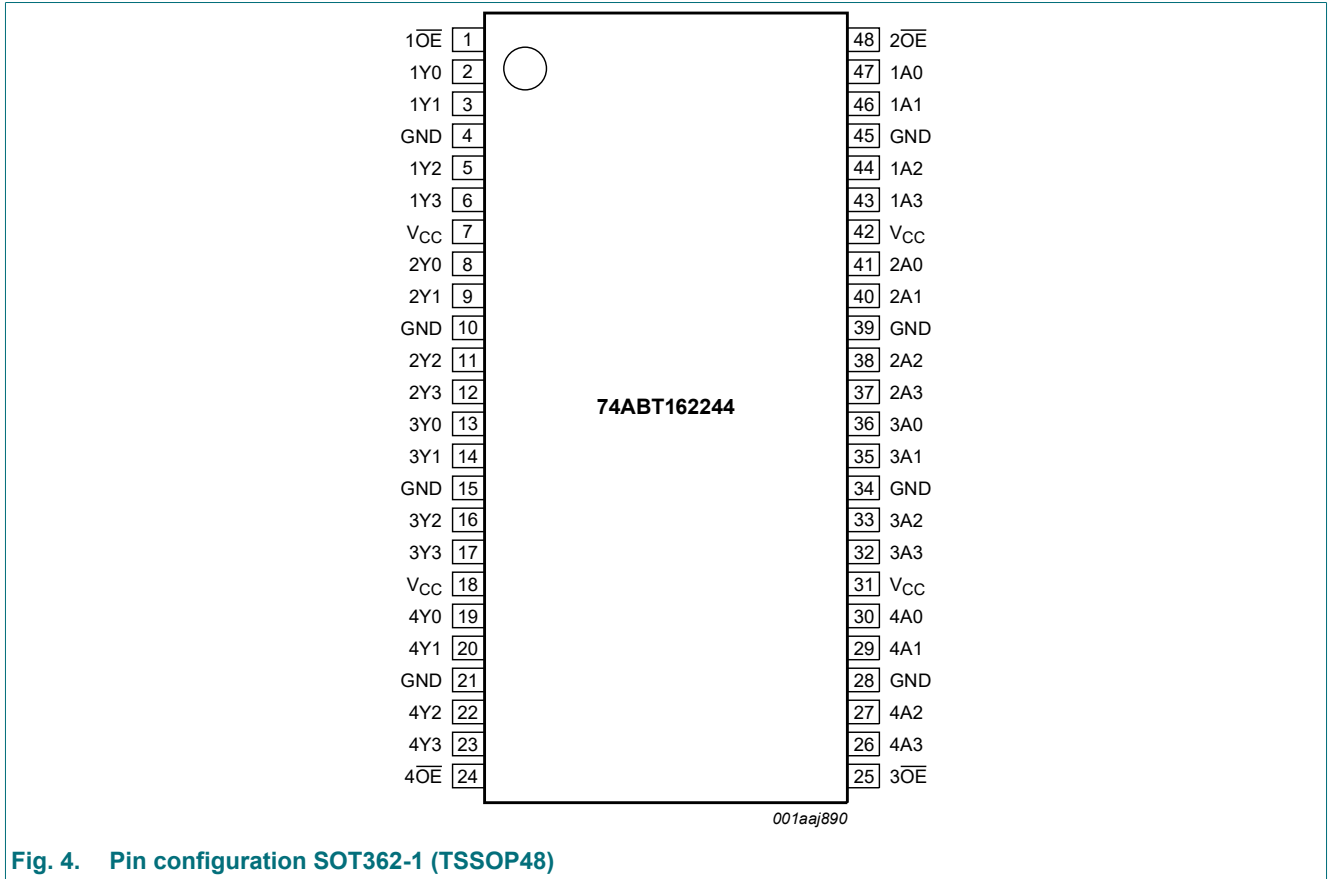


Fig. 4. Pin configuration SOT362-1 (TSSOP48)

5.2. Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|--------------------|-------------------------------|-----------------------------------|
| 1OE, 2OE, 3OE, 4OE | 1, 48, 25, 24 | 1 to 4 output enable (LOW active) |
| 1Y0, 1Y1, 1Y2, 1Y3 | 2, 3, 5, 6 | 1 data output 0 to output 3 |
| GND | 4, 10, 15, 21, 28, 34, 39, 45 | ground (0 V) |
| V _{CC} | 7, 18, 31, 42 | supply voltage |
| 2Y0, 2Y1, 2Y2, 2Y3 | 8, 9, 11, 12 | 2 data output 0 to output 3 |
| 3Y0, 3Y1, 3Y2, 3Y3 | 13, 14, 16, 17 | 3 data output 0 to output 3 |
| 4Y0, 4Y1, 4Y2, 4Y3 | 19, 20, 22, 23 | 4 data output 0 to output 3 |
| 4A0, 4A1, 4A2, 4A3 | 30, 29, 27, 26 | 4 data input 0 to input 3 |
| 3A0, 3A1, 3A2, 3A3 | 36, 35, 33, 32 | 3 data input 0 to input 3 |
| 2A0, 2A1, 2A2, 2A3 | 41, 40, 38, 37 | 2 data input 0 to input 3 |
| 1A0, 1A1, 1A2, 1A3 | 47, 46, 44, 43 | 1 data input 0 to input 3 |

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

| Control | Input | Output |
|---------|-------|--------|
| nOE | nAn | nYn |
| L | L | L |
| L | H | H |
| H | X | Z |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|-----------------------------------|----------|------|--------------|
| V_{CC} | supply voltage | | -0.5 | +7.0 | V |
| V_I | input voltage | | [1] -1.2 | +7.0 | V |
| V_O | output voltage | output in OFF-state or HIGH-state | [1] -0.5 | +5.5 | V |
| I_{IK} | input clamping current | $V_I < 0$ V | -18 | - | mA |
| I_{OK} | output clamping current | $V_O < 0$ V | -50 | - | mA |
| I_O | output current | output in LOW-state | - | 128 | mA |
| | | output in HIGH-state | - | -64 | mA |
| T_j | junction temperature | | [2] - | 150 | $^{\circ}$ C |
| T_{stg} | storage temperature | | -65 | +150 | $^{\circ}$ C |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

8. Recommended operating conditions

Table 5. Operating conditions

Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|-------------|-----|-----|----------|--------------|
| V_{CC} | supply voltage | | 4.5 | - | 5.5 | V |
| V_I | input voltage | | 0 | - | V_{CC} | V |
| V_{IH} | HIGH-level input voltage | | 2.0 | - | - | V |
| V_{IL} | LOW-level Input voltage | | - | - | 0.8 | V |
| I_{OH} | HIGH-level output current | | -32 | - | - | mA |
| I_{OL} | LOW-level output current | | - | - | 12 | mA |
| $\Delta t/\Delta V$ | input transition rise and fall rate | | - | - | 10 | ns/V |
| T_{amb} | ambient temperature | in free air | -40 | - | +85 | $^{\circ}$ C |

9. Static characteristics

Table 6. Static characteristics

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | Unit |
|-----------------|------------------------------------|---|-------|------------|-----------|------------------|-----------|---------------|
| | | | Min | Typ | Max | Min | Max | |
| V_{IK} | input clamping voltage | $V_{CC} = 4.5 \text{ V}$; $I_{IK} = -18 \text{ mA}$ | - | -0.9 | -1.2 | - | -1.2 | V |
| V_{OH} | HIGH-level output voltage | $V_I = V_{IL}$ or V_{IH} | | | | | | |
| | | $V_{CC} = 4.5 \text{ V}$; $I_{OH} = -3 \text{ mA}$ | 2.5 | 2.9 | - | 2.5 | - | V |
| | | $V_{CC} = 5.0 \text{ V}$; $I_{OH} = -3 \text{ mA}$ | 3.0 | 3.4 | - | 3.0 | - | V |
| | | $V_{CC} = 4.5 \text{ V}$; $I_{OH} = -32 \text{ mA}$ | 2.0 | 2.4 | - | 2.0 | - | V |
| V_{OL} | LOW-level output voltage | $V_I = V_{IL}$ or V_{IH} | | | | | | |
| | | $V_{CC} = 4.5 \text{ V}$; $I_{OL} = 8 \text{ mA}$ | - | - | 0.65 | - | 0.65 | V |
| | | $V_{CC} = 4.5 \text{ V}$; $I_{OL} = 12 \text{ mA}$ | - | - | 0.80 | - | 0.80 | V |
| I_I | input leakage current | $V_{CC} = 5.5 \text{ V}$; $V_I = V_{CC}$ or GND | - | ± 0.01 | ± 1.0 | - | ± 1.0 | μA |
| I_{OFF} | power-off leakage current | $V_{CC} = 0 \text{ V}$; V_I or $V_O \leq 4.5 \text{ V}$ | - | ± 5.0 | ± 100 | - | ± 100 | μA |
| $I_{O(pu/pd)}$ | power-up/power-down output current | $V_{CC} = 2.0 \text{ V}$; $V_O = 0.5 \text{ V}$; $V_I = \text{GND}$ or V_{CC} ; $n\overline{OE} = \text{HIGH}$ [1] | - | ± 5.0 | ± 50 | - | ± 50 | μA |
| I_{OZ} | OFF-state output current | $V_{CC} = 5.5 \text{ V}$; $V_I = V_{IL}$ or V_{IH} | | | | | | |
| | | output HIGH-state at $V_O = 5.5 \text{ V}$ | - | 0.1 | 10 | - | 10 | μA |
| | | output LOW-state at $V_O = 0 \text{ V}$ | - | -0.1 | -10 | - | -10 | μA |
| I_{CEX} | output high leakage current | HIGH-state; $V_O = 5.5 \text{ V}$; $V_{CC} = 5.5 \text{ V}$; $V_I = \text{GND}$ or V_{CC} | - | 5.0 | 50 | - | 50 | μA |
| I_O | output current | $V_{CC} = 5.5 \text{ V}$; $V_O = 2.5 \text{ V}$ [2] | -50 | -100 | -180 | -50 | -180 | mA |
| I_{CC} | supply current | $V_{CC} = 5.5 \text{ V}$; $V_I = \text{GND}$ or V_{CC} | | | | | | |
| | | outputs HIGH-state | - | 0.50 | 1.0 | - | 1.0 | mA |
| | | outputs LOW-state | - | 10 | 19 | - | 19 | mA |
| | | outputs 3-state | - | 0.50 | 1.0 | - | 1.0 | mA |
| ΔI_{CC} | additional supply current | per input pin; $V_{CC} = 5.5 \text{ V}$; one input at 3.4 V and other inputs at V_{CC} or GND [3] [4] | - | 100 | 250 | - | 250 | μA |
| C_I | input capacitance | $V_I = 0 \text{ V}$ or V_{CC} | - | 3 | - | - | - | pF |
| $C_{I/O}$ | input/output capacitance | outputs disabled; $V_O = 0 \text{ V}$ or V_{CC} | - | 7 | - | - | - | pF |

[1] This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 ms.

From $V_{CC} = 2.1 \text{ V}$ to $V_{CC} = 5 \text{ V} \pm 10 \%$, a transition time of up to 100 μs is permitted.

[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[3] This is the increase in supply current for each input at 3.4 V.

[4] This data sheet limit may vary among suppliers.

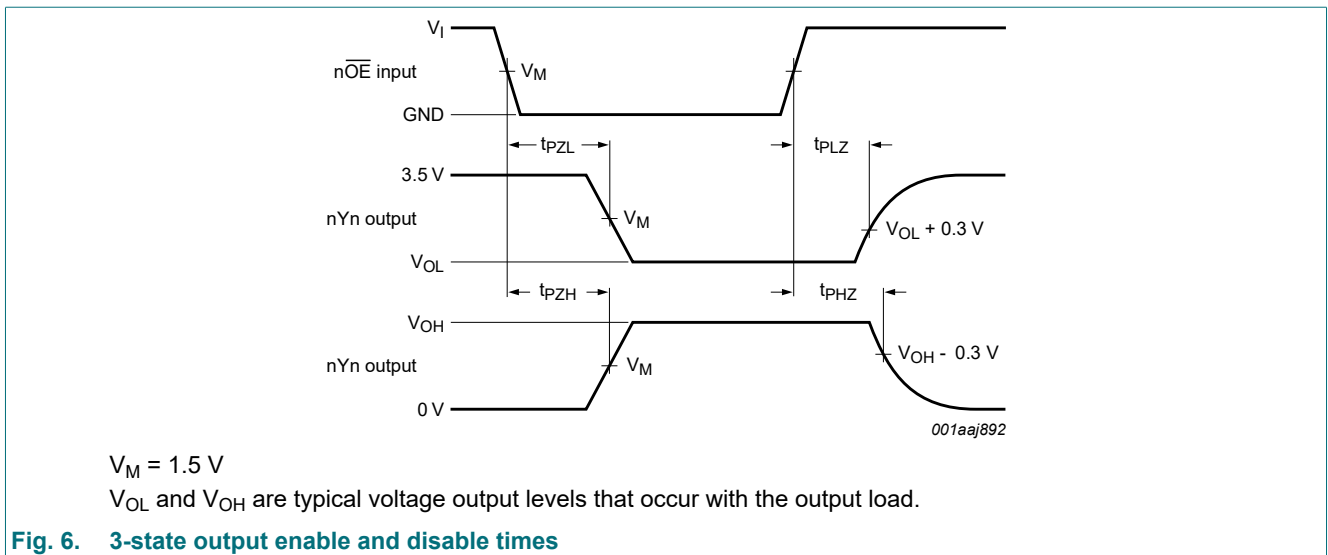
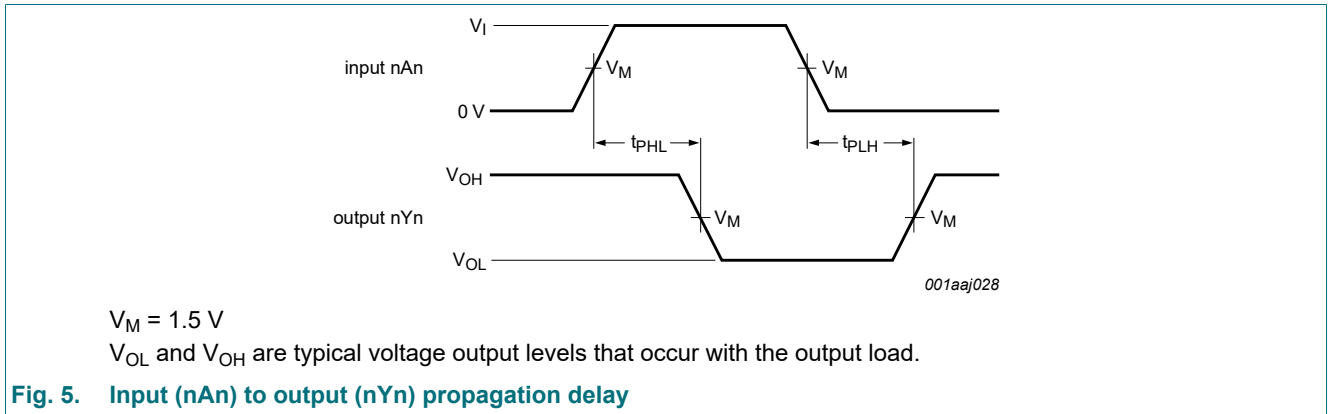
10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V. For test circuit, see Fig. 7.

| Symbol | Parameter | Conditions | 25 °C; V _{CC} = 5.0 V | | | -40 °C to +85 °C; V _{CC} = 5.0 V ± 0.5 V | | Unit |
|------------------|-------------------------------------|--------------------------------------|--------------------------------|-----|-----|--|-----|------|
| | | | Min | Typ | Max | Min | Max | |
| t _{PLH} | LOW to HIGH propagation delay | nAn to nYn, see Fig. 5 | 1.0 | 1.8 | 2.4 | 1.0 | 2.7 | ns |
| t _{PHL} | HIGH to LOW propagation delay | nAn to nYn, see Fig. 5 | 1.6 | 3.2 | 4.0 | 1.6 | 4.4 | ns |
| t _{PZH} | OFF-state to HIGH propagation delay | n \overline{OE} to nYn; see Fig. 6 | 1.2 | 2.7 | 3.5 | 1.2 | 4.3 | ns |
| t _{PZL} | OFF-state to LOW propagation delay | n \overline{OE} to nYn; see Fig. 6 | 2.6 | 5.0 | 6.2 | 2.6 | 7.3 | ns |
| t _{PHZ} | HIGH to OFF-state propagation delay | n \overline{OE} to nYn; see Fig. 6 | 1.5 | 3.0 | 3.8 | 1.5 | 4.5 | ns |
| t _{PLZ} | LOW to OFF-state propagation delay | n \overline{OE} to nYn; see Fig. 6 | 1.3 | 2.6 | 3.3 | 1.3 | 4.6 | ns |

10.1. Waveforms and test circuit



16-bit buffer/line driver with 30 Ω series termination resistors; 3-state

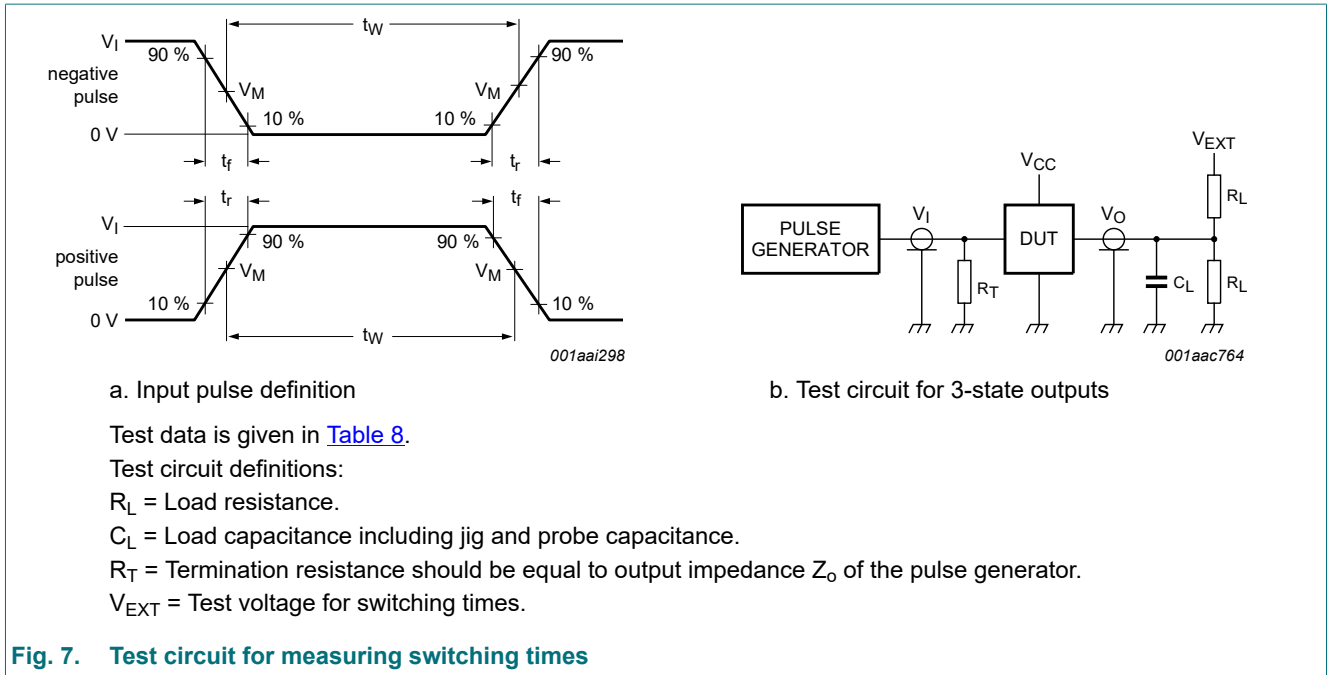


Fig. 7. Test circuit for measuring switching times

Table 8. Test data

| Input | | | | Load | | V_{EXT} | | |
|-------|-------|--------|------------|-------|-------|--------------------|--------------------|--------------------|
| V_I | f_i | t_w | t_r, t_f | C_L | R_L | t_{PHZ}, t_{PZH} | t_{PLZ}, t_{PZL} | t_{PLH}, t_{PHL} |
| 3.0 V | 1 MHz | 500 ns | 2.5 ns | 50 pF | 500 Ω | open | 7.0 V | open |

11. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

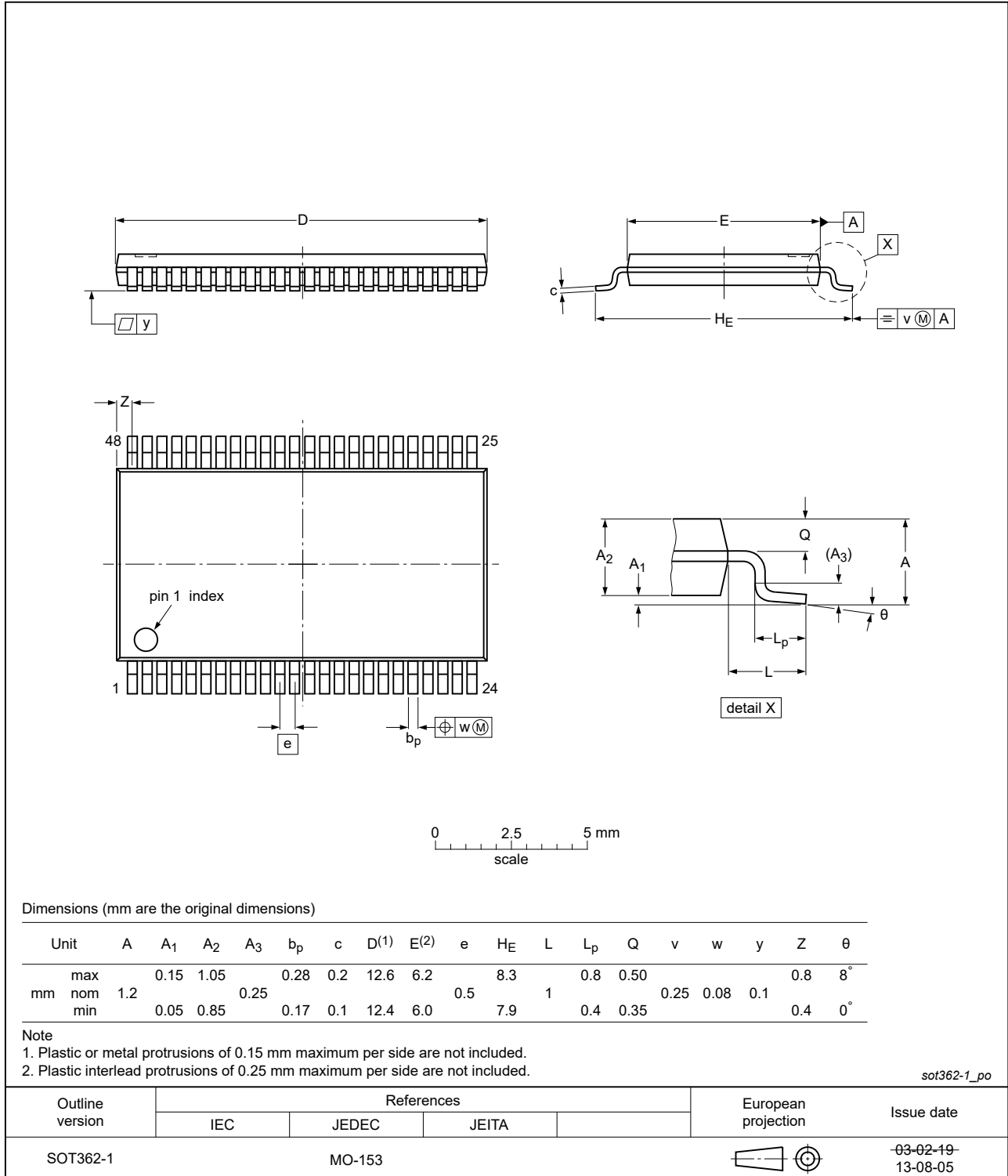


Fig. 8. Package outline SOT362-1 (TSSOP48)

12. Abbreviations

Table 9. Abbreviations

| Acronym | Description |
|---------|---|
| BiCMOS | Bipolar Complementary Metal Oxide Semiconductor |
| CDM | Charged Device Model |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| TTL | Transistor-Transistor Logic |

13. Revision history

Table 10. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-------------------|--|-----------------------|---------------|-------------------|
| 74ABT162244 v.7 | 20210702 | Product data sheet | - | 74ABT162244 v.6 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Fig. 8: Package outline drawing SOT362-1 (TSSOP48) updated. Type number 74ABT162244DL (SOT370-1/SSOP48) removed. Section 1 and Section 2 updated. | | | |
| 74ABT162244 v.6 | 20111103 | Product data sheet | - | 74ABT162244 v.5 |
| Modifications: | <ul style="list-style-type: none"> Legal pages updated | | | |
| 74ABT162244 v.5 | 20100525 | Product data sheet | - | 74ABT162244 v.4 |
| 74ABT162244 v.4 | 20090409 | Product data sheet | - | 74ABT_H162244 v.3 |
| 74ABT_H162244 v.3 | 19981022 | Product specification | - | 74ABT_H162244 v.2 |
| 74ABT_H162244 v.2 | 19980225 | Product specification | - | 74ABT_H162244 v.1 |
| 74ABT_H162244 v.1 | 19961023 | Product specification | - | - |

14. Legal information

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| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

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- [2] The term 'short data sheet' is explained in section "Definitions".
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Contents

| | |
|--|-----------|
| 1. General description | 1 |
| 2. Features and benefits | 1 |
| 3. Ordering information | 1 |
| 4. Functional diagram | 2 |
| 5. Pinning information | 3 |
| 5.1. Pinning..... | 3 |
| 5.2. Pin description..... | 3 |
| 6. Functional description | 4 |
| 7. Limiting values | 4 |
| 8. Recommended operating conditions | 4 |
| 9. Static characteristics | 5 |
| 10. Dynamic characteristics | 6 |
| 10.1. Waveforms and test circuit..... | 6 |
| 11. Package outline | 8 |
| 12. Abbreviations | 9 |
| 13. Revision history | 9 |
| 14. Legal information | 10 |

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