BF909; BF909R

N-channel dual gate MOS-FETs

Rev. 02 — 19 November 2007

Product data sheet

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FEATURES

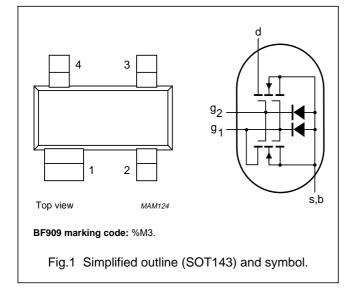
- Specially designed for use at 5 V supply voltage
- · High forward transfer admittance
- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Superior cross-modulation performance during AGC.

APPLICATIONS

 VHF and UHF applications with 3 to 7 V supply voltage such as television tuners and professional communications equipment.

DESCRIPTION

Enhancement type field-effect transistor in a plastic microminiature SOT143 or SOT143R package. The



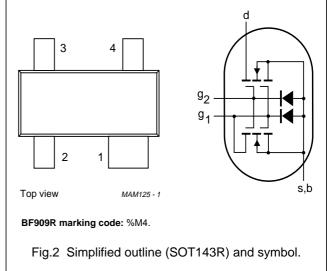
transistor consists of an amplifier MOS-FET with source and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g ₂	gate 2
4	g ₁	gate 1



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{DS}	drain-source voltage		_	_	7	V
I _D	drain current		_	_	40	mA
P _{tot}	total power dissipation		_	_	200	mW
Tj	operating junction temperature		_	_	150	°C
y _{fs}	forward transfer admittance		36	43	50	mS
C _{ig1-s}	input capacitance at gate 1		_	3.6	4.3	pF
C _{rs}	reverse transfer capacitance	f = 1 MHz	_	35	50	fF
F	noise figure	f = 800 MHz	_	2	2.8	dB

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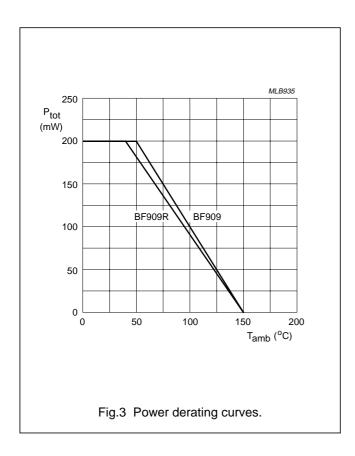
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{DS}	drain-source voltage		_	7	V
I_D	drain current		_	40	mA
I _{G1}	gate 1 current		_	±10	mA
I_{G2}	gate 2 current		_	±10	mA
P _{tot}	total power dissipation	see Fig.3			
	BF909	up to $T_{amb} = 50 ^{\circ}C$; note 1	_	200	mW
	BF909R	up to $T_{amb} = 40 ^{\circ}C$; note 1	_	200	mW
T _{stg}	storage temperature		-65	+150	°C
T _j	operating junction temperature		_	150	°C

Note

1. Device mounted on a printed-circuit board.



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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th j-a}	thermal resistance from junction to ambient	note 1		
	BF909		500	K/W
	BF909R		550	K/W
R _{th j-s}	thermal resistance from junction to soldering point	note 2		
	BF909	T _s = 92 °C	290	K/W
	BF909R	T _s = 78 °C	360	K/W

Notes

- 1. Device mounted on a printed-circuit board.
- 2. T_s is the temperature at the soldering point of the source lead.

STATIC CHARACTERISTICS

 T_i = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{(BR)G1-SS}	gate 1-source breakdown voltage	$V_{G2-S} = V_{DS} = 0$; $I_{G1-S} = 10 \text{ mA}$	6	15	V
V _{(BR)G2-SS}	gate 2-source breakdown voltage	$V_{G1-S} = V_{DS} = 0$; $I_{G2-S} = 10 \text{ mA}$	6	15	V
V _{(F)S-G1}	forward source-gate 1 voltage	$V_{G2-S} = V_{DS} = 0$; $I_{S-G1} = 10 \text{ mA}$	0.5	1.5	V
V _{(F)S-G2}	forward source-gate 2 voltage	$V_{G1-S} = V_{DS} = 0$; $I_{S-G2} = 10 \text{ mA}$	0.5	1.5	V
V _{G1-S(th)}	gate 1-source threshold voltage	$V_{G2-S} = 4 \text{ V}; V_{DS} = 5 \text{ V};$ $I_D = 20 \mu A$	0.3	1	V
V _{G2-S(th)}	gate 2-source threshold voltage	$V_{G1-S} = V_{DS} = 5 \text{ V}; I_D = 20 \mu\text{A}$	0.3	1.2	V
I _{DSX}	drain-source current	$V_{G2-S} = 4 \text{ V}; V_{DS} = 5 \text{ V};$ $R_{G1} = 120 \text{ k}\Omega; \text{ note 1}$	12	20	mA
I _{G1-SS}	gate 1 cut-off current	V _{G1-S} = 5 V; V _{G2-S} = V _{DS} = 0	_	50	nA
I _{G2-SS}	gate 2 cut-off current	$V_{G2-S} = 5 \text{ V}; V_{G1-S} = V_{DS} = 0$	_	50	nA

Note

1. R_{G1} connects gate 1 to V_{GG} = 5 V; see Fig.18.

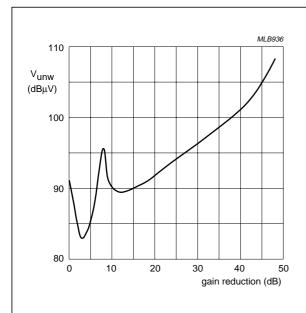
DYNAMIC CHARACTERISTICS

Common source; T_{amb} = 25 °C; V_{DS} = 5 V; V_{G2-S} = 4 V; I_D = 15 mA; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
y _{fs}	forward transfer admittance	pulsed; T _j = 25 °C	36	43	50	mS
C _{ig1-s}	input capacitance at gate 1	f = 1 MHz	_	3.6	4.3	pF
C _{ig2-s}	input capacitance at gate 2	f = 1 MHz	_	2.3	3	pF
Cos	drain-source capacitance	f = 1 MHz	_	2.3	3	pF
C _{rs}	reverse transfer capacitance	f = 1 MHz	_	35	50	fF
F	noise figure	$f = 800 \text{ MHz}; G_S = G_{Sopt}; B_S = B_{Sopt}$	_	2	2.8	dB

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 $V_{DS} = 5 \text{ V; } V_{GG} = 5 \text{ V; } f_w = 50 \text{ MHz.}$ $f_{unw} = 60 \text{ MHz; } T_{amb} = 25 \text{ °C; } R_{G1} = 120 \text{ k}\Omega.$

Fig.4 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values; see Fig.18.

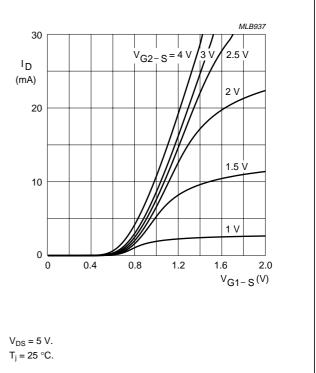
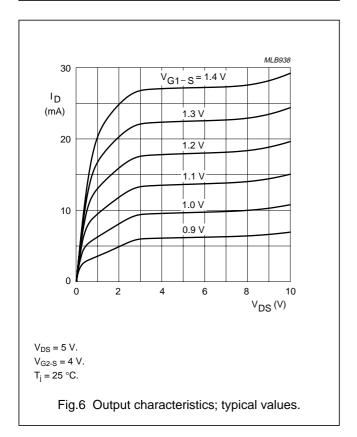
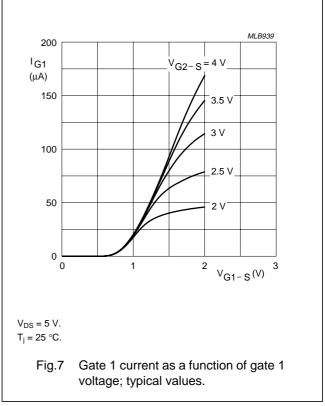
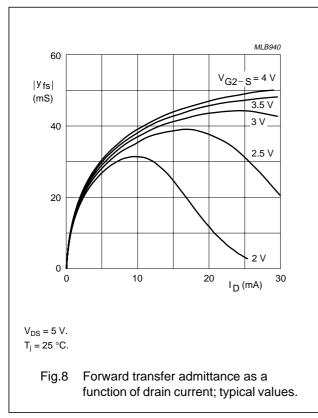


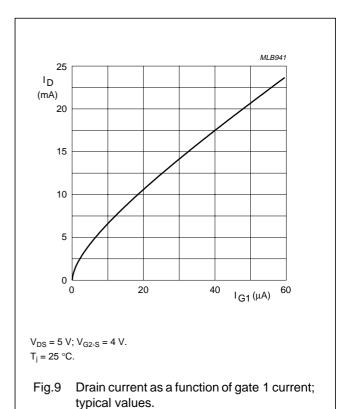
Fig.5 Transfer characteristics; typical values.

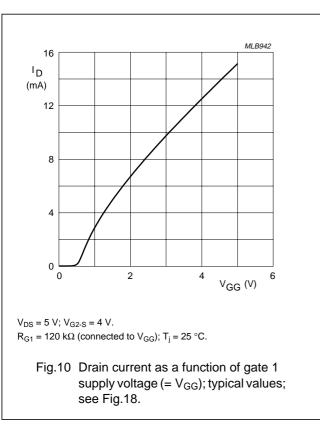


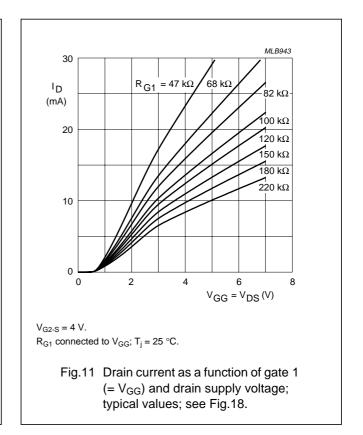


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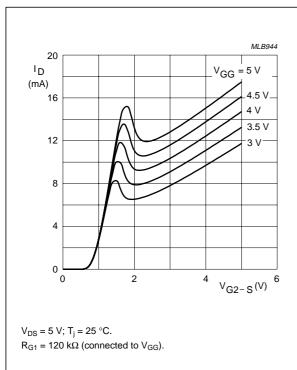
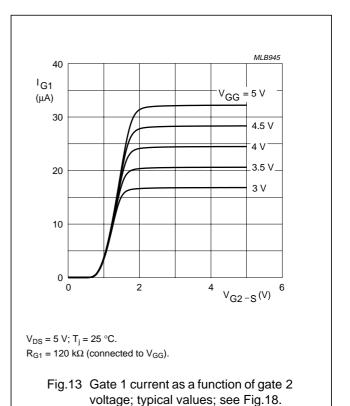
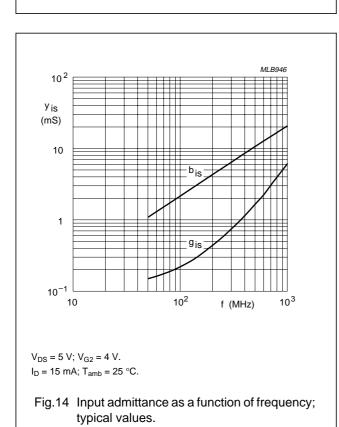
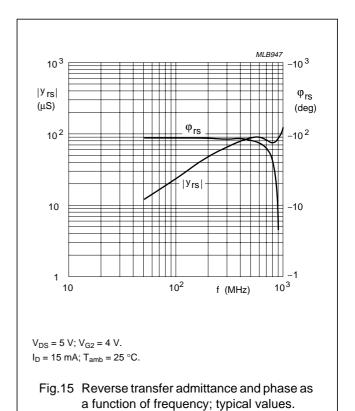


Fig.12 Drain current as a function of gate 2 voltage; typical values; see Fig.18.







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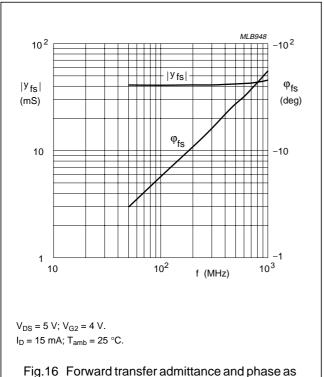


Fig.16 Forward transfer admittance and phase as a function of frequency; typical values.

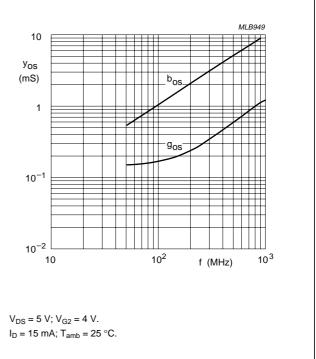
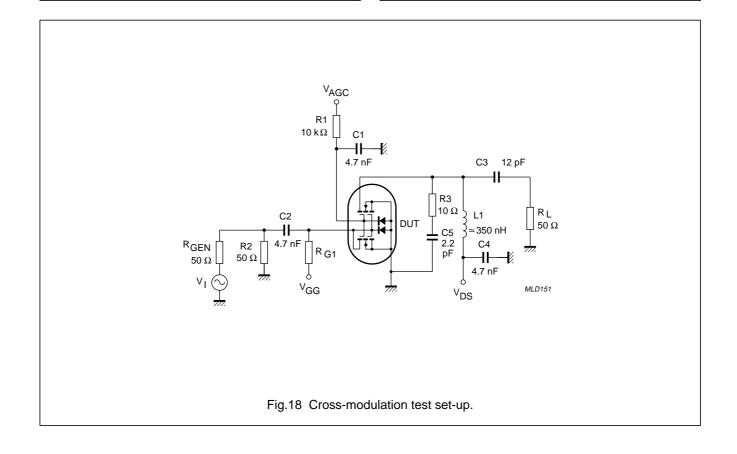


Fig.17 Output admittance as a function of frequency; typical values.



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Table 1 Scattering parameters: $T_{amb} = 25 \, ^{\circ}C$; $V_{DS} = 5 \, V$; $V_{G2-S} = 4 \, V$; $I_D = 15 \, mA$

4	S ₁₁		S ₂₁ S ₁₂		s ₁₂		S ₂₂	
(MHz)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.985	-6.4	4.064	172.3	0.001	86.9	0.985	-3.2
100	0.978	-12.6	3.997	164.9	0.002	82.7	0.982	-6.4
200	0.957	-25.0	3.886	150.8	0.005	74.3	0.973	-12.6
300	0.931	-36.5	3.682	137.3	0.006	68.9	0.960	-18.6
400	0.899	-47.6	3.484	123.8	0.007	59.6	0.947	-24.2
500	0.868	-57.4	3.260	111.7	0.007	57.9	0.936	-29.6
600	0.848	-66.6	3.053	101.0	0.006	58.5	0.927	-34.8
700	0.816	-74.6	2.829	90.3	0.005	65.5	0.919	-39.8
800	0.792	-82.2	2.652	79.9	0.005	83.3	0.913	-44.6
900	0.772	-89.3	2.470	69.5	0.005	114.9	0.910	-49.5
1000	0.754	-95.6	2.328	59.5	0.006	138.7	0.909	-54.6

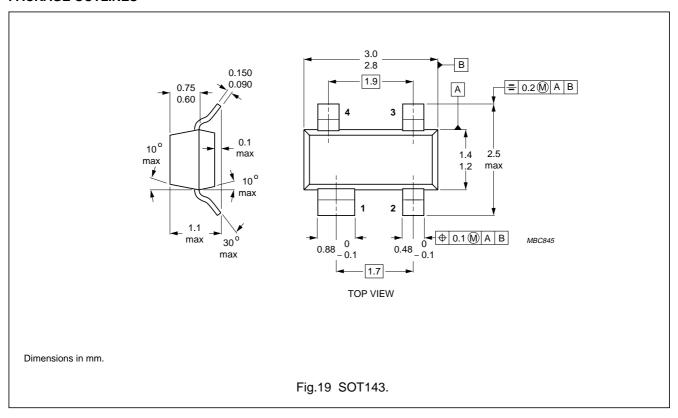
Table 2 Noise data: T_{amb} = 25 °C; V_{DS} = 5 V; V_{G2-S} = 4 V; I_D = 15 mA

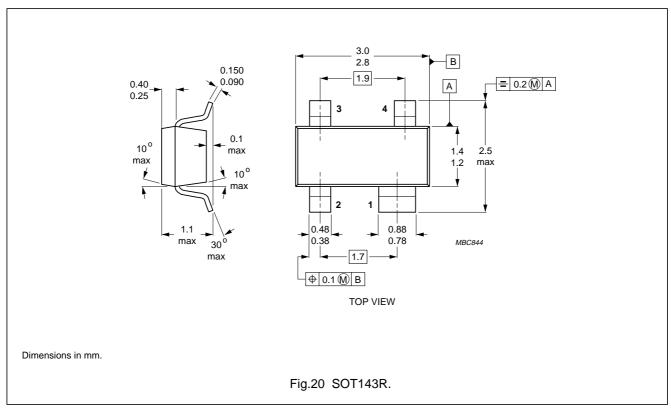
f	F _{min}	$\Gamma_{ extsf{opt}}$		
(MHz)	(dB)	(ratio)	(deg)	'n
800	2.00	0.603	67.71	0.581

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PACKAGE OUTLINES





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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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Revision history

Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BF909_N_2	20071119	Product data sheet	-	BF909_1
Modifications:	• Fig.1 and 2	on page 2; Figure note change	ed	
BF909_1	19950425	Product specification	-	-



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