Document Number: AFT26H200W03S
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VRoHS

RF Power LDMOS Transistor

N–Channel Enhancement–Mode Lateral MOSFET

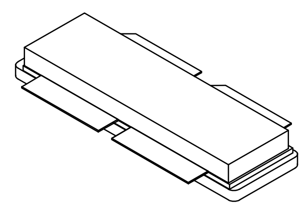
AFT26H200W03SR6

This 45 watt asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 2496 to 2690 MHz.

- Typical Doherty Single–Carrier W–CDMA Performance: V_{DD} = 28 Volts, I_{DQA} = 500 mA, V_{GSB} = 0.3 Vdc, P_{out} = 45 Watts Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
2496 MHz	14.1	45.2	7.8	–31.1
2590 MHz	14.2	44.0	7.8	–35.6
2690 MHz	13.9	44.1	7.6	–37.5

2496–2690 MHz, 45 W AVG., 28 V AIRFAST RF POWER LDMOS TRANSISTOR



NI–1230S–4S

Features

- Advanced High Performance In–Package Doherty
- Designed for Wide Instantaneous Bandwidth Applications
- Greater Negative Gate–Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- In Tape and Reel. R6 Suffix = 150 Units, 56 mm Tape Width, 13–inch Reel.

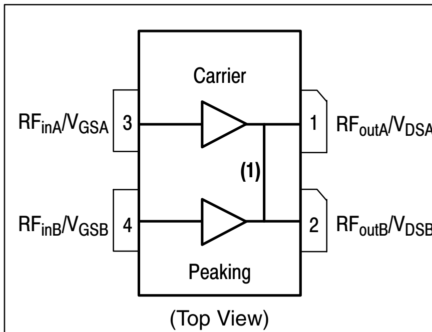


Figure 1. Pin Connections

1. Pin connections 1 and 2 are DC coupled and RF independent.

freescale Airfast

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate–Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +125	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 76°C, 45 W–CDMA, 28 Vdc, I_{DQA} = 500 mA, V_{GSB} = 0.3 Vdc, 2590 MHz	$R_{\theta JC}$	0.46	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22–A114)	2
Machine Model (per EIA/JESD22–A115)	B
Charge Device Model (per JESD22–C101)	III

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

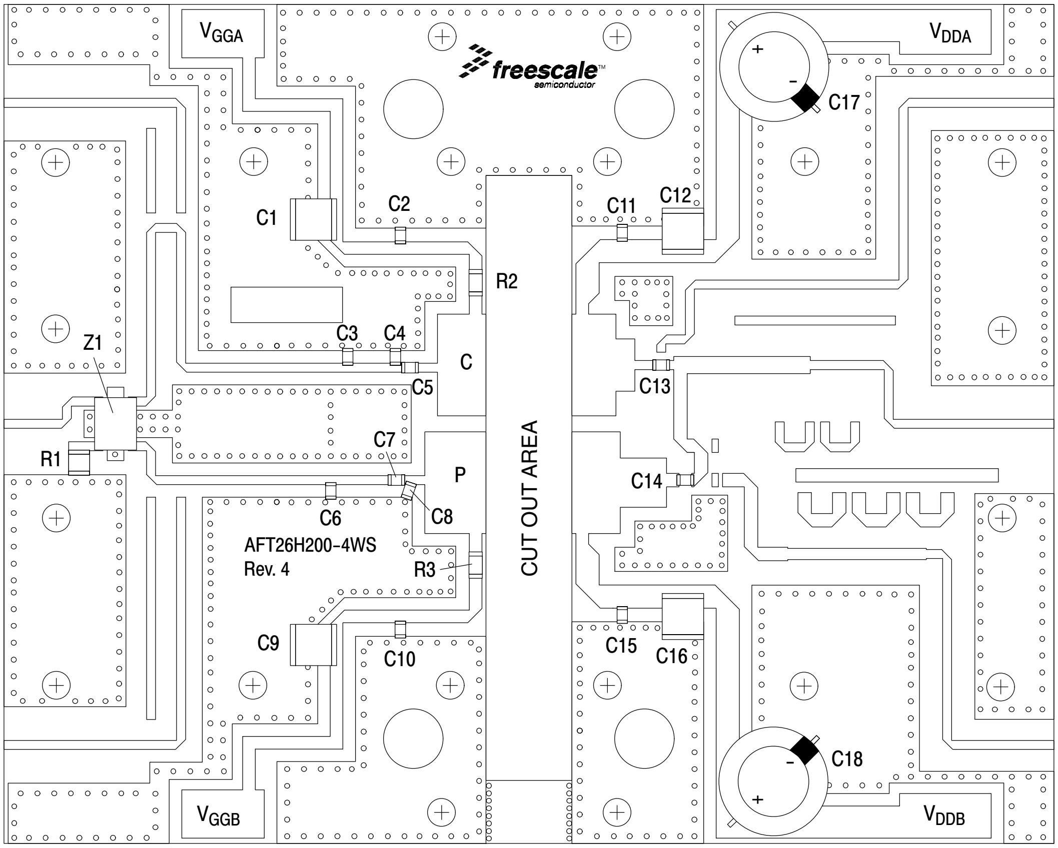
Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (4)					
Zero Gate Voltage Drain Leakage Current (5) (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (5) (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	5	μAdc
Gate–Source Leakage Current (6) (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics – Side A (4,6) (Carrier)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 100 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DA} = 500 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	1.4	1.8	2.2	Vdc
Drain–Source On–Voltage (V_{GS} = 6 Vdc, I_D = 1.0 Adc)	$V_{DS(on)}$	0.1	0.15	0.3	Vdc
On Characteristics – Side B (4,6) (Peaking)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 180 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Drain–Source On–Voltage (V_{GS} = 6 Vdc, I_D = 1.8 Adc)	$V_{DS(on)}$	0.1	0.15	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes – AN1955.
4. V_{DDA} and V_{DDB} must be tied together and powered by a single DC power supply.
5. Side A and Side B are tied together for these measurements.
6. Each side of device measure separately.

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests [1,2,3] (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 500 mA, V_{GSB} = 0.3 Vdc, P_{out} = 45 W Avg., f = 2496 MHz, Single–Carrier W–CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	13.0	14.1	16.0	dB
Drain Efficiency	η_D	42.0	45.2	—	%
Output Peak–to–Average Ratio @ 0.01% Probability on CCDF	PAR	7.5	7.8	—	dB
Adjacent Channel Power Ratio	ACPR	—	–31.1	–28.0	dBc
Load Mismatch (In Freescale Test Fixture, 50 ohm system) I_{DQA} = 500 mA, V_{GSB} = 0.3 Vdc, f = 2590 MHz, 10 μsec Pulse Width, 10% Duty Cycle, <100 ns Input Rise Time					
VSWR 10:1 at 30 Vdc, 280 W Pulse Output Power (3 dB Input Overdrive from 250 W Pulse Rated Power)	No Device Degradation				
Typical Performances [3] (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 500 mA, V_{GSB} = 0.3 Vdc, 2496–2690 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	200	—	W
P_{out} @ 3 dB Compression Point [4]	P3dB	—	280	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2496–2690 MHz frequency range)	Φ	—	–13	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	220	—	MHz
Gain Flatness in 194 MHz Bandwidth @ P_{out} = 45 W Avg.	G_F	—	0.3	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.019	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.0377	—	dB/°C

1. V_{DDA} and V_{DDB} must be tied together and powered by a single DC power supply.
2. Part internally matched both on input and output.
3. Measurements made with device in an asymmetrical Doherty configuration.
4. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W–CDMA single–carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.



Note: V_{DDA} and V_{DDB} must be tied together and powered by a single DC power supply.

Figure 2. AFT26H200W03SR6 Test Circuit Component Layout

Table 5. AFT26H200W03SR6 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C9, C12, C16	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C2, C5, C7, C10, C11, C14, C15	6.8 pF Chip Capacitors	ATC600F6R8BT250XT	ATC
C3, C4	0.7 pF Chip Capacitors	ATC600F0R7BT250XT	ATC
C6, C8	0.5 pF Chip Capacitors	ATC600F0R5BT250XT	ATC
C13	2.0 pF Chip Capacitor	ATC600F2R0BT250XT	ATC
C17, C18	220 μF, 50 V Electrolytic Capacitors	227CKS050M	Illinois Capacitor
R1	50 Ω, 4 W Chip Resistor	CW12010T0050GBK	ATC
R2, R3	3.0 Ω, 1/4 W Chip Resistors	CRCW12063R00FNEA	Vishay
Z1	2300–2700 MHz, 5 dB, Directional Coupler	X3C25P1-05S	Anaren
PCB	0.020″, ε_r = 3.5	RO4350B	Rogers

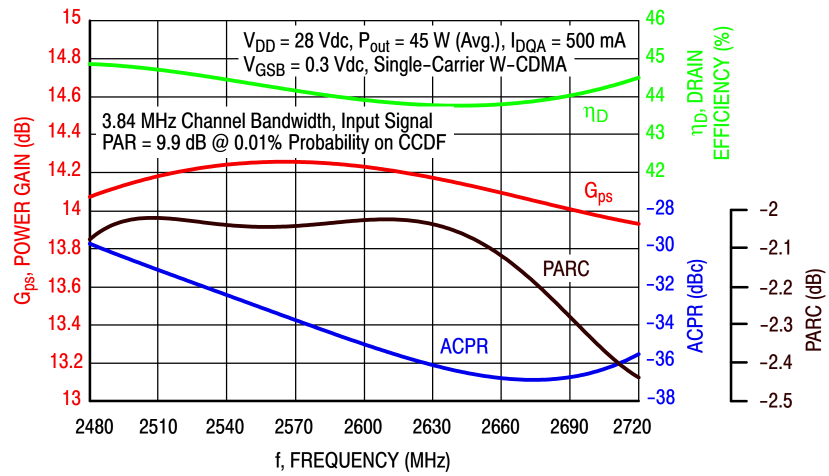


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 45 Watts Avg.

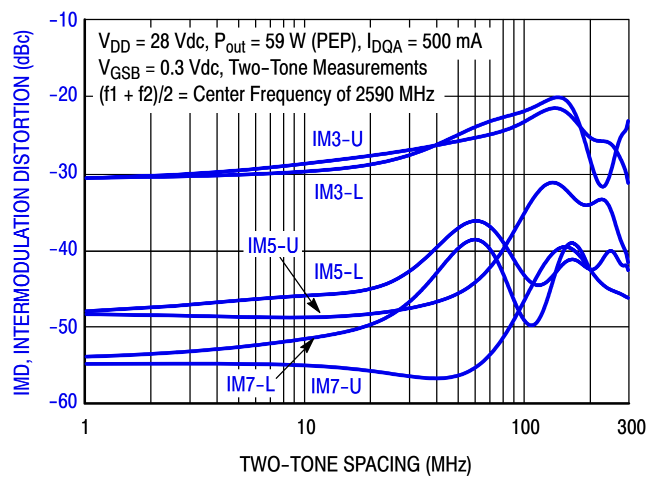


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

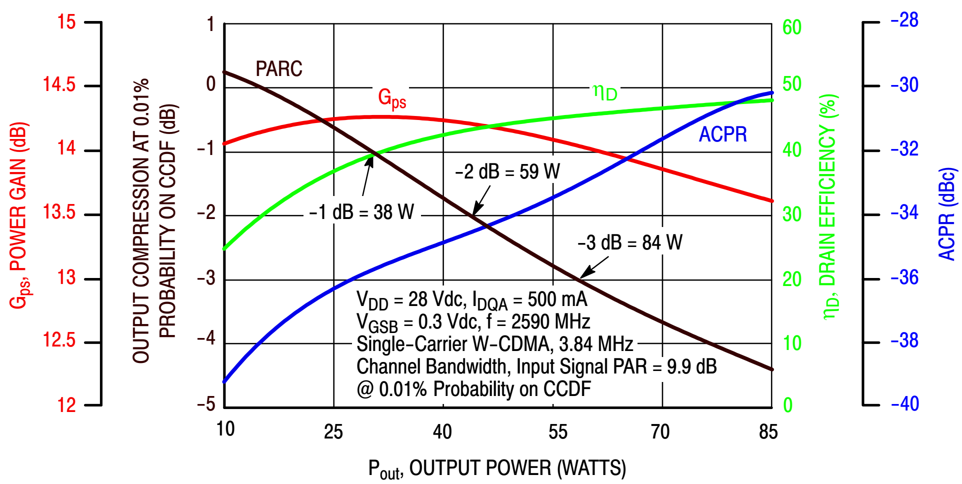


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

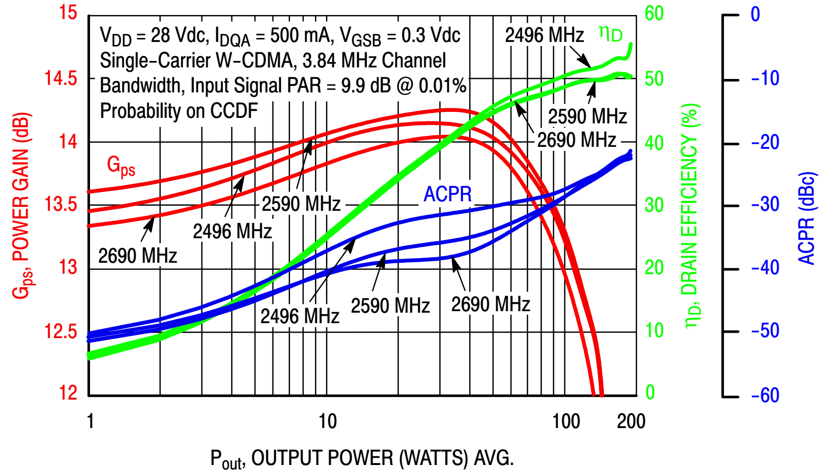


Figure 6. Single−Carrier W−CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

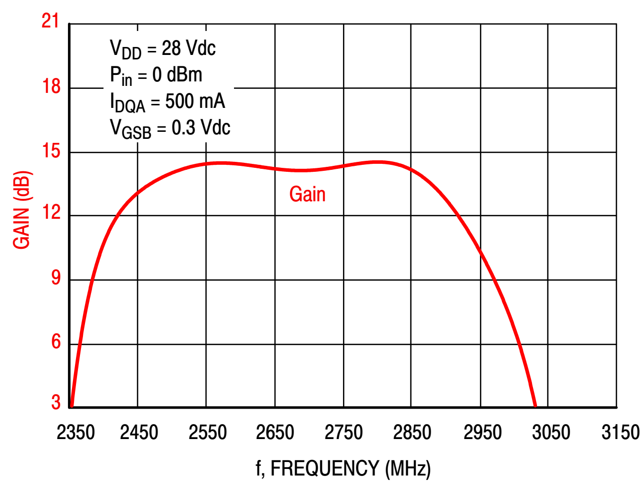


Figure 7. Broadband Frequency Response

V_{DD} = 28 Vdc, I_{DQA} = 494 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB					
			Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	9.09 - j14.0	8.87 + j13.4	4.40 - j8.11	17.3	50.3	107	53.1	-12
2590	16.1 - j13.2	15.2 + j12.7	4.32 - j8.14	17.5	50.3	107	53.6	-13
2690	22.9 - j0.41	20.5 + j1.37	4.28 - j8.80	17.5	50.2	104	52.2	-13

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB					
			Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	9.09 - j14.0	9.41 + j14.6	4.15 - j8.72	15.1	51.0	127	53.7	-17
2590	16.1 - j13.2	17.5 + j13.6	4.16 - j8.90	15.2	51.0	127	53.7	-18
2690	22.9 - j0.41	22.2 - j1.34	4.21 - j9.41	15.2	50.9	123	52.3	-18

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 8. Carrier Side Load Pull Performance — Maximum Power Tuning

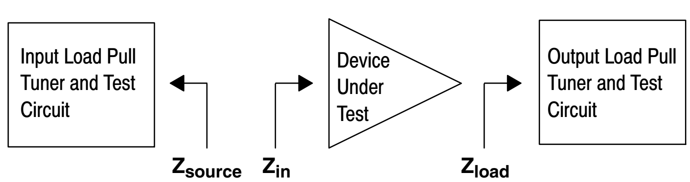
V_{DD} = 28 Vdc, I_{DQA} = 494 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB					
			Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	9.09 - j14.0	8.65 + j14.2	9.14 - j5.50	19.4	48.7	74	63.1	-20
2590	16.1 - j13.2	15.2 + j14.1	7.18 - j4.60	19.5	48.8	74	63.2	-21
2690	22.9 - j0.41	22.1 + j2.44	6.06 - j4.93	19.5	48.7	74	61.6	-21

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB					
			Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	9.09 - j14.0	8.89 + j15.2	8.01 - j6.15	17.1	49.8	95	63.7	-26
2590	16.1 - j13.2	17.2 + j15.2	6.92 - j5.30	17.3	49.6	92	63.4	-27
2690	22.9 - j0.41	23.6 - j0.47	6.02 - j6.43	17.0	49.9	98	61.6	-25

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 9. Carrier Side Load Pull Performance — Maximum Drain Efficiency Tuning



V_{DD} = 28 Vdc, V_{GSB} = 0.3 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P1dB					
			Z_{load} [(1)] (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	5.24 - j10.6	5.15 + j9.87	2.61 - j5.59	11.6	52.6	181	52.5	-19
2590	10.3 - j9.81	9.38 + j9.30	2.63 - j5.84	12.0	52.5	176	51.9	-20
2690	12.7 - j0.94	12.0 + j1.20	2.68 - j6.10	12.3	52.1	164	49.8	-20

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P3dB					
			Z_{load} [(2)] (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	5.24 - j10.6	5.51 + j10.5	2.57 - j5.91	9.4	53.2	211	52.7	-25
2590	10.3 - j9.81	10.7 + j9.63	2.68 - j6.12	9.4	53.1	205	52.3	-25
2690	12.7 - j0.94	12.2 - j0.26	2.79 - j6.48	10.2	52.8	190	49.7	-25

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 10. Peaking Side Load Pull Performance — Maximum Power Tuning

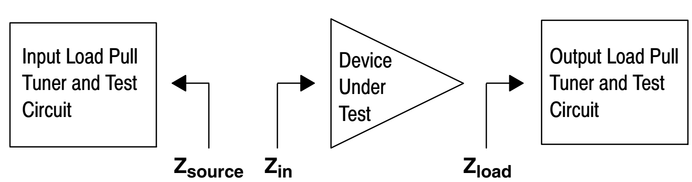
V_{DD} = 28 Vdc, V_{GSB} = 0.3 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P1dB					
			Z_{load} [(1)] (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	5.24 - j10.6	4.66 + j10.2	5.91 - j4.19	12.8	51.1	129	61.3	-27
2590	10.3 - j9.81	8.53 + j10.5	4.92 - j2.75	13.2	50.6	116	61.2	-30
2690	12.7 - j0.94	13.2 + j3.53	3.52 - j2.21	13.1	49.7	93	59.0	-35

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P3dB					
			Z_{load} [(2)] (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	5.24 - j10.6	5.08 + j10.8	5.29 - j4.65	10.7	52.0	160	61.9	-34
2590	10.3 - j9.81	10.2 + j10.5	4.64 - j4.15	11.1	52.0	158	61.2	-34
2690	12.7 - j0.94	13.3 + j1.00	3.85 - j3.19	11.2	51.0	127	58.2	-38

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 11. Peaking Side Load Pull Performance — Maximum Drain Efficiency Tuning



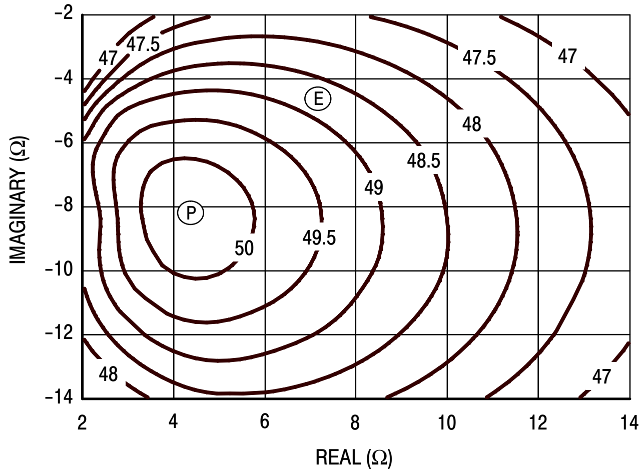


Figure 12. P1dB Load Pull Output Power Contours (dBm)

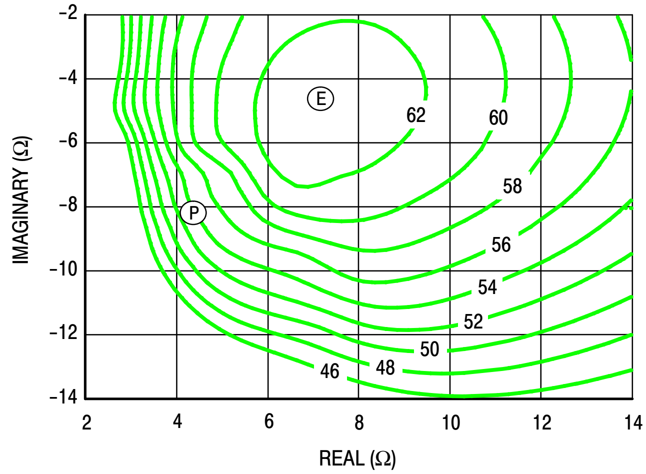


Figure 13. P1dB Load Pull Efficiency Contours (%)

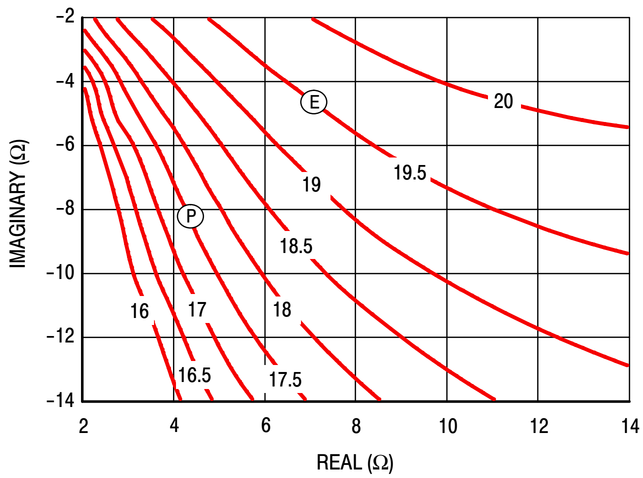


Figure 14. P1dB Load Pull Gain Contours (dB)

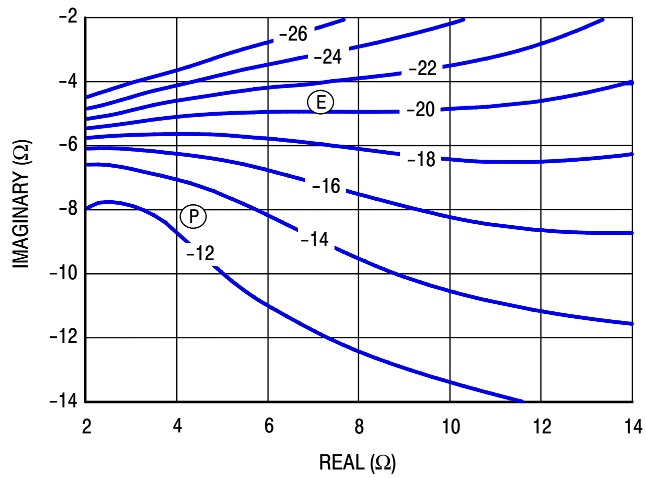


Figure 15. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Power Gain
Drain Efficiency
Linearity
Output Power

P3dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 2590 MHz

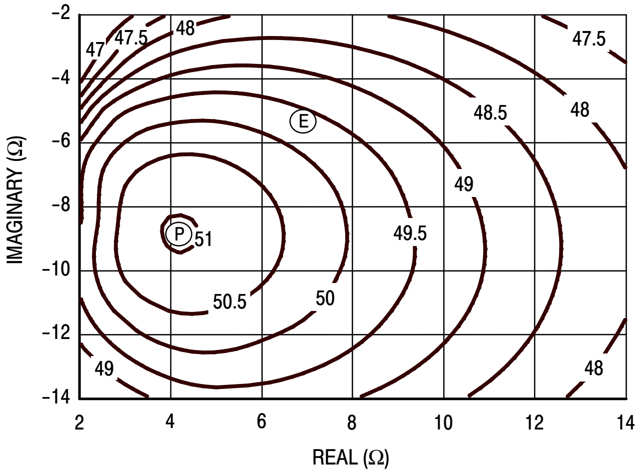


Figure 16. P3dB Load Pull Output Power Contours (dBm)

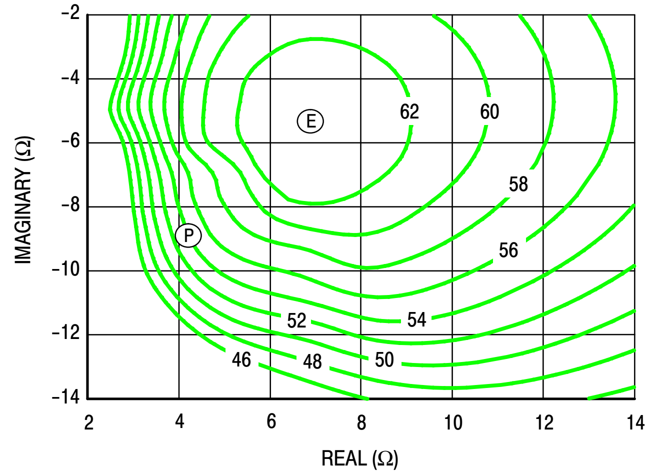


Figure 17. P3dB Load Pull Efficiency Contours (%)

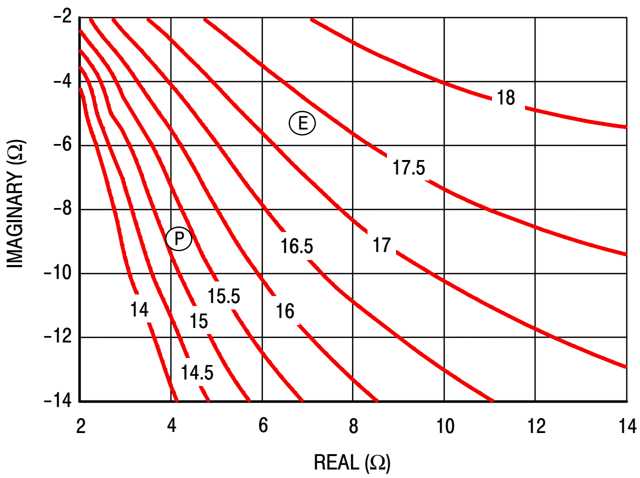


Figure 18. P3dB Load Pull Gain Contours (dB)

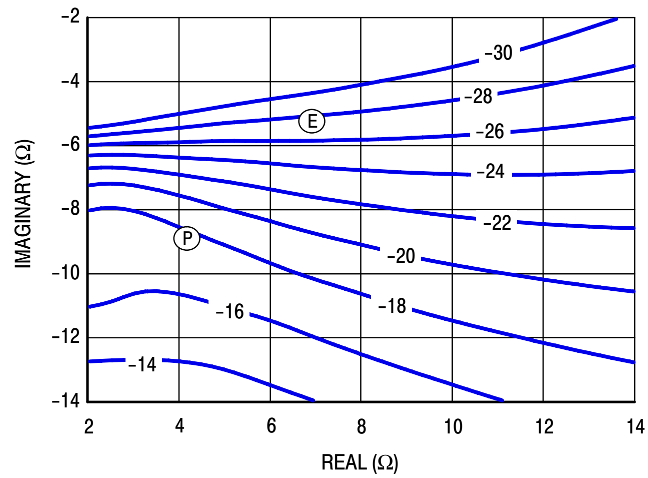


Figure 19. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power

(E) = Maximum Drain Efficiency

- Power Gain
- Drain Efficiency
- Linearity
- Output Power

P1dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 2590 MHz

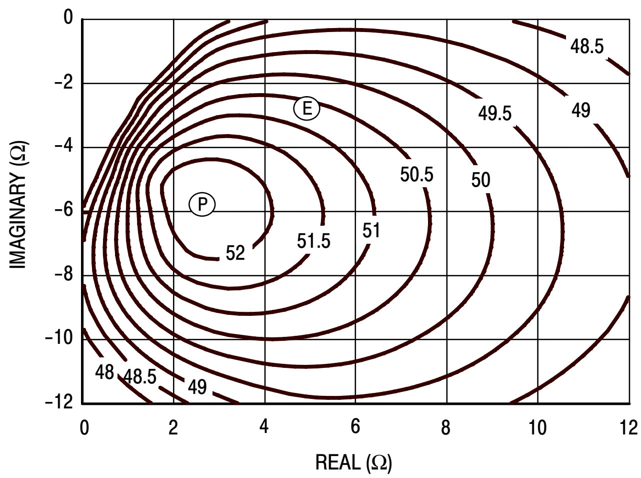


Figure 20. P1dB Load Pull Output Power Contours (dBm)

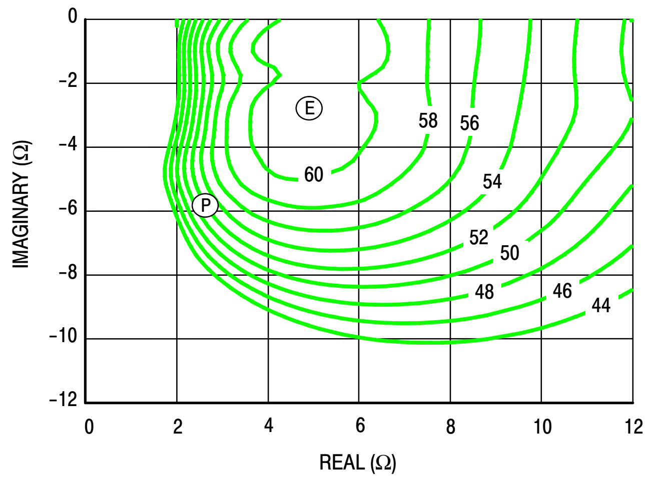


Figure 21. P1dB Load Pull Efficiency Contours (%)

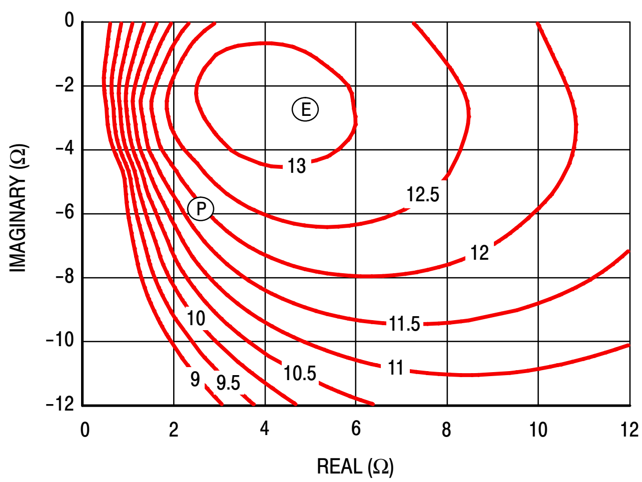


Figure 22. P1dB Load Pull Gain Contours (dB)

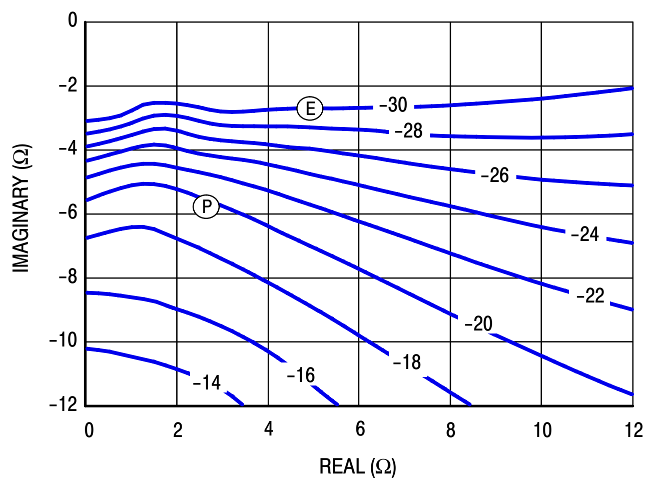


Figure 23. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Power Gain
Drain Efficiency
Linearity
Output Power

P3dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 2590 MHz

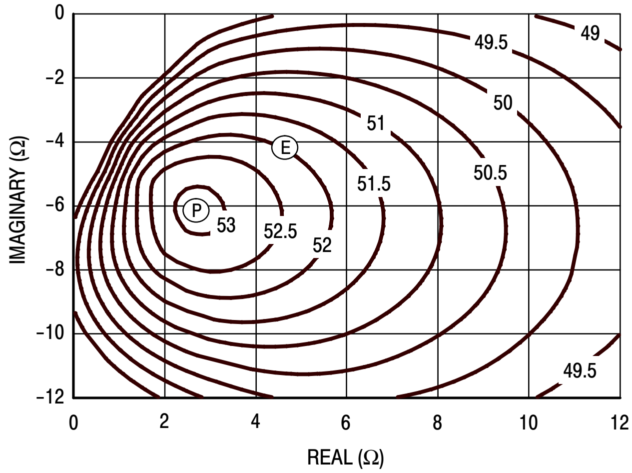


Figure 24. P3dB Load Pull Output Power Contours (dBm)

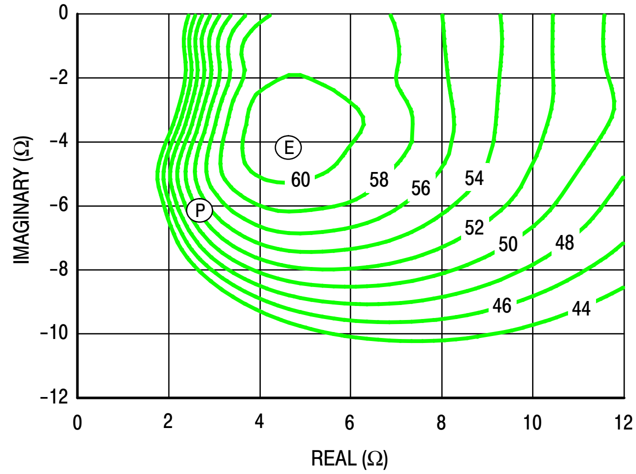


Figure 25. P3dB Load Pull Efficiency Contours (%)

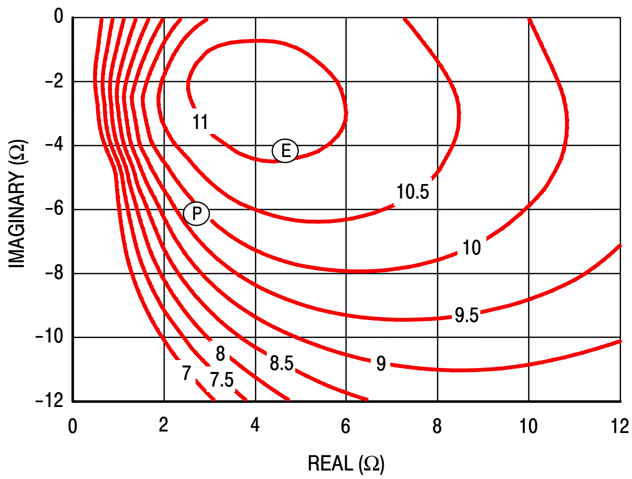


Figure 26. P3dB Load Pull Gain Contours (dB)

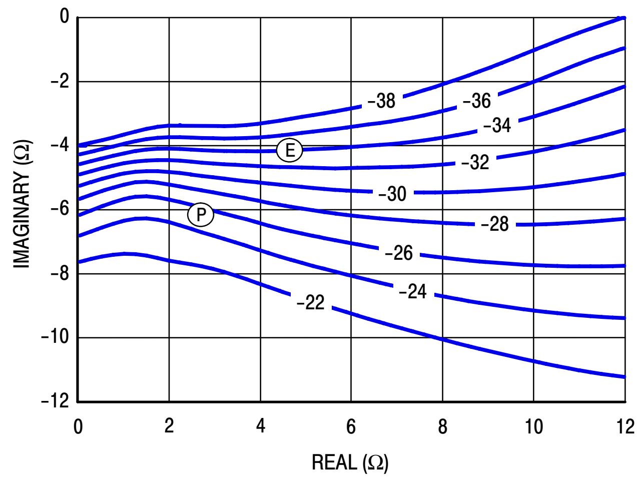


Figure 27. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

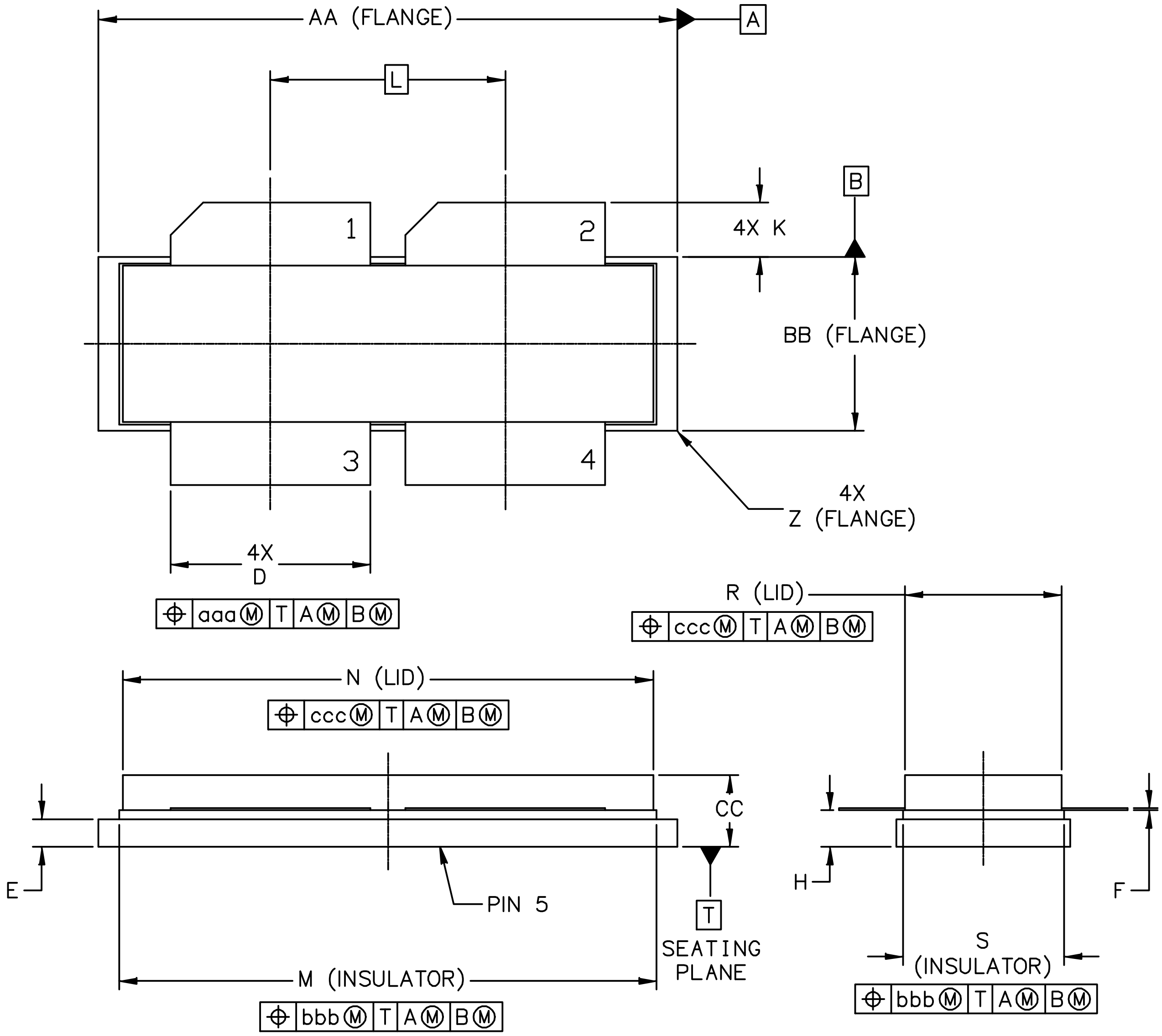
Power Gain

Drain Efficiency

Linearity

Output Power

PACKAGE DIMENSIONS



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NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

2. CONTROLLING DIMENSION: INCH

3. DIMENSION H IS MEASURED .030 INCH (0.762 MM) AWAY FROM PACKAGE BODY

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
AA	1.265	1.275	32.13	32.39	R	.355	.365	9.02	9.27
BB	.395	.405	10.03	10.29	S	.365	.375	9.27	9.53
CC	.170	.190	4.32	4.83	Z	R.000	R.040	R0.00	R1.02
D	.455	.465	11.56	11.81					
E	.062	.066	1.57	1.68	aaa	.013		0.33	
F	.004	.007	0.10	0.18	bbb	.010		0.25	
H	.082	.090	2.08	2.29	ccc	.020		0.51	
K	.117	.137	2.97	3.48					
L	.540 BSC		13.72 BSC						
M	1.219	1.241	30.96	31.52					
N	1.218	1.242	30.94	31.55					

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following documents, software and tools to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the "Part Number" link. Go to the Software & Tools tab on the part's Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Aug. 2013	• Initial Release of Data Sheet

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