

BLL1214-35

L-band radar LDMOS driver transistor

Rev. 2 — 1 September 2015

AMPLEON

Product data sheet

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Thank you for your cooperation and understanding,

Ampleon

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FEATURES

- High power gain
- Easy power control
- Excellent ruggedness
- Source on mounting base eliminates DC isolators, reducing common mode inductance.

APPLICATIONS

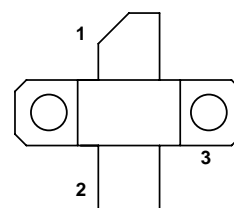
- L-band radar applications in the 1200 to 1400 MHz frequency range.

DESCRIPTION

Silicon N-channel enhancement mode lateral D-MOS transistor encapsulated in a 2-lead flange package (SOT467C) with a ceramic cap. The common source is connected to the flange.

PINNING - SOT467C

PIN	DESCRIPTION
1	drain
2	gate
3	source, connected to flange



Top view MBK584

Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at $T_h = 25\text{ °C}$ in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
Pulsed class-AB; $t = 1\text{ ms}$; $\delta = 10\%$	1200 to 1400	36	35	>13	>43

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	75	V
V_{GS}	gate-source voltage		–	± 15	V
P_{tot}	total power dissipation	under RF conditions; $T_h \leq 25\text{ °C}$	–	110	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	200	°C

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$Z_{th\ j-h}$	thermal impedance from junction to heatsink	$T_h = 25\text{ °C}$; note 1	1.1	K/W

Note

1. Thermal resistance is determined under RF operating conditions; $t_p = 1\text{ ms}$, $\delta = 10\%$.

CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = 0.7\text{ mA}$	75	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 70\text{ mA}$	4.5	–	5.5	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0$; $V_{DS} = 36\text{ V}$	–	–	10	μA
I_{DSX}	on-state drain current	$V_{GS} = V_{GSth} + 9\text{ V}$; $V_{DS} = 10\text{ V}$	10	–	–	A
I_{GSS}	gate leakage current	$V_{GS} = \pm 20\text{ V}$; $V_{DS} = 0$	–	–	125	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}$; $I_D = 2.5\text{ A}$	–	2	–	S
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 2.5\text{ A}$	–	300	–	$\text{m}\Omega$

APPLICATION INFORMATION

RF performance in a common source class-AB circuit. $T_h = 25\text{ °C}$; $Z_{th\ mb-h} = 0.65\text{ K/W}$, unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
Pulsed class-AB; $t = 1\text{ ms}$; $\delta = 10\%$	1200 to 1400	36	50	35	>13	>43

Ruggedness in class-AB operation

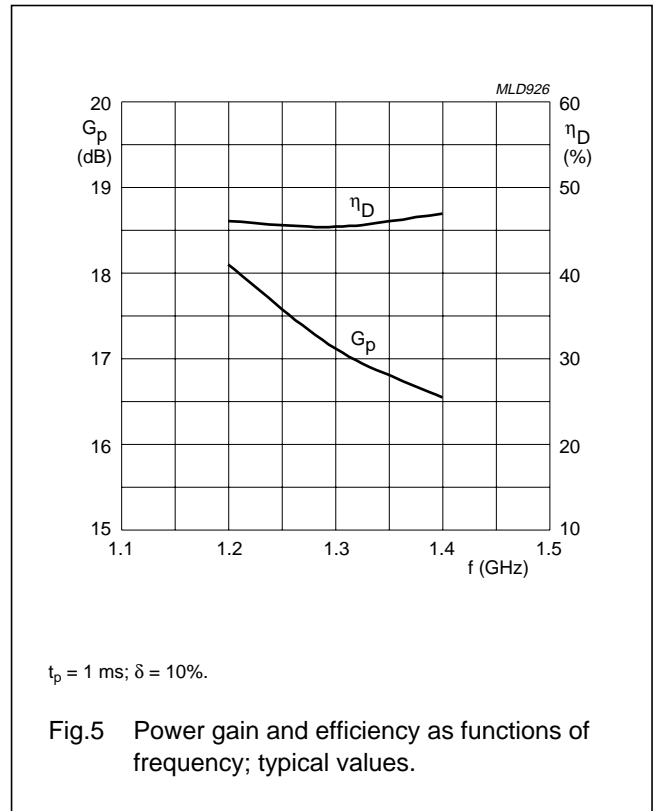
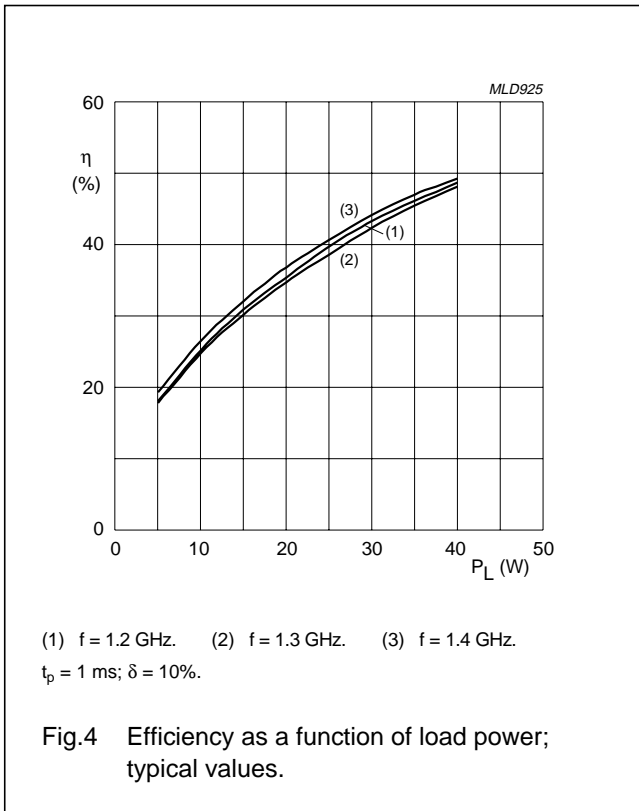
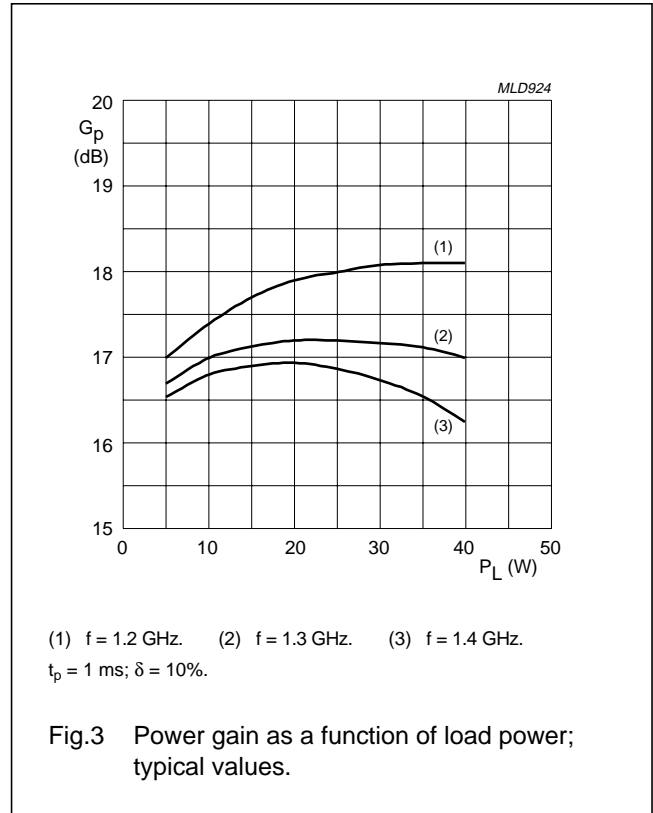
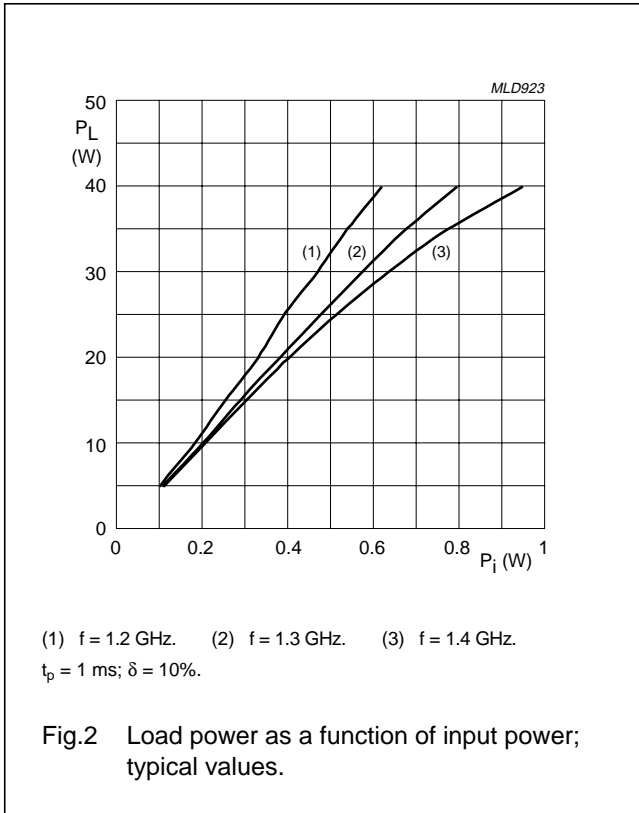
The BLL1214-35 is capable of withstanding a load mismatch corresponding to $VSWR = 5 : 1$ through all phases under the following conditions: $V_{DS} = 36\text{ V}$; frequency from 1200 MHz to 1400 MHz at rated load power.

Typical impedance

FREQUENCY (GHZ)	Z_s (Ω)	Z_L (Ω)
1.20	$6.48 - j\ 3.9$	$1.95 + j\ 3.27$
1.25	$3.88 - j\ 3.2$	$1.90 + j\ 2.57$
1.30	$3.28 - j\ 2.4$	$2.01 + j\ 2.27$
1.35	$2.55 - j\ 1.48$	$2.20 + j\ 2.26$
1.40	$1.69 - j\ 0.51$	$1.72 + j\ 2.35$

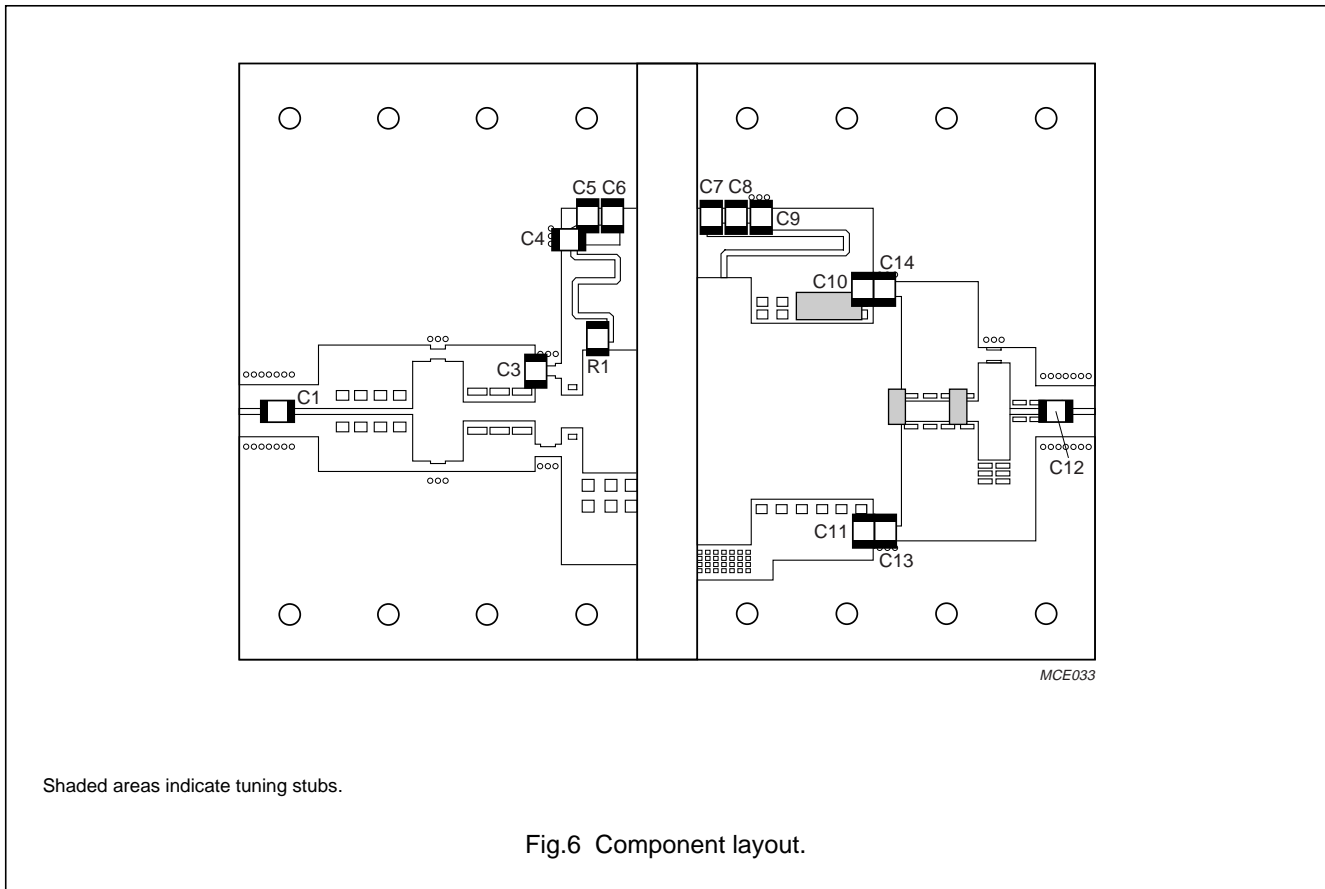
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List of components (see Fig.6)

COMPONENT	DESCRIPTION	VALUE	CATALOGUE NO.
C1, C12	capacitor	51 pF	ATC100A
C3	capacitor	6.8 pF	ATC100A
C4, C9	capacitor	47 pF	ATC100A
C6, C7	capacitor	4.7 μ F/50 V	475 50k 952
C5, C8	capacitor	2.3 nF	ATC100B
C10	capacitor	2.7 pF	ATC100A
C11	capacitor	1.0 pF	ATC100A
C13, C14	capacitor	1.5 pF	ATC100A
R1	chip resistor	82 Ω	

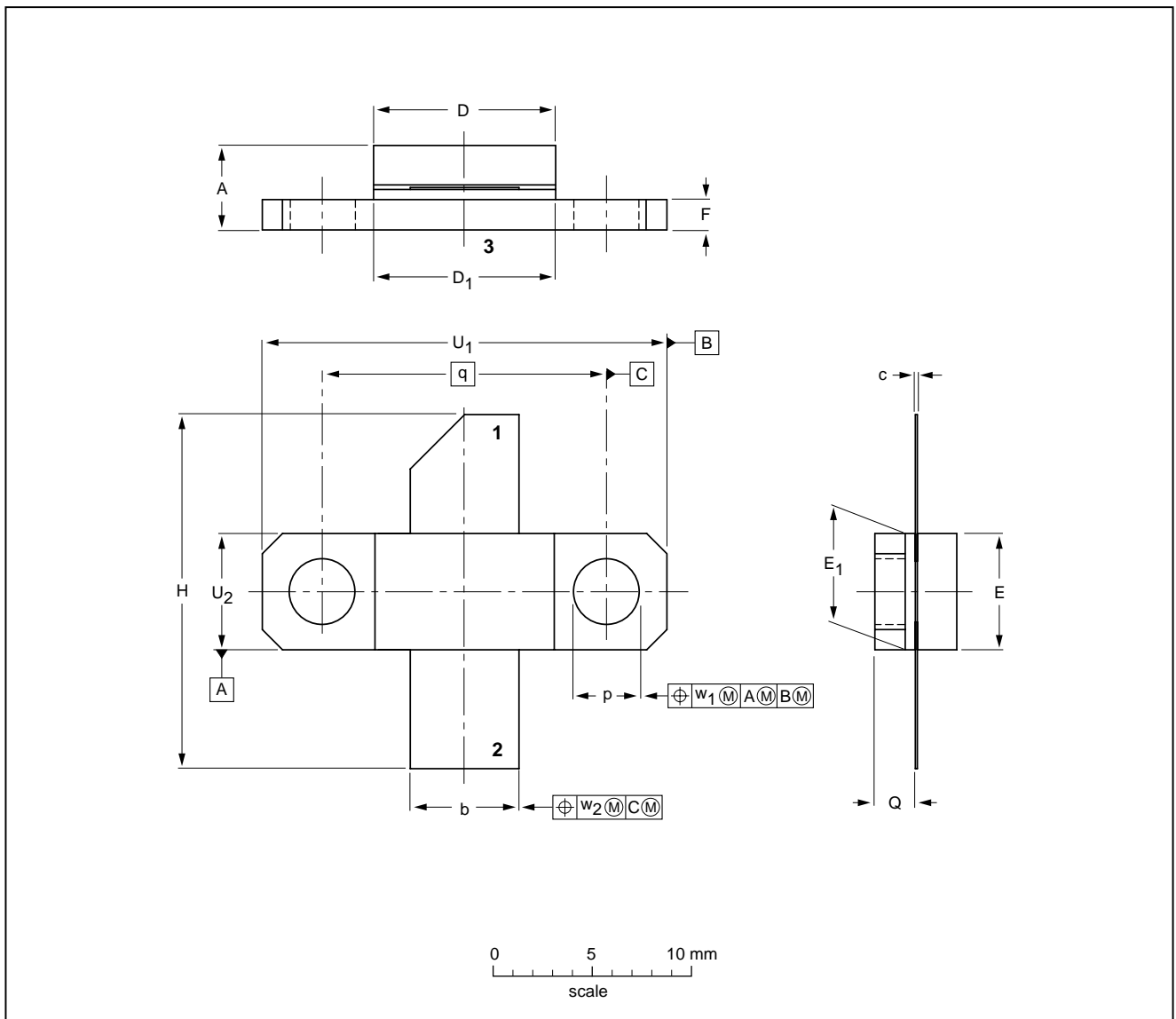
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PACKAGE OUTLINE

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads

SOT467C



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D ₁	E	E ₁	F	H	p	Q	q	U ₁	U ₂	w ₁	w ₂
mm	4.67 3.94	5.59 5.33	0.15 0.10	9.25 9.04	9.27 9.02	5.92 5.77	5.97 5.72	1.65 1.40	18.54 17.02	3.43 3.18	2.21 1.96	14.27	20.45 20.19	5.97 5.72	0.25	0.51
inch	0.184 0.155	0.220 0.210	0.006 0.004	0.364 0.356	0.365 0.355	0.233 0.227	0.235 0.225	0.065 0.055	0.73 0.67	0.135 0.125	0.087 0.077	0.562	0.805 0.795	0.235 0.225	0.010	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT467C						99-12-06 99-12-28

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DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

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Printed in The Netherlands

613524/01/pp8

Date of release: 2002 Sep 27

Document order number: 9397 750 09541

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