# 74LVC2244A

## Octal buffer/line driver; 30 Ω series termination; 5 V tolerant input/output; 3-state

Rev. 6 — 20 September 2021 Product data sheet

## 1. General description

The 74LVC2244A is an 8-bit buffer/line driver with 3-state outputs. The device can be used as two 4-bit buffers or one 8-bit buffer. The device features two output enables (1$\overline{OE}$ and 2$\overline{OE}$), each controlling four of the 3-state outputs. A HIGH on n$\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using $I_{OFF}$. The $I_{OFF}$ circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

## 2. Features and benefits

- Overvoltage tolerant inputs to 5.5 V
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low-power consumption
- Direct interface with TTL levels
- Integrated 30 Ω termination resistors
- $I_{OFF}$ circuitry provides partial Power-down mode operation
- Complies with JEDEC standard:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115B exceeds 200 V
  - CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74LVC2244AD | -40 °C to +125 °C | SO20 | plastic small outline package; 20 leads; body width 7.5 mm | SOT163-1 |
| 74LVC2244APW | -40 °C to +125 °C | TSSOP20 | plastic thin shrink small outline package; 20 leads; body width 4.4 mm | SOT360-1 |
| 74LVC2244ABQ | -40 °C to +125 °C | DHVQFN20 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm | SOT764-1 |

## 4. Functional diagram

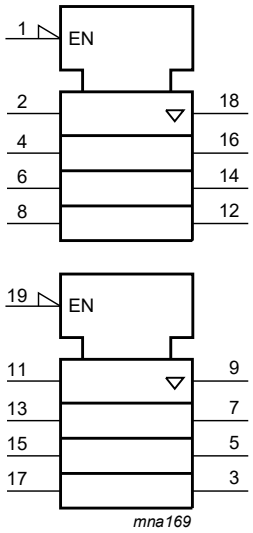



Fig. 1. IEC logic symbol

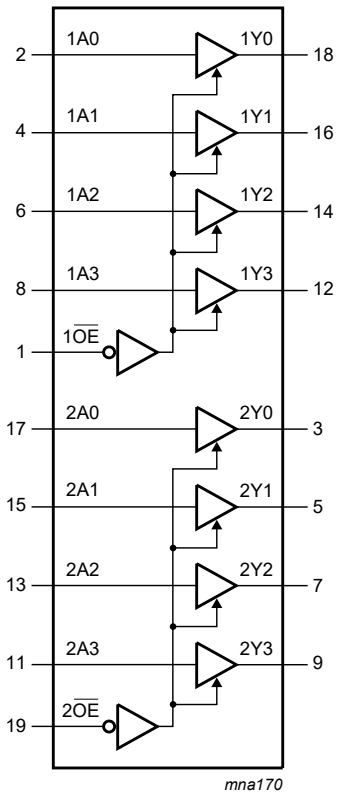



Fig. 2. Logic diagram

# 5. Pinning information

## 5.1. Pinning

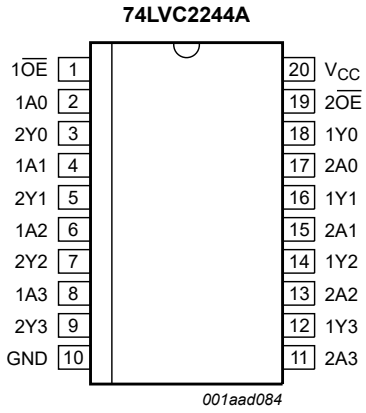
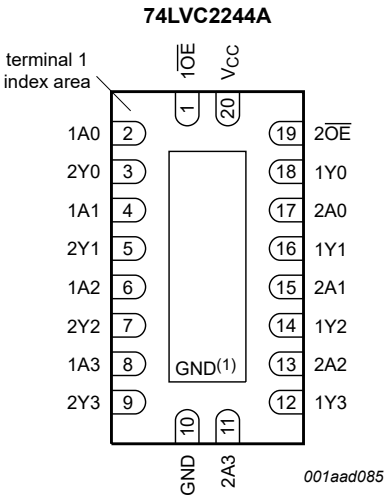



**Fig. 3. Pin configuration SOT163-1 (SO20) and SOT360-1 (TSSOP20)**




Transparent top view

(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

**Fig. 4. Pin configuration SOT764-1 (DHVQFN20)**

## 5.2. Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| $1\overline{OE}$ | 1 | output enable input (active LOW) |
| $2\overline{OE}$ | 19 | output enable input (active LOW) |
| 1A0, 1A1, 1A2, 1A3 | 2, 4, 6, 8 | data input |
| 2A0, 2A1, 2A2, 2A3 | 17, 15, 13, 11 | data input |
| 1Y0, 1Y1, 1Y2, 1Y3 | 18, 16, 14, 12 | data output |
| 2Y0, 2Y1, 2Y2, 2Y3 | 3, 5, 7, 9 | data output |
| GND | 10 | ground (0 V) |
| $V_{CC}$ | 20 | supply voltage |

# 6. Functional description

**Table 3. Functional table**

*H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state*

| Input | | Output |
|---|---|---|
| **$n\overline{OE}$** | **nAn** | **nYn** |
| L | L | L |
| L | H | H |
| H | X | Z |

# 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | -0.5 | +6.5 | V |
| $I_{IK}$ | input clamping current | $V_I < 0$ V | | -50 | - | mA |
| $V_I$ | input voltage | | [1] | -0.5 | +6.5 | V |
| $I_{OK}$ | output clamping current | $V_O > V_{CC}$ or $V_O < 0$ V | | - | ±50 | mA |
| $V_O$ | output voltage | output HIGH or LOW state | [2] | -0.5 | $V_{CC}$ + 0.5 | V |
| | | output 3-state | [2] | -0.5 | +6.5 | V |
| $I_O$ | output current | $V_O$ = 0 V to $V_{CC}$ | | - | ±50 | mA |
| $I_{CC}$ | supply current | | | - | 100 | mA |
| $I_{GND}$ | ground current | | | -100 | - | mA |
| $T_{stg}$ | storage temperature | | | -65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = -40 °C to +125 °C | [3] | - | 500 | mW |

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.
[2] The output voltage ratings may be exceeded if the output current ratings are observed.
[3] For SOT163-1 (SO20) package: $P_{tot}$ derates linearly with 12.3 mW/K above 109 °C.
For SOT360-1 (TSSOP20) package: $P_{tot}$ derates linearly with 10.0 mW/K above 100 °C.
For SOT764-1 (DHVQFN20) package: $P_{tot}$ derates linearly with 12.9 mW/K above 111 °C.

# 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 1.65 | - | 3.6 | V |
| | | functional | 1.2 | - | - | V |
| $V_I$ | input voltage | | 0 | - | 5.5 | V |
| $V_O$ | output voltage | output HIGH or LOW state | 0 | - | $V_{CC}$ | V |
| | | output 3-state | 0 | - | 5.5 | V |
| $T_{amb}$ | ambient temperature | | -40 | - | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | $V_{CC}$ = 1.65 V to 2.7 V | 0 | - | 20 | ns/V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 0 | - | 10 | ns/V |

# 9. Static characteristics

**Table 6. Static characteristics**

*At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ [1] | Max | Min | Max | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 1.2 V | 1.08 | - | - | 1.08 | - | V |
| | | $V_{CC}$ = 1.65 V to 1.95 V | $0.65V_{CC}$ | - | - | $0.65V_{CC}$ | - | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | - | - | 1.7 | - | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2.0 | - | - | 2.0 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 1.2 V | - | - | 0.12 | - | 0.12 | V |
| | | $V_{CC}$ = 1.65 V to 1.95 V | - | - | $0.35V_{CC}$ | - | $0.35V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | - | - | 0.7 | - | 0.7 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | - | - | 0.8 | - | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | | | |
| | | $I_O$ = -100 µA; $V_{CC}$ = 1.65 V to 3.6 V | $V_{CC}$ - 0.2 | $V_{CC}$ | - | $V_{CC}$ - 0.3 | - | V |
| | | $I_O$ = -2 mA; $V_{CC}$ = 1.65 V | 1.2 | - | - | 1.05 | - | V |
| | | $I_O$ = -4 mA; $V_{CC}$ = 2.3 V | 1.8 | - | - | 1.65 | - | V |
| | | $I_O$ = -6 mA; $V_{CC}$ = 2.7 V | 2.2 | - | - | 2.05 | - | V |
| | | $I_O$ = -9 mA; $V_{CC}$ = 2.7 V | 2.4 | - | - | 2.25 | - | V |
| | | $I_O$ = -12 mA; $V_{CC}$ = 3.0 V | 2.2 | - | - | 2.0 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | | | |
| | | $I_O$ = 100 µA; $V_{CC}$ = 1.65 V to 3.6 V | - | - | 0.2 | - | 0.3 | V |
| | | $I_O$ = 2 mA; $V_{CC}$ = 1.65 V | - | - | 0.45 | - | 0.65 | V |
| | | $I_O$ = 4 mA; $V_{CC}$ = 2.3 V | - | - | 0.6 | - | 0.8 | V |
| | | $I_O$ = 6 mA; $V_{CC}$ = 2.7 V | - | - | 0.4 | - | 0.6 | V |
| | | $I_O$ = 12 mA; $V_{CC}$ = 3.0 V | - | - | 0.55 | - | 0.8 | V |
| $I_I$ | input leakage current | $V_{CC}$ = 3.6 V; $V_I$ = 5.5 V or GND | - | ±0.1 | ±5 | - | ±20 | µA |
| $I_{OZ}$ | OFF-state output current | $V_I = V_{IH}$ or $V_{IL}$; $V_{CC}$ = 3.6 V; $V_O$ = 5.5 V or GND | - | ±0.1 | ±5 | - | ±20 | µA |
| $I_{OFF}$ | power-off leakage current | $V_{CC}$ = 0 V; $V_I$ or $V_O$ = 5.5 V | - | ±0.1 | ±10 | - | ±20 | µA |
| $I_{CC}$ | supply current | $V_{CC}$ = 3.6 V; $V_I = V_{CC}$ or GND; $I_O$ = 0 A | - | 0.1 | 10 | - | 40 | µA |
| $\Delta I_{CC}$ | additional supply current | per input pin; $V_{CC}$ = 2.7 V to 3.6 V; $V_I = V_{CC}$ - 0.6 V; $I_O$ = 0 A | - | 5 | 500 | - | 5000 | µA |
| $C_I$ | input capacitance | $V_{CC}$ = 0 V to 3.6 V; $V_I$ = GND to $V_{CC}$ | - | 4.0 | - | - | - | pF |

[1] All typical values are measured at $V_{CC}$ = 3.3 V (unless stated otherwise) and $T_{amb}$ = 25 °C.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

*Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 7.*

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ [1] | Max | Min | Max | |
| $t_{pd}$ | propagation delay | nAn to nYn; see Fig. 5 [2] | | | | | | |
| | | $V_{CC}$ = 1.2 V | - | 35 | - | - | - | ns |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 1.9 | 7.8 | 17.7 | 1.9 | 18.6 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.5 | 4.1 | 8.7 | 1.5 | 9.6 | ns |
| | | $V_{CC}$ = 2.7 V | 1.5 | 4.1 | 6.4 | 1.5 | 7.0 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.5 | 3.5 | 5.5 | 1.5 | 8.0 | ns |
| $t_{en}$ | enable time | $n\overline{OE}$ to nYn; see Fig. 6 [2] | | | | | | |
| | | $V_{CC}$ = 1.2 V | - | 38 | - | - | - | ns |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 2.3 | 8.9 | 19.7 | 2.3 | 20.7 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.9 | 5.0 | 10.3 | 1.9 | 11.4 | ns |
| | | $V_{CC}$ = 2.7 V | 1.5 | 5.1 | 8.1 | 1.5 | 9.0 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.0 | 4.0 | 7.1 | 1.0 | 10.5 | ns |
| $t_{dis}$ | disable time | $n\overline{OE}$ to nYn; see Fig. 6 [2] | | | | | | |
| | | $V_{CC}$ = 1.2 V | - | 9.0 | - | - | - | ns |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 2.9 | 4.7 | 9.3 | 2.9 | 9.8 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.0 | 2.6 | 5.0 | 1.0 | 5.6 | ns |
| | | $V_{CC}$ = 2.7 V | 1.5 | 3.4 | 6.4 | 1.5 | 7.0 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.5 | 3.2 | 5.4 | 1.5 | 8.0 | ns |
| $t_{sk(o)}$ | output skew time | $V_{CC}$ = 3.0 V to 3.6 V [3] | - | - | 1.0 | - | 1.5 | ns |
| $C_{PD}$ | power dissipation capacitance | per input; $V_I$ = GND to $V_{CC}$ [4] | | | | | | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | - | 1.8 | - | - | - | pF |
| | | $V_{CC}$ = 2.3 V to 2.7 V | - | 4.9 | - | - | - | pF |
| | | $V_{CC}$ = 3.0 V to 3.6 V | - | 7.7 | - | - | - | pF |

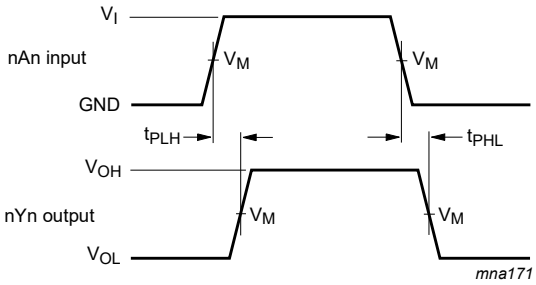
[1] Typical values are measured at $T_{amb}$ = 25 °C and $V_{CC}$ = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.

[2] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$.
$t_{en}$ is the same as $t_{PZL}$ and $t_{PZH}$.
$t_{dis}$ is the same as $t_{PLZ}$ and $t_{PHZ}$.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
$f_i$ = input frequency in MHz; $f_o$ = output frequency in MHz
$C_L$ = output load capacitance in pF
$V_{CC}$ = supply voltage in Volts
N = number of inputs switching
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

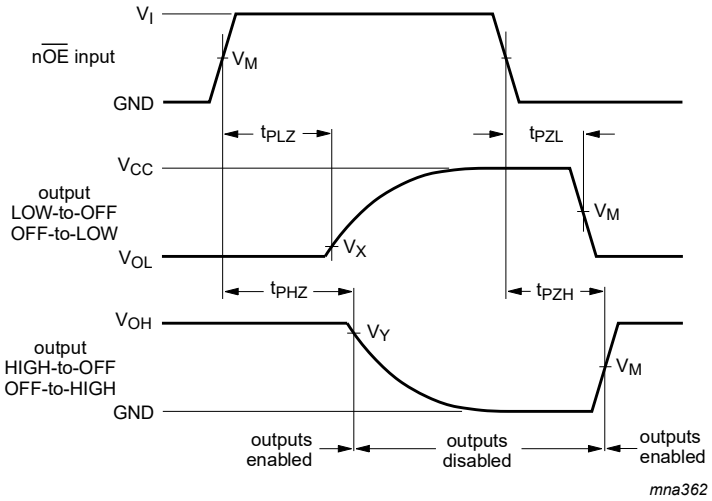
## 10.1. Waveforms and test circuit




Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Fig. 5. The input (nAn) to output (nYn) propagation delays**



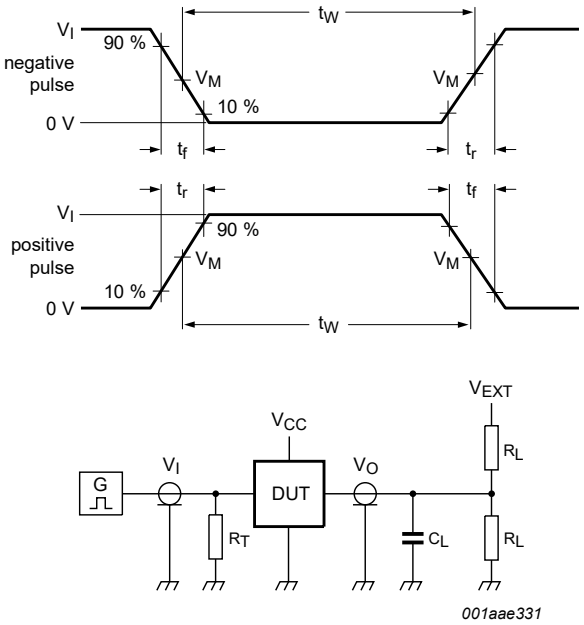

Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Fig. 6. 3-state enable and disable times**

**Table 8. Measurement points**

| Supply voltage | Input | | Output | | |
|---|---|---|---|---|---|
| $V_{CC}$ | $V_I$ | $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| 1.2 V | $V_{CC}$ | 0.5 × $V_{CC}$ | 0.5 × $V_{CC}$ | $V_{OL}$ + 0.15 V | $V_{OH}$ - 0.15 V |
| 1.65 V to 1.95 V | $V_{CC}$ | 0.5 × $V_{CC}$ | 0.5 × $V_{CC}$ | $V_{OL}$ + 0.15 V | $V_{OH}$ - 0.15 V |
| 2.3 V to 2.7 V | $V_{CC}$ | 0.5 × $V_{CC}$ | 0.5 × $V_{CC}$ | $V_{OL}$ + 0.15 V | $V_{OH}$ - 0.15 V |
| 2.7 V | 2.7 V | 1.5 V | 1.5 V | $V_{OL}$ + 0.3 V | $V_{OH}$ - 0.3 V |
| 3.0 V to 3.6 V | 2.7 V | 1.5 V | 1.5 V | $V_{OL}$ + 0.3 V | $V_{OH}$ - 0.3 V |




Test data is given in Table 9.

Definitions for test circuit:

$R_L$ = Load resistance.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$V_{EXT}$ = External voltage for measuring switching times.

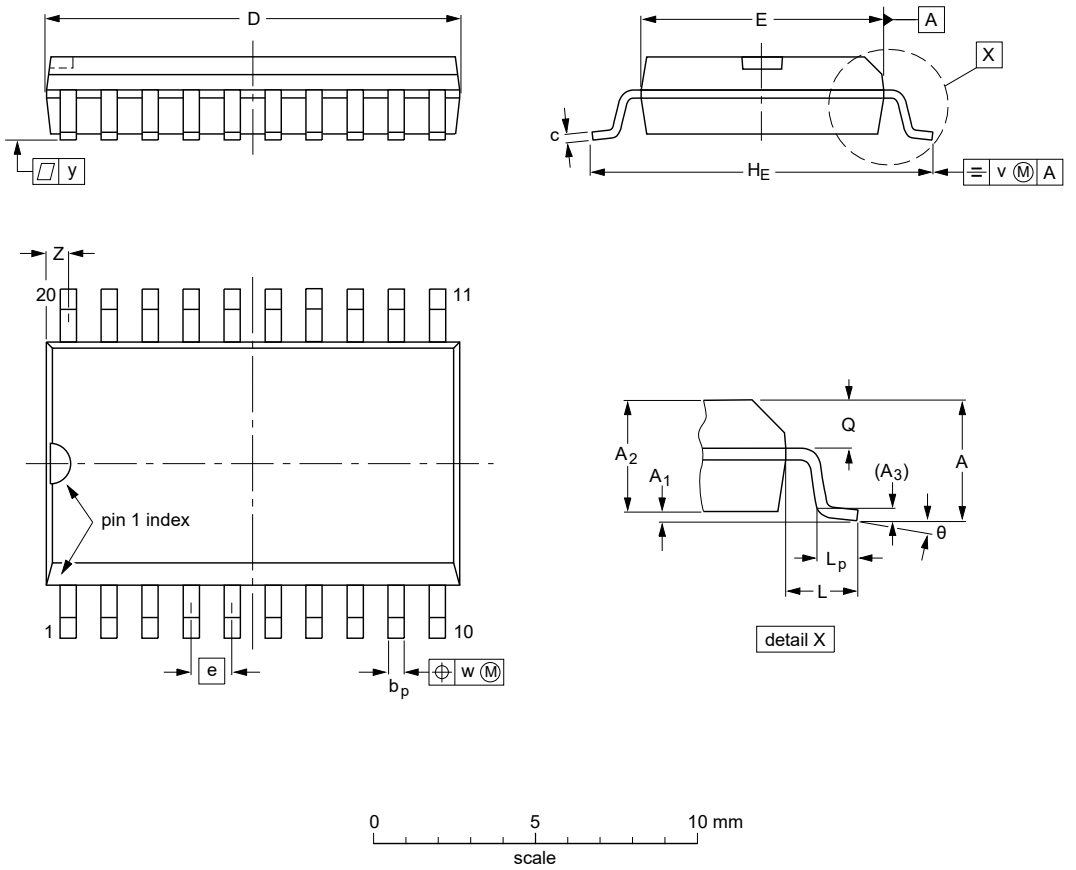
**Fig. 7. Test circuit for measuring switching times**

**Table 9. Test data**

| Supply voltage | Input | | Load | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PLH}$, $t_{PHL}$ | $t_{PLZ}$, $t_{PZL}$ | $t_{PHZ}$, $t_{PZH}$ |
| 1.2 V | $V_{CC}$ | ≤ 2 ns | 30 pF | 1 kΩ | open | 2 × $V_{CC}$ | GND |
| 1.65 V to 1.95 V | $V_{CC}$ | ≤ 2 ns | 30 pF | 1 kΩ | open | 2 × $V_{CC}$ | GND |
| 2.3 V to 2.7 V | $V_{CC}$ | ≤ 2 ns | 30 pF | 500 Ω | open | 2 × $V_{CC}$ | GND |
| 2.7 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | 2 × $V_{CC}$ | GND |
| 3.0 V to 3.6 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | 2 × $V_{CC}$ | GND |

# 11. Package outline

**SO20: plastic small outline package; 20 leads; body width 7.5 mm** **SOT163-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.65 | 0.3<br>0.1 | 2.45<br>2.25 | 0.25 | 0.49<br>0.36 | 0.32<br>0.23 | 13.0<br>12.6 | 7.6<br>7.4 | 1.27 | 10.65<br>10.00 | 1.4 | 1.1<br>0.4 | 1.1<br>1.0 | 0.25 | 0.25 | 0.1 | 0.9<br>0.4 | 8°<br>0° |
| inches | 0.1 | 0.012<br>0.004 | 0.096<br>0.089 | 0.01 | 0.019<br>0.014 | 0.013<br>0.009 | 0.51<br>0.49 | 0.30<br>0.29 | 0.05 | 0.419<br>0.394 | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016 | |

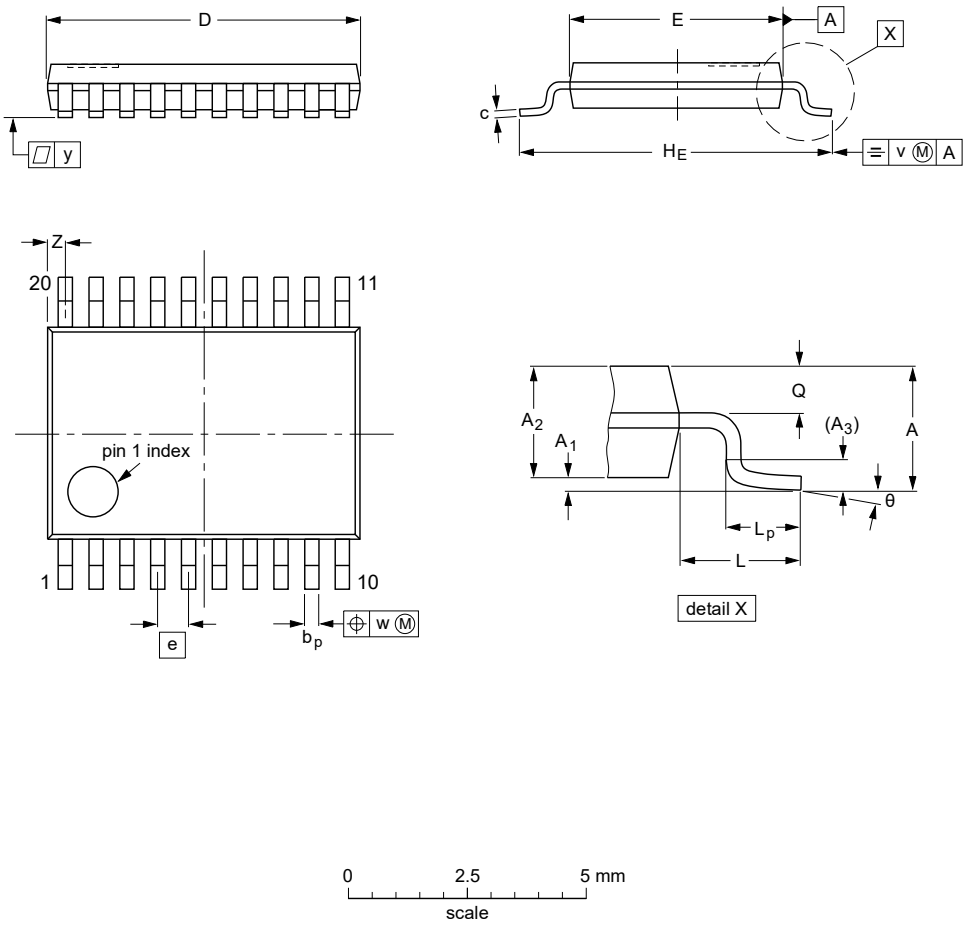
**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT163-1 | 075E04 | MS-013 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig. 8. Package outline SOT163-1 (SO20)**

**TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm** **SOT360-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 6.6<br>6.4 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.5<br>0.2 | 8°<br>0° |

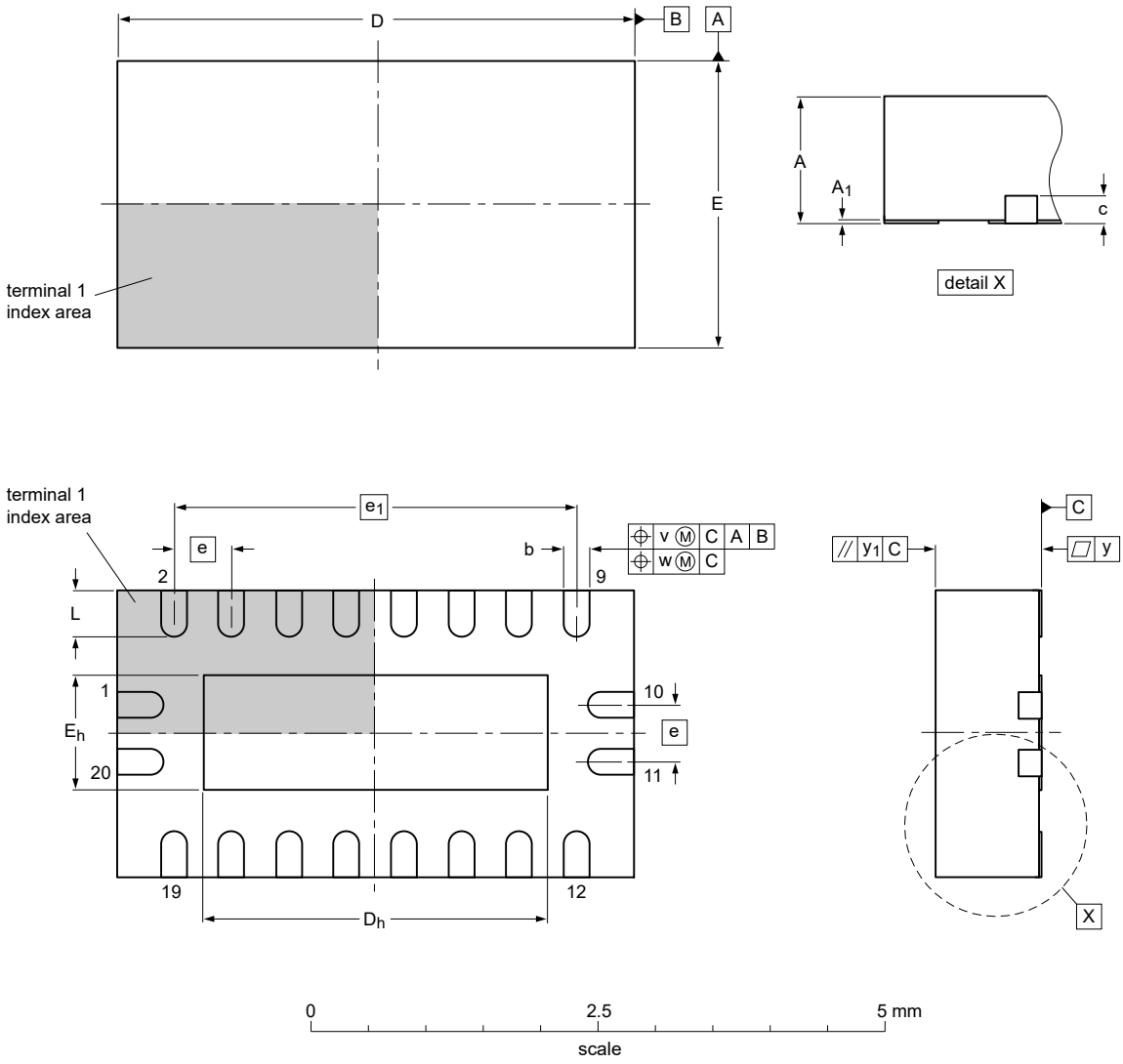
**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT360-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig. 9. Package outline SOT360-1 (TSSOP20)**

**DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm** **SOT764-1**




Dimensions (mm are the original dimensions)

| Unit | | $A^{(1)}$ | $A_1$ | b | c | $D^{(1)}$ | $D_h$ | $E^{(1)}$ | $E_h$ | e | $e_1$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | max | 1.00 | 0.05 | 0.30 | | 4.6 | 3.15 | 2.6 | 1.15 | | | 0.5 | | | | |
| mm | nom | 0.90 | 0.02 | 0.25 | 0.2 | 4.5 | 3.00 | 2.5 | 1.00 | 0.5 | 3.5 | 0.4 | 0.1 | 0.05 | 0.05 | 0.1 |
| | min | 0.80 | 0.00 | 0.18 | | 4.4 | 2.85 | 2.4 | 0.85 | | | 0.3 | | | | |

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

*sot764-1_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT764-1 | - - - | MO-241 | - - - | | | ~~03-01-27~~ 14-12-12 |

**Fig. 10. Package outline SOT764-1 (DHVQFN20)**

## 12. Abbreviations

**Table 10. Abbreviations**

| Acronym | Description |
|---|---|
| CDM | Charged Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

## 13. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74LVC2244A v.6 | 20210920 | Product data sheet | - | 74LVC2244A v.5 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• Section 1 updated.<br>• Type number 74LVC2244ADB (SOT339-1/SSOP20) removed.<br>• Section 7: Derating values for $P_{tot}$ total power dissipation updated.<br>• Table 8: Measurement points table added.<br>• Fig. 10: Package outline drawing SOT764-1 (DHVQFN20) updated. | | | |
| 74LVC2244A v.5 | 20111103 | Product data sheet | - | 74LVC2244A v.4 |
| Modifications: | • The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• Table 4, Table 5, Table 6, Table 7 and Table 9: values added for lower voltage ranges. | | | |
| 74LVC2244A v.4 | 20040407 | Product specification | - | 74LVC2244A v.3 |
| 74LVC2244A v.3 | 20021213 | Product specification | - | 74LVC2244A v.2 |
| 74LVC2244A v.2 | 20020618 | Product specification | - | 74LVC2244A v.1 |
| 74LVC2244A v.1 | 19990930 | Product specification | - | - |

# 14. Legal information

## Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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